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Miniaturized Foldable Electrodes with Direct CMOS Integration for Implantable Applications

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***Abstract*—This study demonstrates the feasibility of directly integrating foldable microelectrodes (starting from 250μm width and 1600μm length) with CMOS front-end for implantable biomedical applications. Mechanical robustness was evaluated through Finite Element Method (FEM) simulations and validated by implantation into an agarose phantom, showing no structural failure. Electrical performance was assessed using Electrochemical Impedance Spectroscopy (EIS) measurement, with results in agreement with values reported in the literature, confirming the integrity of the microfabrication process. Additionally, an electrochemical sensing front-end was also designed, consisting of a full-custom digital potentiostat to illustrate functional capability. This study presents a complete and reproducible microfabrication workflow, providing a promising foundation for future development of highly integrated, minimally invasive bioelectronic interfaces.**

***Index Terms*—Neural Implant, Finite Element Method, Microfabrication, Electrochemical Impedance Spectroscopy, Dopamine Sensing, Potentiostat.**

I. Introduction

Implantable electrodes have played a central role in brain stimulation research, particularly in the realm of neuromodulation, where targeted electrical stimulation is used to alter neural activity. [1]–[8] Their use has driven major advancements in neuroscience, deepening our understanding of brain function and contributing to therapeutic strategies for a variety of neurological and psychiatric disorders.

Progress in neurophysiology has been greatly accelerated by the development and application of microelectrodes, which allow high-resolution investigation of individual neuronal activity and the broader dynamics of neural networks. Due to their small diameter (typically 50–100 μm), single microelectrodes induce minimal tissue disruption and permit localized recordings [9]. However, their limited spatial sampling restricts their utility in capturing the coordinated activity across neural populations. This limitation has catalyzed the shift toward multielectrode arrays (MEAs), which support simultaneous recordings from multiple sites within the brain [10]–[13], including the widely used Utah Intracortical Electrode Array (UIEA) and Michigan probes. These devices offer superior mechanical stability and scalability for large-scale neural recordings. But they often suffer from poor long-term biocompatibility. In parallel, nonconventional electrode configurations [7], [14]–[16] employ polymers with mechanical properties that match those of the surrounding tissue, enhancing long-term biocompatibility. However, establishing a stable and efficient electrical interface between electrodes and implantable electronics remains a key challenge. Today, most microelectrodes are manually affixed to CMOS chips using conductive silver paste and wire bonding. While widely adopted, this manual assembly introduces significant limitations in terms of reliability, repeatability, and miniaturization. Moreover, the electrical characteristics of connection are suboptimal for high-performance recording. Although the UIEA supports direct integration with CMOS, it suffers from the so-called "bed-of-needles" effect—low mechanical conformity that can cause substantial damage to surrounding tissue [17]. A comparative overview of the advantages and limitations of probe types is provided in Table I. To overcome these limitations, the Smart Micro Neural Dust project [18]–[20] proposed the novel architecture of self-electrodeized CMOS die for a decentralized application, illustrated in Fig. 1(a). To this end, we designed a miniature digital potentiostat for dopamine detection and developed a detailed process flow for microelectrode fabrication.

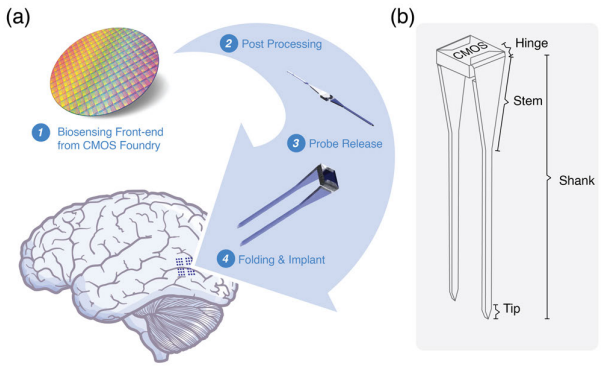

Fig. 1. (a) Directly integrating foldable electrodes to CMOS front-end. (b) The basic configuration of the foldable implant.

II. Materials and System Design

This study aims to propose a CMOS-compatible microfabrication process that enables the direct integration of electrode structures onto CMOS dies through a post-processing step. To ensure the feasibility and effectiveness of this approach, several critical factors have been considered: signal acquisition performance, mechanical integrity, long-term reliabil-

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TABLE I
ADVANTAGES AND DISADVANTAGES OF DIFFERENT NEURAL IMPLANTS, LISTED IN THE ORDER OF THEIR DEVELOPMENT

Probe Type	Advantages	Disadvantages
Tungsten	High mechanical strength Good conductivity Ease of fabrication Cheaper	Mismatched mechanical properties Difficult to integrate with Microfabrication
MICHIGAN	Detailed mapping of neural signals Reliable signal acquisition Compatibility with Microfabrication	Wiring complexity
TETRODE	Greater sensitivity in recording Comprehensive view of brain activity Noise reduction	Wiring complexity Limited coverage
UIEA	High spatial resolution Flexibility and precision Reliable signal acquisition	Mismatched mechanical properties
Nonconventional Electrodes	High bio compatibility Flexibility and precision Reliable signal acquisition	Wiring complexity Difficult to integrate with Microfabrication

ity, and biocompatibility. Among these, signal performance and mechanical robustness are the primary focus of this work, while reliability and biocompatibility are addressed through careful material selection and structural design. To enhance biocompatibility, the strategy emphasizes minimizing the electrode-tissue interface area by reducing the overall implant size and exploring the use of wireless communication to eliminate external wiring. Platinum (Pt) is selected as the electrode material due to its well-established biocompatibility and electrochemical stability, making it a suitable interface for neural recording applications. On the other hand, the shanks must have sufficient mechanical strength to penetrate brain tissue, while also being ductile enough to allow bending at the hinge. Aluminum is a suitable candidate for our application due to its low cost, corrosion resistance, light weight, and, most importantly, compatibility with CMOS processes.

The electrode design comprises four principal components (Fig. 1(b)): Hinge – Connects the electrode shanks to the primary CMOS chip and provides connection pads for secondary electronics. Shank – A slender structure enabling targeted penetration into brain tissue, optimized for mechanical robustness. Pt recording electrodes – The biosensing sites are deposited on the outer SiO_2 layer (insulated from aluminum), leading to the hinge interface. The shank body is composed of a SiO_2–Si–SiO_2–Al–SiO_2 heterostructure.

To address this, FEM was conducted using COMSOL Multiphysics to simulate mechanical stresses and optimize structural parameters. Based on these simulations, the foldable electrodes were fabricated and evaluated. Mechanical validation was performed via implantation into agarose gel, simulating the mechanical resistance of brain tissue. Electrical characteristics of the electrodes were analyzed using EIS, and a miniaturized digital potentiostat was designed to enable low-power dopamine detection from the electrodes.

III. RESULTS AND DISCUSSION

A. In-silico simulation

The implants are usually inserted under the dura mater and penetrate the pia mater into the arachnoid. This pia-arachnoid complex (PAC) is often simulated as a thin layer of hyperelastic shell covering a hyperviscous bulk substrate. If the implant creates a deep dimple before the penetration of the pia mater, the brain tissue underneath is subject to several pressure-induced injuries [17]. A good implant must be stiff enough to withstand the force applied during implantation while having a small cross-sectional area to minimize its interference with the surrounding tissue. To find the optimum parameters, a model was built in COMSOL Multiphysics.

Buckling is a physical phenomenon when a gradually increasing force induces a sudden structure deformation. It is described by Euler's Column Formula [21] in (1):

$$P = \frac{m\pi^2 EI}{{L_U}^2} \tag{1}$$

where P is the Critical buckling load, E is the Young's modulus, I is the second moment of inertia, and L_U is the unsupported length during insertion. m is a constant delineating the end condition of the beam; in our design, it is more similar to both side fixed condition, hence $m = 0.5$.

The preset linear buckling study is used to investigate the mechanical properties of the folded probe. Fixed constraints are applied at the boundaries of the two electrode tips. The CMOS chip is allowed to move along the insertion direction via a prescribed displacement setting. Only the first buckling mode is being investigated.

The parameters, such as Si support thickness and length of the electrode, are swept. Both the electrode with SiO_2 coating and without SiO_2 coating are being studied.

The critical load is computed and plotted against the optimizing parameters; the results are shown in Fig. 2(a) and 2(b). Four possible deformations are predicted by the machine; they happen at different Si backbone thicknesses. The largest deformation occurs closer and closer to the hinge part when the Si thickness increases. Without Si backbone, the probe collapses near the center of the shank, which conforms with the findings from preliminary experiments. When t_{Si} reaches 25 μm thickness, the critical buckling load reaches a plateau. This corresponds to the fourth buckling profile in Fig. 2, where the hinge becomes the vulnerable structure. A 30 μm of Si backbone with SiO_2 layer can provide buckling resistance up to 250 mN. The critical load reduces as the shank length increases. For the SiO_2 covered shank, its critical buckling load drops dramatically after 1.8 mm.

B. Microfabrication

The parameters defined in the simulation mentioned above are used to design the foldable electrodes. The electrodes are deliberately placed opposite to each other on the edge of a

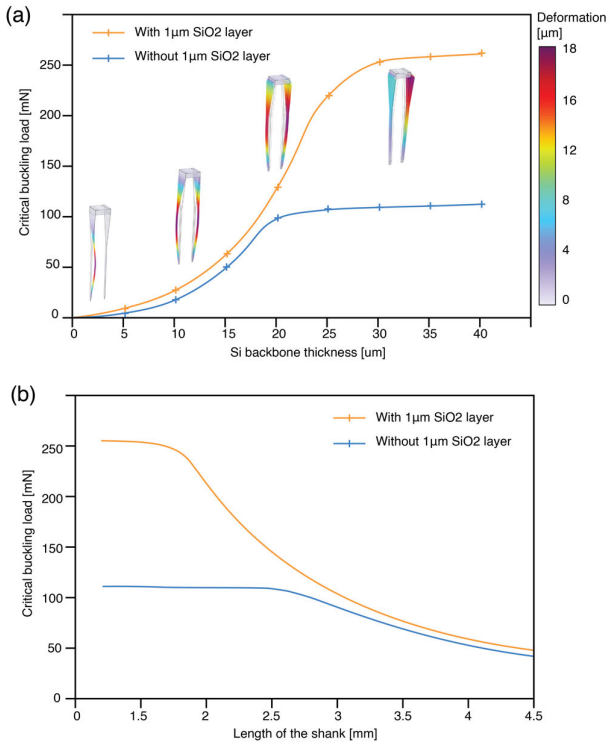

Fig. 2. (a) The linear buckling simulation at different Si backbone thicknesses, with the four types of deformation taking place at different thicknesses. (b) The linear buckling simulation at different shank lengths.

virtual CMOS chip of 500 μm x 500 μm. A 200 nm platinum layer is added to the surface of the shank, enabling high biocompatibility. The entire electrode is insulated by SiO_2; windows are opened at the sensing site at the tip and at the pad near the hinge. The area of the sensing site is designed to be 400 μm^2. A comprehensive process flow is developed to realize the design, Fig. 3(a).

Aluminum and platinum are patterned next to the CMOS chip using a sequence of sputtering, photolithography, and dry etching. Chloride chemistry is used to remove Aluminum via Reactive Ion Etching (RIE), while platinum is removed via a broad beam etcher using Argon ions. These two metallic layers are insulated using SiO_2 deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). The open sites are defined by photolithography and etched using C_4F_8 chemistry RIE. The surface profile and the electrode patterns of the front side fabrication is shown in Fig. 3(b)&(c). The sample then undergoes backside grinding to remove the bulky Si substrate, and the induced stress is released by a short Si RIE step (step: Si thinning). From now on the front side is protected by a 10μm parylene layer. This avoids direct contact with the electrostatic clamps and prevents other contamination. To fabricate the Si backbone, a two step Si etching is employed. In the first step, the trench between the CMOS chip and the shanks is defined (diagram 6, step: Si DRIE 1). After stripping the photoresist from the previous step, the rest of the Si is etched, the etching area is defined by the SiO_2 mask produced in step SiO_2 Dry Etching 2 (diagram 5). Fig. 3(d) shows that the front side features are well aligned with the Si backbone at the hing location. The backside is insulated by another layer of SiO_2 deposited using sputtering at room temperature. By etching the parylene protecting layer the devices are released and fall into the dummy cavity wafer.

To fold the probes into their operational shape with high reproducibility, a 3D printed micrometer scale die cast mold is produced, the casting procedure is illustrated in Fig. 3(e). Ultimately, the electrodes are implanted into an agarose phantom (0.6% agarose). The electrodes penetrated the phantom without buckling, and no deflection of the shank was observed. The result is shown in Fig. 3(f).

C. Impedance Characterization

EIS was employed to characterize the impedance of the electrodes in a 10 mM phosphate-buffered saline (PBS) solution. Measurements were conducted using an Autolab PGSTAT302N (Metrohm), which recorded impedance magnitude and phase across a frequency range of 1 Hz to 100 kHz for three electrode samples.

The impedance spectrum, Fig. 4 (a), is consistent with previously reported data for electrodes of comparable size and geometry [22]. The curve represents the average of the three electrodes, while the relatively large standard deviation observed is attributed to variations in radius of few μm, compatible with the critical resolution of photolithography. At 1 Hz, a value of approximately 600 MΩ was measured. These results confirm robust electrical connectivity between the contact pad and sensing site, with no electrical failure.

D. Dopamine sensing electrochemical cell

To enable low-power, miniaturized readout of dopamine levels via our fabricated microelectrodes, we employed a fully digital potentiostat [23], [24] fabricated in TSMC 180 nm CMOS. The schematic and microphotograph of the digital potentiostat are shown in Fig. 4(b)-(e). The potentiostat operates in a standard three-electrode electrochemical cell configuration, applying a fixed potential difference between the WE and RE while sourcing/sinking current through the CE. The RE is biased at a stable 200 mV using an on-chip 4-transistor voltage reference, while the WE is connected to the supply voltage (400 mV), thereby setting the WE-RE potential at 200 mV, suitable for dopamine oxidation. This voltage is maintained by a negative feedback loop formed by a digital operational transconductance amplifier (OTA) that regulates the CE current. The design integrates the sensing, digitization, and control functions into a unified, fully digital architecture, eliminating the need for traditional analog frontends such as transimpedance amplifiers (TIAs) [22], [25] and analog-to-digital converters (ADCs) [26]. Instead, the faradaic current is directly translated into a pair of pulse streams (Dp and Dn) generated by PMOS and NMOS transistors in the output stage as current sources. The entire potentiostat core occupies

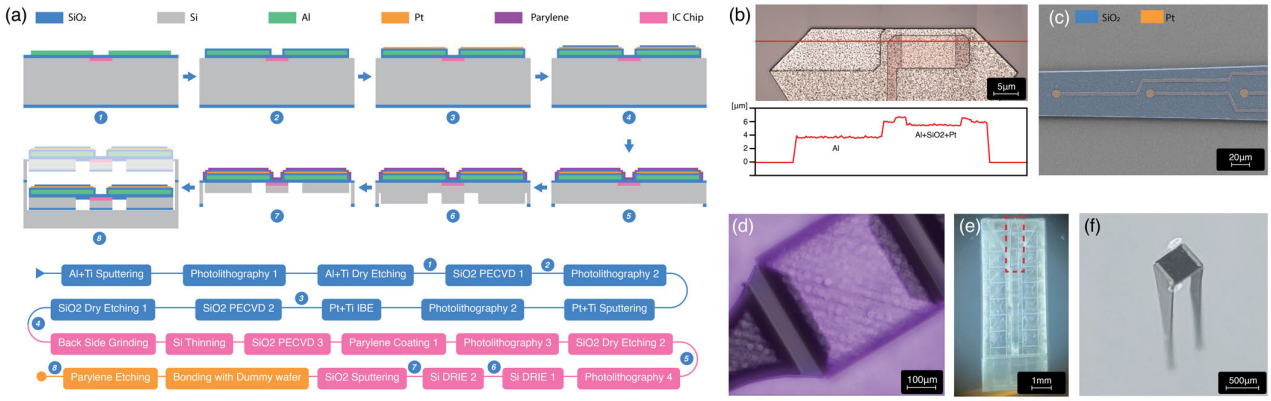

Fig. 3. (a) The process flow of the microfabrication. The diagrams correspond to the critical steps along the manufacturing of the foldable electrodes (legend: Magenta: CMOS, Grey: Si, Blue: SiO_2, Green: Al, Orange: Pt, Purple: Parylene). (b) The surface profile of the top side features at the hinge region acquired using a mechanical profilometer. (c) SEM image of Pt electrodes patterns on the shank insulated by SiO_2, with false colors. (Orange: Pt; Blue: SiO_2)(d) A microscope photo take using backside infrared illumination, showing the good alignment between the top and bottom side patterns. (e) 3D printed die casting mold, the electrode is highlighted by the red dashline. (f) Implantation of the folded electrodes into agarose phantom.

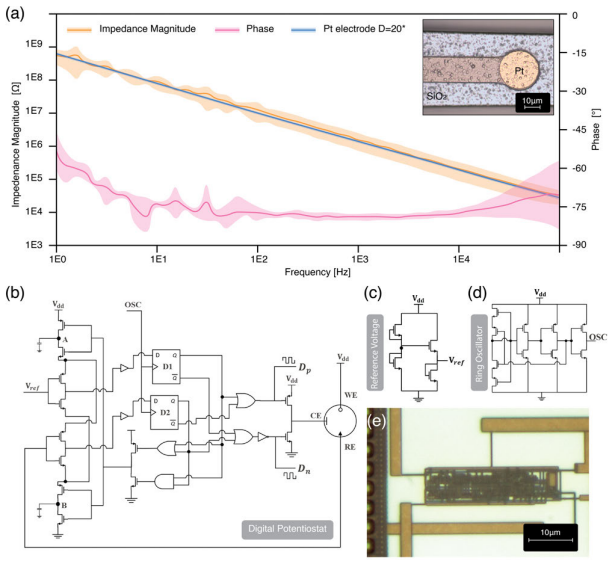

Fig. 4. (a) The EIS measurement, with the working electrode show in the insert.*Data adapted from [22] (b) Digital potentiostat for DA measurement. (c) Reference voltage. (d) Ring oscillator. (e) Microimage of the CMOS electronic front-end.

just 260 μm^2 and consumes 1.2 nW when operated at 0.4 V. Including the 3-stage ring oscillator and voltage reference, the total system consumes only 9.2 nW and occupies 370 μm^2. The ring oscillator [27], implemented using dynamic leakage suppression logic, generates a 25kHz clock signal for the digital logic while maintaining ultra-low energy operation. These specifications make the proposed potentiostat exceptionally well-suited for ultra-miniaturized, wirelessly-powered implants. After CMOS fabrication, this chip is wire bonded at the top of the foldable micro-electrodes.

IV. Conclusion

In this study, we demonstrated the feasibility of directly integrating implantable micro-electrodes with CMOS circuitry. The concept was first validated through in-silico simulations for parameter optimization. Based on the simulation results, a 30μm-thick silicon backbone was added to the aluminum shank to enhance mechanical stability while minimizing tissue damage. With a SiO_2 passivation layer, the length can extend to 1.8 mm with sufficient rigidity.

We then fabricated foldable electrodes positioned on opposite edges of a dummy CMOS die. Using a 3D-printed mold, the electrodes were folded and implanted into an agarose phantom without mechanical failure. EIS characterization of the sensing sites confirmed electrical integrity, with results consistent with the existing literature. We have also developed a low-power, miniaturized front-end. Multiple units can be integrated within the area of a single dummy die, enabling multi-channel detection. As a future direction, electrodes will be directly integrated onto the front-end and tested in an in vitro environment to evaluate long-term reliability.

In conclusion, this foldable electrode platform presents a promising and versatile solution for decentralized in vivo biomedical applications, such as biosensing, neural recording, and stimulation, by offering stronger, more reliable connections to embedded IC circuits while significantly minimizing the overall device footprint.

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