Journal of Electronic Science and Technology 20 (2022) 100177

Contents lists available at ScienceDirect

Journal of Electronic Science and Technology

journal homepage: www.keaipublishing.com/en/journals/journal-of-electronic-science-and-technology/

Invited paper

Redox memristors with volatile threshold switching behavior for neuromorphic computing

Yu-Hao Wang [a,b], Tian-Cheng Gong [a,b,c], Ya-Xin Ding [a,b], Yang Li [c], Wei Wang [c], Zi-Ang Chen [d,e], Nan Du [d,e], Erika Covi [f], Matteo Farronato [g], Daniele Ielmini [g], Xu-Meng Zhang [a,b,h,**], Qing Luo [a,b,c,*]

[a] *Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, 100029, China*
[b] *University of Chinese Academy of Sciences, Beijing, 100049, China*
[c] *Peng Cheng Laboratory, Shenzhen, 518055, China*
[d] *Institute for Solid State Physics, University of Jena, Jena, 07743, Germany*
[e] *Department of Quantum Detection, Leibniz Institute of Photonic Technology, Jena 07743, Germany*
[f] *Nanoelectronic Materials Laboratory, Dresden, 01187, Germany*
[g] *Department of Electronics, Information and Bioengineering, Politecnico di Milano, Milan, 20133, Italy*
[h] *Frontier Institute of Chip and System, Fudan University, Shanghai, 200433, China*

ARTICLE INFO

Keywords:
Memristors
Threshold switching
Neuromorphic computing

ABSTRACT

The spiking neural network (SNN), closely inspired by the human brain, is one of the most powerful platforms to enable highly efficient, low cost, and robust neuromorphic computations in hardware using traditional or emerging electron devices within an integrated system. In the hardware implementation, the building of artificial spiking neurons is fundamental for constructing the whole system. However, with the slowing down of Moore's Law, the traditional complementary metal-oxide-semiconductor (CMOS) technology is gradually fading and is unable to meet the growing needs of neuromorphic computing. Besides, the existing artificial neuron circuits are complex owing to the limited bio-plausibility of CMOS devices. Memristors with volatile threshold switching (TS) behaviors and rich dynamics are promising candidates to emulate the biological spiking neurons beyond the CMOS technology and build high-efficient neuromorphic systems. Herein, the state-of-the-art about the fundamental knowledge of SNNs is reviewed. Moreover, we review the implementation of TS memristor-based neurons, and their systems, and point out the challenges that should be further considered from devices to circuits in the system demonstrations. We hope that this review could provide clues and be helpful for the future development of neuromorphic computing with memristors.

* Corresponding author. Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, 100029, China.

** Corresponding author. Key Laboratory of Microelectronic Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, 100029, China.

E-mail addresses: xumengzhang@fudan.edu.cn (X.-M. Zhang), luoqing@ime.ac.cn (Q. Luo).

https://doi.org/10.1016/j.jnlest.2022.100177
Received 19 June 2022; Received in revised form 3 November 2022; Accepted 11 November 2022
Available online 17 November 2022

1. Introduction

In recent years, with the continuous development of neuroscience, big data, and deep learning algorithms, conventional electronic computing systems have shown superior capabilities in image classification, speech recognition, natural language processing, task decision-making, intelligent driving, and other fields [1–5]. However, there are challenges associated with the energy inefficiency and latency due to the von Neumann bottleneck and memory wall [6–8]. To further improve computing efficiency, neuromorphic computing inspired by the human brain is a promising candidate. Neuromorphic computing aims to study the most efficient computing and learning processes belonging to the structure and mechanism of the brain, including neurons and the connecting synapses between them, and reproduce them in hardware. Neuromorphic computing has the characteristics of event-driven, parallel computing, analog computing, and in-memory computing [9], all features are of paramount importance to achieve low-power and high-density computing systems. In particular, these characteristics are inherent in spiking neural networks (SNNs), considered as the third generation of neural networks, which process the information encoded in the form of spikes only when necessary, i.e., when an event occurs.

In the hardware implementation, memristors have been recognized as a new platform for neuromorphic computing beyond the CMOS technology. Memristors rely on ion dynamics processes which are similar to biological neurons and synapses, and thus can faithfully emulate the related functions of neurons and synapses [6]. Besides, according to Ohm's law and Kirchhoff's law, the arrays of memristors can realize the dot product operation ($\mathrm{OUT}_j = \sum_i \mathrm{IN}_i \times W_{i,j}$, where IN_i is the element of an input vector, $W_{i,j}$ is the element of the weight matrix, and OUT_j is the element of the output vector) in the neural networks naturally [10,11], and have the characteristics of analog computing, parallel computing, and in-memory computing, simultaneously.

Memristors are 2-terminal devices consisting of two metal electrodes sandwiching a typically thin switching layer [12,13]. Different

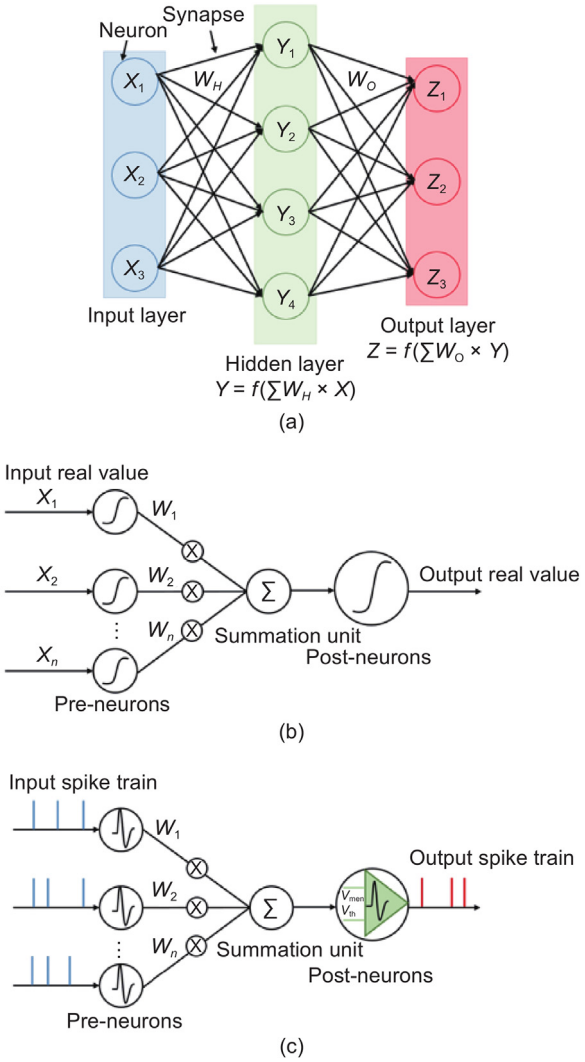


Fig. 1. Neural network structures and the comparison between ANN and SNN: (a) typical two-layer neural network schematic, including the input, hidden, and output nodes; (b) working schematic of ANNs; (c) working schematic of SNNs.

types of switching dielectrics utilize different mechanisms of the memory state transition [14]. According to the different transformation mechanisms, such as the redox [15], phase change [16], ferroelectric tunnel junction (FTJ) effect [17], magnetoresistive effect [18], memristors have a variety of applications. In particular, redox memristors have received great attention due to their fast switching speed, excellent endurance, and scalability [15,19,20]. Redox memristors can be divided into two categories, non-volatile and volatile. Non-volatile memristors have been extensively reviewed in previous work for storage or to emulate synapses, which have been extensively reported and reviewed, and thus will not be described in this review.

There are three types of volatile memristors with threshold switching (TS) characteristics: TS memristors based on insulator-metal transition (IMT) [21,22], TS memristors based on conductive metal filaments [23–25], and TS memristors based on defect assisted tunneling [26]. These TS memristors are originally used as selectors and have shown remarkable performance in the field of neuromorphic computing.

In this review, recent progress on the applications of TS memristors in the field of neuromorphic computing is reviewed. SNN is introduced by classifying its working mechanism and advantages. Neuron models of SNNs are discussed for different emulation principles. Moreover, applications of TS memristors in artificial neurons, SNNs implementation, and artificial spiking afferent nerves are presented in detail.

2. Neural networks

2.1. Algorithmic models of neural network

The high efficiency of the brain can be attributed to three factors: Integration of data storage and calculation, highly interconnected functional topology, and time-dependent neurons and synapses. The basic components of biological neural networks are neurons and synapses [27]. The term "neuromorphic engineering" was first proposed in the 1990s, specifically referring to the use of analog circuits to emulate the functions of biological neurons and synapses to build a computing system similar to the brain [28]. In recent years, neuromorphic computing also refers to implementing a neural network through analog, digital, or mixed digital-analog circuits and software algorithms, achieving a similar effect as the biological neural network. Fig. 1 (a) is the schematic diagram of a typical two-layer neural network, including the first layer between the input nodes and hidden nodes, and the second layer between hidden nodes and output nodes. The initial input is received by the input nodes and then used as the input for the hidden nodes after being weighted and summed. Furthermore, the input for the hidden node is nonlinearly transformed by the neuron and then presented at the output. The key to implementing neural computing in the neural network is the dot product of the vector and the matrix [1].

According to the different neuron models used, neural networks can be roughly divided into artificial neural networks (ANNs) and SNNs. ANNs are the main models currently used in deep learning, which mainly simulate the topological interconnection structure in biological neural networks and use a nonlinear function to represent neurons to achieve the cognitive function of biological neural networks to a certain extent. Fig. 1 (b) shows how ANNs work. In ANNs, the nonlinear function serves as the basic computing unit transforming the input **x** to the corresponding analog output.

In SNNs, spiking neurons are used as basic computing units [29]. SNNs process information using spikes, or action potentials, which are unique neuron outputs with a fixed shape and amplitude, and sometimes are referred to as binary events that can be 0 or 1. Similar to biological neurons, neurons in SNNs are activated only when they receive or emit spikes, thus SNNs are more energy-efficient. The schematic diagram of SNNs is shown in Fig. 1 (c). Compared with ANNs, SNNs, introducing timing parameters into the calculation process, have the advantages of asynchronous communications, sparse coding, and event-driven processing of information [30]. Besides, SNNs are the fundamental platforms for performing neuromorphic computing.

2.2. Neuron models

Different neuron models have been proposed to describe the process of how the neurons generate action potentials on the circuit or mathematically. One is the biophysical model, whose goal is to emulate the electrophysiological state of the neuron membrane (for example, the Hodgkin-Huxley (H-H) model [31]). The other is the phenomenological model, whose goal is to use simple mathematical abstractions (for example, the leaky integrate-and-fire (LIF) model [32]) to capture the input-output behavior of neurons. The H-H neuron and LIF models are the most widely used and studied in circuit implementations and algorithm applications. Fig. 2 (a) shows the schematic of the H-H neuron circuit model. In this model, two variable resistors with different turn-on voltages (R_{Na} and R_K) represent the Na^+ and K^+ channels of biological neurons, respectively. Meanwhile, a capacitor represents the membrane, and a fixed resistance R_L represents the leakage path of the membrane. After receiving the input stimuli, the membrane potential lifts up and activates the two

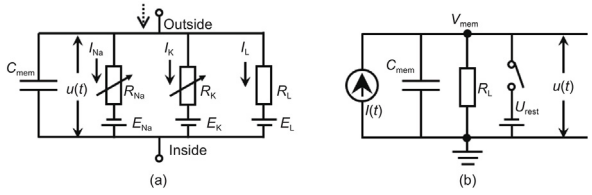


Fig. 2. Schematic diagrams of (a) H-H neuron circuit model and (b) LIF neuron circuit model.

voltage-gated ion channels to the open state in sequence when the membrane potential surpasses a threshold value, resulting in an action potential. Compared with the H-H model, the LIF neuron model is relatively simple, as shown in Fig. 2 (b). In this model, a capacitor is used as a membrane to integrate the input signal, R_L is used as the resistance of the leakage loop, and the threshold switch (or the variable resistance) serves as the ion channel.

2.3. Hardware implementation of neuromorphic computing

At present, the hardware implementation of neuromorphic computing mainly involves physical neural networks, which could be divided into two types: CMOS-based and non-CMOS-based. The neuromorphic computing technology based on emerging devices is in its infancy, and one of the most attractive directions is using memristors to build neuromorphic chips. In a narrow sense, neuromorphic chips also specifically refer to the hardware implementation of SNNs.

In the conventional CMOS process, neuron circuits and synaptic circuits are the bases for hardware implementation. For achieving complex brain-inspired interconnection, neuromorphic chips are usually implemented through a multi-level scheme of a horizontal and vertical cross matrix (X-bar), network on chip (NoC), and multi-core interconnections [33,34]. Many chips have been successfully developed based on this architecture, showing great application potential in areas, such as smart cities, real-time information processing for autonomous driving, and deep facial recognition. For example, IBM's TrueNorth [35], the representative digital chip with global asynchronous and local synchronous, Intel's Loihi [33], realizing online learning based on fin field-effect transistor (FinFET) technology, Stanford University's Neurogrid [36], a digital-analog hybrid programmable neuromorphic chip.

Compared with existing CMOS transistors, memristors have the advantages of simple structures, low power consumption, good scalability, rich dynamics, and easy three-dimensional integration, also in the Back-End-Of-Line (BEOL) of the standard CMOS fabrication process [37–39]. In view of the potential advantages of memristors in building neuromorphic chips, memristors have been considered to be ideal hardware units for building low-power, high-density neuromorphic chips, attracting widespread attention from academia and industry.

3. Application of threshold switching redox memristors

3.1. Different mechanisms in TS devices

Threshold switching memristors (TSMs) feature the ability to spontaneously switch from a low-impedance state to a high-impedance state without any additional voltage, which can greatly simplify the design and fabrication of neuron circuits. As mentioned above, TSM can be divided into three types according to their working mechanisms: IMT, metal ion threshold transition, or ovonic threshold switching (OTS) [40].

TSM based on IMT is commonly observed in NbO_x or VO_x material systems, a NbO_2 or VO_2 conductive channel with the characteristics of IMT is formed after the forming voltage is applied. IMT is closely related to the energy in the channel. An external voltage can cause the channel to change from a high-resistance insulating state at rest to a low-resistance metallic state. When the external voltage excitation is insufficient, the conductive channel will be broken and the device will spontaneously change from a low-resistance state (LRS) to a high-resistance state (HRS), showing a volatile characteristic (see Fig. 3 (a)).

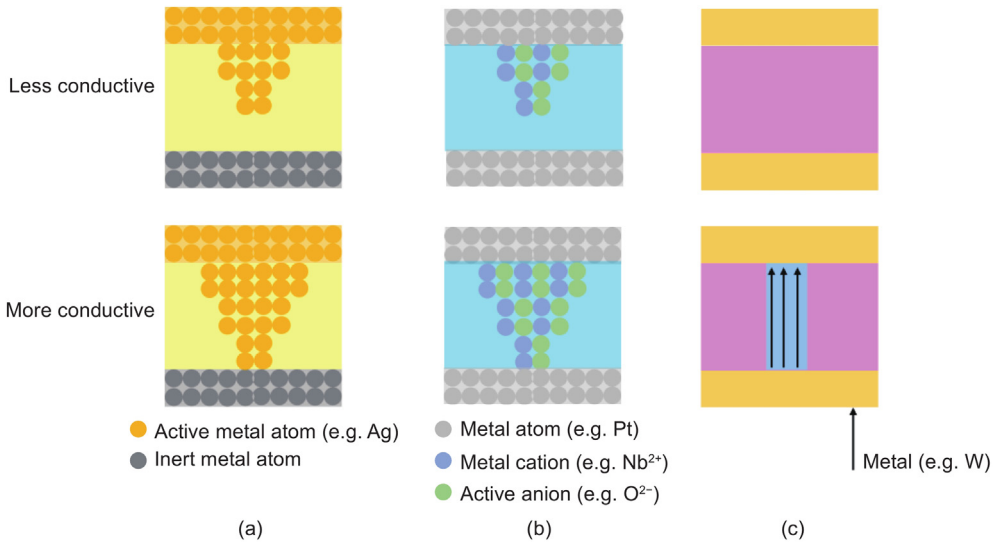


Fig. 3. Schematic presentation of three types of TSM operating in a less conductive or more conductive state, (a) TSM based on IMT, (b) TSM based on metal ion threshold transition, (c) TSM based on OTS.

TSM based on the metal ion threshold transition is characterized by the metal conductive channel formed due to redox and electromigration of metal cations. Taking the diffusion memristor of Ag filaments as an example, when the metal channel is formed, minimization of interfacial energy between the metal conductive path and the surrounding medium or the Thomson-Gibbs effect tends to break the conduction path spontaneously if no sufficient electrical excitation is applied (see Fig. 3 (b)).

TSM based on OTS realizes the switching operation by field-assisted tunneling. The S-based Ge alloy is an appealing OTS material. In

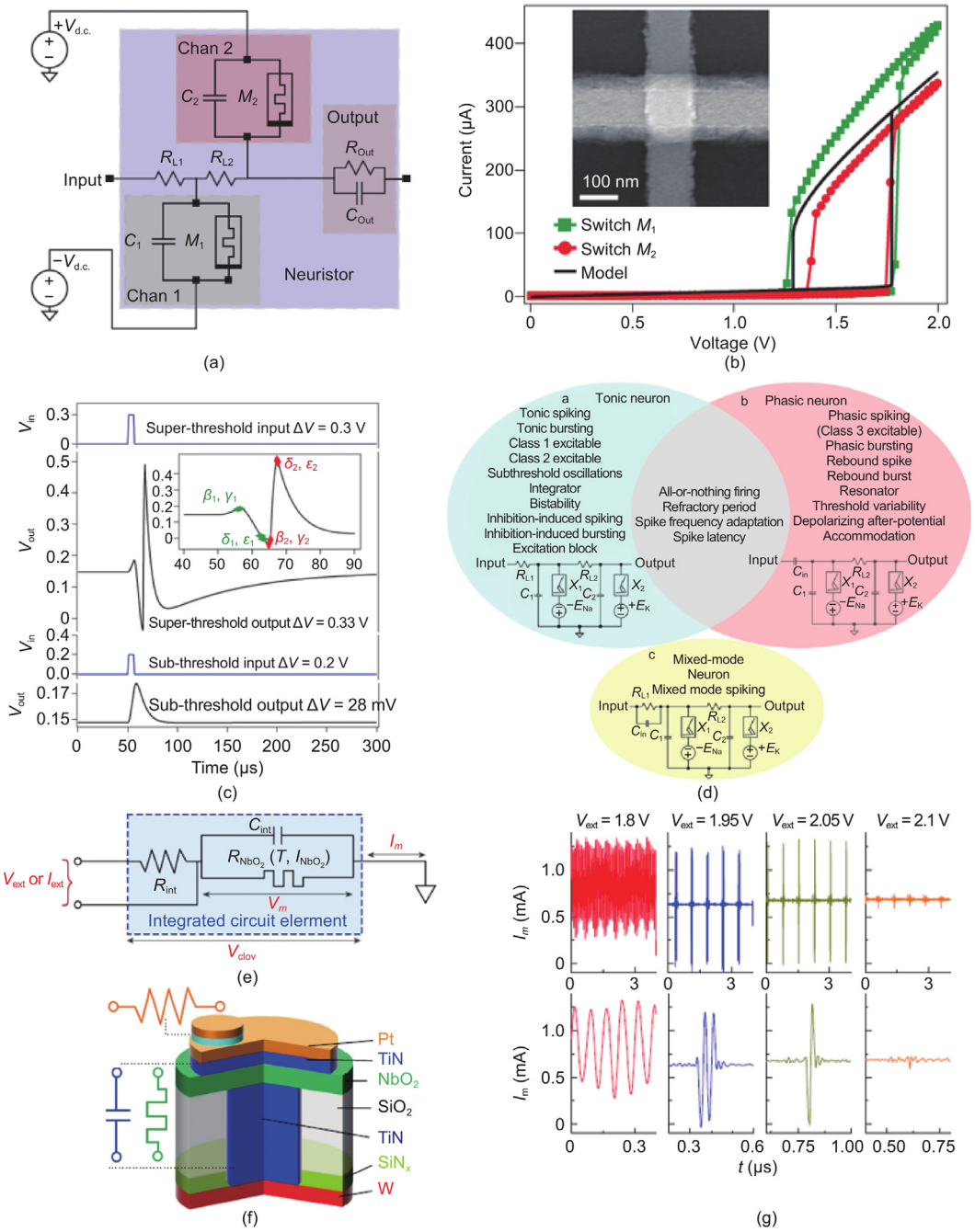


Fig. 4. Artificial neurons based on TSM with IMT characteristic: (a) H-H neuron circuit based on double Pt/Nb_2O_5/Pt memristors; (b) *I-V* characteristic of the proposed IMT-based neuristor; (c) schematic illustration of the all-or-nothing threshold discharge characteristics of the H-H neuron [46], Copyright 2013, Springer Nature; (d) three prototype neuron circuits and their demonstrated neuromorphic behaviors based on the VO_2 memristor: a) tonic excitatory neurons; b) phasic excitatory neurons; c) mixed-mode neurons [45], Copyright 2018, Springer Nature. Third-order nanocircuit elements based on the NbO_x memristor: (e) the integrated circuit element; (f) schematic diagram of the structure of the memristor; (g) temporal dynamics of the artificial neuron at different external voltage biases [47], Copyright 2020, Nature.

this work, TSM based on OTS is not in our main discussion considering that OTS is based on the concept of phase change memristors, not redox memristors (see Fig. 3 (c)).

3.2. Application in artificial neurons

Nowadays, CMOS devices have been widely reported to realize spiking neuron circuits [41,42]. However, due to the lack of dynamic characteristics similar to neurons, CMOS neuron circuits need dozens of transistors to realize neuron functions, resulting in great challenges in energy efficiency and scalability. LIF neuron circuits with relatively simple structures also need to be composed of a capacitor, reset circuits, and comparators. As an example, when SNNs have to interact with the external environment in real time, the time constants of the network have to match the ones of the real world. This typically results in the use of huge capacitors that can take up to 60% of the chip area [43].

Recently, artificial neurons based on threshold switching redox memristors have received wide attention due to their simple circuit designs. The NbO_x-based memristor, one of the redox memristors, featuring the negative differential resistance (NDR) behavior and abundant device physical dynamics, can serve as the basis of dynamic threshold switching with voltage sweeps [44], and be used to emulate biological neurons. In 2013, Pickett et al. reported a neuristor built using two nanoscale $Pt/Nb_2O_5/Pt$ memristors according to the H-H neuron circuit model [45]. Fig. 4 (a) presents the schematic of this neuristor. In this circuit, two NbO_2 memristors act as Na^+ ion channels and K^+ ion channels, respectively. Both channels consist of a memristor and a capacitance in parallel and are coupled by a load resistor. Fig. 4 (b) shows the *I-V* curve of this IMT memristor, the existence of the hysteresis loop is owing to the Mott transition. The IMT-based neuristor can realize the neuronal behaviors of threshold firing, the all-or-nothing action potential, lossless spike propagation, the refractory period, tonic firing, and rapid burst firing. As shown in Fig. 4 (c) [46], no complete action potentials generate when the input stimulus is relatively small (0.2 V), but a complete action potential is out to complete a discharge when the input stimulus is large enough (0.3 V). As far as we know, this work is pioneering work in the realization of spiking neuron circuits using memristors, laying the foundation for scalable and CMOS compatible neuromorphic circuits.

To further realize more neuron firing modes, Yi et al. optimized the H-H neuron circuit model and implemented 23 biological neuron firing modes based on volatile neuron devices [45], which more fully reflected the advanced nature of memristor-based neuron circuits. Fig. 4 (d) [45] shows the three prototype neuron circuits, and their experimental demonstrated neuromorphic behaviors based on this VO_2 active memristor. Different neuron firing modes are implemented by customizing the passive *R* and *C* elements with no need for varying VO_2 device parameters. This work greatly simplifies the design and fabrication of an integrated circuit.

Neuron circuits based on the H-H model have high requirements for device uniformity and parameter matching between circuits, increasing the difficulty of large-scale integration and applications. In the meantime, the LIF model has received extensive attention in system integration owing to its simple structure and low computational complexity. In the LIF neuron circuit, only one capacitor coupled with an IMT memristor is essential. The capacitor is responsible for integration, while the IMT memristor performs threshold judgment and generates a spike signal. Based on this, Gao et al. demonstrated a LIF neuron based on NbO_x memristors which are connected with a synapse (a load resistor) [48]. In this work, the oscillation frequency of the spiking neuron was proportional to the synaptic conductance, thus supporting the feasibility of integrating the weighted sum.

Considering the unique dynamics of TSM associated with Mott transitions, it is of great significance to fully exploit the dynamics of the device in neuronal circuits. In 2020, Kumar et al. further used the third-order dynamics of the NbO_x memristor, the parasitic capacitance of the device, and stacked integrated external resistors to achieve multiple neuron discharge modes in a single integrated

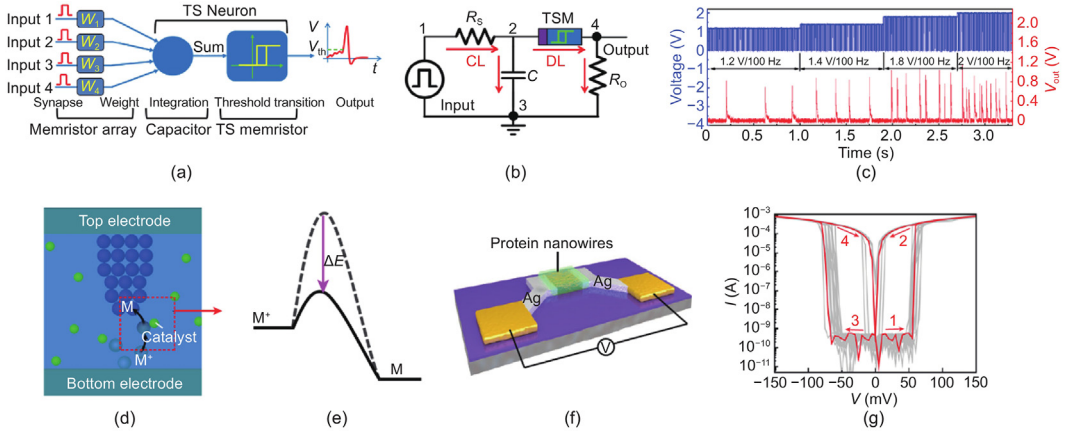


Fig. 5. Artificial neuron based on TSM with the metal ion threshold transition characteristic: (a) schematic diagram of the spiking neuron circuit with a TS memristor as the dynamic threshold switch; (b) schematic illustration of the proposed neuron circuit; (c) discharge characteristics of the neuron under different input pulse amplitudes [50], Copyright 2017, IEEE; (d) schematic of the memristor with the catalyst inserted in the insulator; (e) illustration of the decreased reduction overpotential caused by the catalyst; (f) schematic of the diffusive memristor structure; (g) typical IV curve measured from the memristor, reproduced with permission [52], Copyright 2020, Springer Nature.

device, and verified the on-chip integration for the first time [47]. Fig. 4 (e) shows the integrated nanocircuit element, consisting of a NbO_2 volatile Mott memristor coupled with an internal parallel capacitor and an internal series resistor. Fig. 4 (f) illustrates the structure of the NbO_2 memristor. As shown in Fig. 4 (g) [47], self-sustained sinusoidal oscillation occurs when the bias below the hysteresis (v_{ext} = 1.8 V), and periodic two-spike bursting occurs when the bias within the hysteresis (v_{ext} = 1.95 V). This results in distinct dynamics appearing in the memristor under different voltages. This work provides a feasible solution for realizing high-density neuron circuits to construct an efficient brain-like system.

Except for the IMT-based TS memristors that can be used to build neuron circuits, the TS memristors with metal filaments are also promising candidates. Wang et al. created a LIF neuron with stochastic dynamics based on a diffusive Pt/SiO_xN_y:Ag/Pt memristor, where the migration of Ag is similar to actual neuron ion channels [49]. In addition, Zhang et al. demonstrated a novel LIF neuron based on Ag/SiO_2/Au TSM [50]. Fig. 5 (a) presents the schematic of the spiking neuron circuit. A memristor and an output resistance are connected together to complete the neuron, paralleled by a capacitor, as shown in Fig. 5 (b). Fig. 5 (c) shows the firing characteristic of this artificial neuron; with the increase of the input pulse amplitude, the discharge frequency increases obviously. This circuit achieved four fundamental neuron functions: The all-or-nothing spiking of an action potential, threshold-driven spiking, a refractory period, and strength-modulated frequency response. Furthermore, the feasibility of the neural network based on this TSM neuron in digital recognition was verified by system simulation. In addition, based on their Ag/SiO_2/Au TS memristors, Zhang et al. further constructed a hybrid memristor-CMOS neuron, which has the basic LIF neuron function and enables the *in-situ* tuning of the connected synapses [51]. This work proposed a novel way to realize the *in-situ* learning for future neuromorphic computing systems.

However, the switching voltages of the devices we mentioned above are still much higher than the amplitude in biological counterparts. To further decrease the switching voltages to the level of biological neurons (~100 mV), Fu et al. then constructed a new type of diffusive Ag memristor utilizing the protein nanowires as the catalyst [52]. The introduced catalyst facilitates metal ion reduction, as shown in Fig. 5 (d). The lower reduction overpotential leads to a decreased switching voltage (Fig. 5 (e)). Fig. 5 (f) shows the structure of the memristor, an insulating substrate (Si/SiO_2) coupled with a pair of silver electrodes. As shown in Fig. 5 (g), in the positive bias, the switching voltage turning the device from HRS to LRS is 60 ± 4 mV. A symmetric behavior happens in the negative bias. The protein nanowires distributed in the insulating substrate not only serve as catalysts to promote cathodic Ag^+ reduction, but also provide this memristor with excellent biocompatibility.

In summary, neuron circuits realized by memristors are mainly based on the H-H neuron circuit model and the LIF neuron circuit model. Using TS memristors to realize neurons facilitates the construction of compact neuromorphic machines. TS memristors based on IMT and TS memristors based on conductive metal filaments have been reported to construct the neuron circuits. Besides, the hybrid memristor-CMOS neuron shows possibilities for implementing neuromorphic computing systems with the ability of *in-situ* learning. To clearly present the current research state of the TS-based neurons, we summarize representative works on artificial neurons with emerging volatile memristors in terms of the device type, working mechanism, device structure, threshold voltage, and neuron model (see Table 1).

3.3. Application in SNNs

The construction of neuron circuits is the foundation of the implementation of neural networks, while the verification of neurons in neural networks is necessary to promote the application of novel neurons. For the past few years, various works have been performed on building SNN-based hardware platforms with memristors. Strukov et al. constructed passive memristor-based SNN consisting of 20 × 20 integrated memristive synapses connected with a spiking neuron composed of CMOS circuits and an external waveform generator [53]. Coincidence detection, one representative task for SNN, was realized in their work.

Due to the complex structure of CMOS neuron circuits, which is not conducive to large-scale integration, the use of memristor neurons to build neuromorphic systems has gradually become a research hotspot. Fig. 6 shows some hardware implementations of SNNs [24,47,49,54–58].

In 2018, Wang et al. used memristor neurons and synapses to build 8 × 8 full memristive SNN for the first time in the world [49]. The schematic diagram of its hardware structure is shown in Fig. 6 (a). Based on this system, convolutional inference operations are validated and unsupervised learning of input patterns is realized. Considering the advantages of lower static power and better emulation of neural functionalities of capacitive neural networks, Wang et al. implemented 4 × 4 capacitive ANN with passive synapses, and verified the Hebbian learning rule and the inference results of the network [54], as shown in Fig. 6 (b). To give full play to the advantages of SNN in power consumption, Zhang et al. demonstrated fully memristive temporal coding (TC) SNN, composed of a NbO_x memristor-based neuron circuit and a 64 × 64 1T1R TaO_x/HfO_x memristor-based RRAM array, which was served as the synapses [55], as shown in Fig. 6

Table 1
Brief summary of some representative artificial neurons based on volatile memristors.

Type	Mechanism	Device structure	Threshold voltage (V)	Neuron model	Ref.
TSM	IMT	Pt/Nb_2O_5/Pt	1.75	H-H	[45]
TSM	IMT	Pt/VO_2/Pt	1.22	H-H	[45]
TSM	IMT	Pt/NbO_x/Pt	1.9	LIF	[47]
TSM	IMT	Pt/TiN/NbO_2/TiN/W	0.5	LIF	[48]
TSM	Metal ion	Pt/SiO_xN_y:Ag/Pt	1.4	LIF	[49]
TSM	Metal ion	Ag/SiO_2/Au	1.0	LIF	[50]
TSM	Metal ion	Ag/SiO_2/Ag (nanowires)	0.5	LIF	[52]

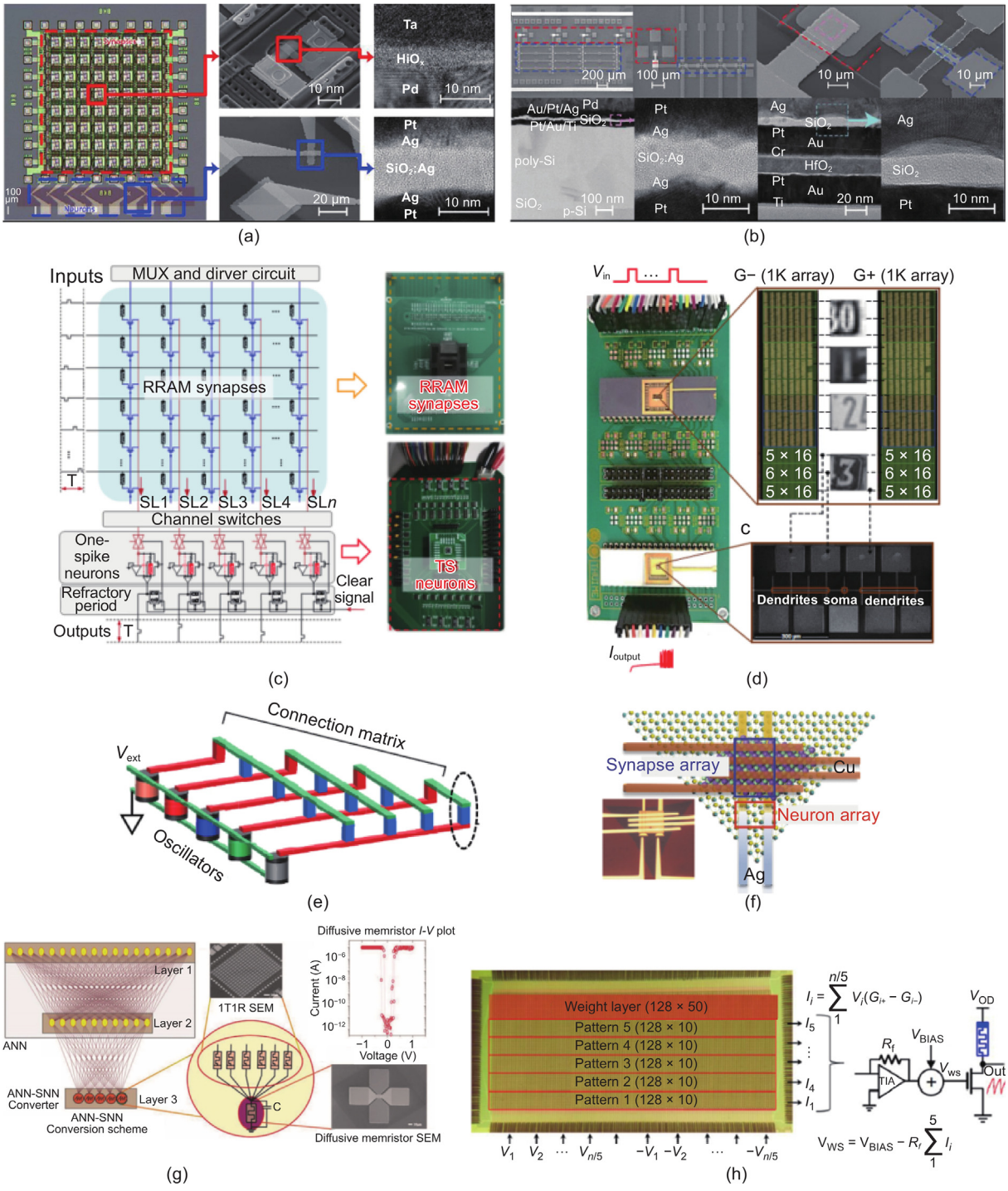


Fig. 6. Hardware implementations of SNNs: (a) hardware diagram of full memristive SNN [49], Copyright 2018, Springer Nature; (b) hardware diagram of capacitive ANNs [54], Copyright 2018, Springer Nature; (c) schematic of constructed fully memristive TC SNNs and the hardware implementation [55], Copyright 2020, IEEE; (d) hardware diagram of the neural network and the synapse array [56], Copyright 2020, Springer Nature; (e) schematic illustration of the experimental system with the neuromorphic oscillators and the connection matrix formed by a crossbar array of pseudo-memcapacitors [47], Copyright 2020, Nature; (f) schematic illustration of the fully memristive neural network [24], Copyright 2020, Advanced Electronic Materials; (g) schematic of ANN-SNN conversion [57], Copyright 2019, Advanced Electronic Materials; (h) hardware schematic diagram of the conversion-based SNN [58], Copyright 2019, IEEE.

(c). Compared with the general rate coding (RC) SNN, this TC SNN shows a significant advantage in latency, power, and lifetime.

Most of current ANNs simplify neurons to simple point models and simplify their calculation function to integrate-and-fire, ignoring the information processing function of dendrites. As a result, ANNs still lag far behind biological neural networks in the flexibility, robustness, and power consumption of complex tasks. Based on this, Li et al. demonstrated a two-terminal memristor-based neural network composed of a HfO_x-based non-volatile memristor as the artificial synapse, a TaO_x/AlO_δ-based dynamic memristor as the artificial dendrite, and a NbO_x-based Mott memristor as the artificial soma [56]. The optical images of the neural network and the synapse array are shown in Fig. 6 (d). This work represents an important step towards more complete, energy-efficient, and accurate neural networks. Generating neuromorphic action potentials in a circuit element theoretically requires at least third-order complexity, whereas most neurons are constructed of first-order or second-order neuromorphic elements. Considering that, Kumar et al. constructed a NbO_x memristor with third-order dynamics and further demonstrated neural networks of third-order elements with no transistors [47]. Fig. 6 (e) shows the experimental system with the neuromorphic oscillators and the connection matrix formed by a crossbar array of pseudo-memcapacitors. This work guides compact and highly functional neural networks.

Compared with traditional neurons based on oxide memristors, artificial neurons based on 2D materials possess lower energy consumption, similar to biological neurons. Hao et al. constructed a 2-dimensional (2D) LIF neuron whose mechanism is attributed to the rapid diffusion and migration of Ag in the MoS_2 lattice under the external field, and further fabricated full memristive ANN by integrating 2D neurons and Cu/GeTe based synapses [24]. Fig. 6 (f) illustrates the fully 2D neural network consisting of a nonvolatile synapse array and 2D MoS_2-based neurons. This work fills in the gap of neural networks fabricated with 2D materials.

Since most of the commonly used data sets are for ANNs, the analog quantity in the data set needs to be converted into pulse trains of corresponding frequencies, when used for SNNs [59], resulting in the loss of accuracy. To alleviate the predicament of applying SNNs to process data, converting ANNs to SNNs by adjusting the weights and neuron parameters is an effective method [60–62]. Conversion method-based SNNs can have both the high energy efficiency of SNNs and the high precision of ANNs [63]. Based on this, Midya et al.

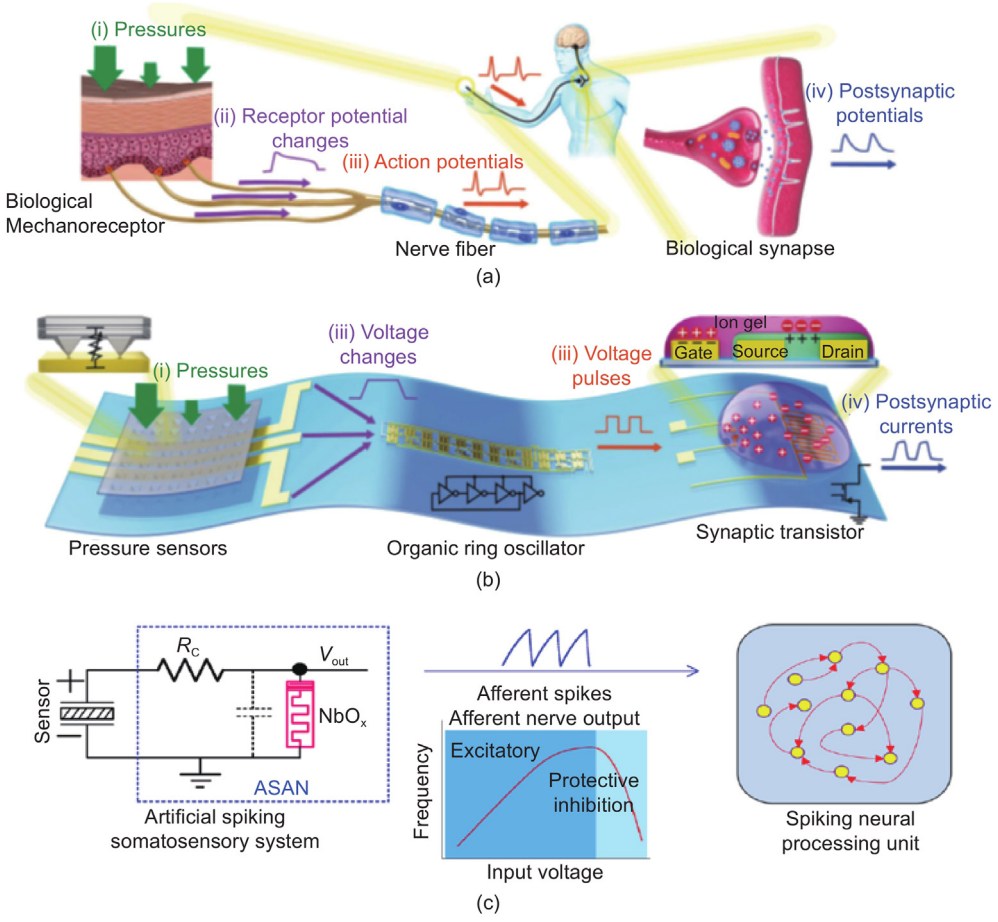


Fig. 7. Schematics of the sensing application based on memristor-based artificial neurons: (a) biological sensing system controlled by pressures, composed of biological mechanoreceptors, a nerve fiber, and a biological synapse; (b) artificial ORO-based bio-inspired efferent nerve, consisting of pressure sensors, an organic ring oscillator, and a synaptic transistor [69], Copyright 2018, Spring Science; (c) schematic of the artificial spiking somatosensory system composed of the NbO_x memristor-based artificial spiking efferent nerve, reproduced with permission [71], Copyright 2020, Spring Nature.

illustrated an ANN-SNN converter using a diffusive memristor and a parallel capacitor [57]. Fig. 6 (g) is the schematic of ANN-SNN conversion. Layer 1 (the input layer) and Layer 2 (the hidden layer) operate like traditional ANN, while Layer 3 (the output layer) transforms the weight activation products into the spiking frequency. Moreover, Zhang et al. experimentally demonstrated conversion-based SNN composed of memristive synaptic weight elements and 1T1R Mott neurons [58]. The Mott neuron was formed by connecting the NbO_x device in series to a transistor, serving as the rectified linear unit (ReLU) in the network. The schematic of the 1T1R neuron circuit and its equivalent circuit is shown in Fig. 6 (h). Practically, the neuron circuit had no external capacitors, which greatly improved the integration density of the neuron circuit. Furthermore, a single-layer fully connected forward neural network (320×10) was implemented for the recognition of the handwritten digits in the modified National Institute of Standard and Technology (MNIST) dataset, obtaining recognition accuracy of up to 85.7%, close to the recognition rate of ReLU software neurons. Moreover, due to the gating effect of the transistor, the X-bar integrated structure of the neuron was proposed for higher system integration.

To summarize this section, implementing SNNs with emerging electronic devices is promising, but more efforts are still needed to improve the efficiency of SNNs and realize large-scale integrated applications. Introducing dendrite functions into neural networks reduces the dynamic power consumption and improves the accuracy of complex information processing. In order to solve the problem of the immaturity of the SNNs training algorithm, the concept of conversion-based SNNs is proposed, showing a new technical approach for the construction of efficient neuromorphic chips in the future.

3.4. Application in artificial afferent nerves

As mentioned above, memristor-based artificial neurons have been actively studied and explored to build efficient SNNs. However, the signals collected from surroundings are usually in analog forms, which cannot be processed directly in SNNs [64–66]. In biological nervous systems, the afferent nerve converts the signals received from sensors into spikes and transmits them to central nervous systems for further processing [67]. Therefore, to realize an intelligent processing system that integrates sensing, storage, and calculation, it is necessary to construct a special unit to mimic the afferent nerve in biological systems.

So far, significant progress has been made in realizing artificial afferent nerves using phase-locked loop circuits. Kim et al. reported a flexible artificial afferent nerve, consisting of resistive pressure sensors, organic ring oscillators (OROs), and a synaptic transistor [68]. The frequency and amplitude of the spikes output by oscillators were positively correlated with the pressure intensity from pyramid-structured pressure sensors. The synaptic transistor, using ion gel as the gate dielectric, can integrate signals from multiple oscillators. Furthermore, this artificial afferent nerve was designed to fabricate a hybrid monosynaptic reflex arc by connecting with biological efferent nerves to control the movement of the cockroach's legs. Fig. 7 (a) illustrates the biological sensing system, composed of the biological mechanoreceptors, a nerve fiber, and a biological synapse. Fig. 7 **(b)** shows the artificial efferent nerve, consisting of the resistive pressure sensors, an organic ring oscillator, and a synaptic transistor [69].

However, similar to the CMOS neuron circuit, the development of the afferent nerve circuit based on CMOS devices is limited by the complexity of the circuit and the physical bottleneck of CMOS devices. To alleviate this limitation, Zhang et al. constructed a highly compact artificial spiking afferent nerve (ASAN) based on a specially designed NbO_x memristor for the first time [70]. The most important component in ASAN is the NbO_x oscillator composed of the NbO_x memristor and a resistor, whose output frequency presented a quasi-linear relationship with the input voltage under normal stimuli and decreased under the excessively strong stimuli. The frequency-voltage curve of ASAN is shown in Fig. 7 (c) [71], similar to the action potential characteristic of the afferent nerve in the biological somatosensory system shown in Fig. 7 (a). Various types of input spikes, such as rectangular, triangular, and sinusoidal pulses, were applied to ASAN to study the dynamic spiking behavior systematically. Furthermore, an artificial spiking mechanoreceptor system (ASMS) based on ASAN connected with a piezoelectric device was constructed, featuring no need of an external power source. In addition, ASAN can be readily extended to process sensory signals from other sensors, such as smell, taste, sight, hearing, temperature, magnetic field, and humidity.

Considering the limit in emulation and implementation of learning and memorizing capabilities of the non-plastic artificial nerve, Tan et al. designed an optoelectronic spiking afferent nerve, featuring neural coding, perceptual learning, and memorizing capabilities [65]. MXene-based sensors and light-emitting diodes coupled with analog-to-digital circuits were responsible for converting the pressure information to optical signals. This afferent nerve could recognize the Morse code, braille, and object movement, providing a novel approach towards e-skin, neurorobotics, and so on.

In conclusion, to build a complete intelligent processing system, an artificial afferent nerve is an indispensable component. Owing to the inherent dynamic characteristics of the TS memristors, the constructed artificial afferent nerves have the advantages of a simple circuit and high integration and can be further used to construct a variety of sensory systems.

4. Conclusion and outlook

In this review, recent progress in the application of volatile redox memristors in SNNs has been reviewed. We started this review by introducing the categories of TS memristors and stating the neural network that is divided into ANNs and SNNs. Among them, event-driven SNNs had received our focus due to their higher biological rationality and higher energy efficiency. Therefore, we introduced the application of non-CMOS-based devices represented by memristors in SNNs, including the construction of spiking neurons, the hardware implementation of SNNs, and the innovation of artificial spiking afferent nerves. Due to the simple structure, low energy consumption, and rich inherent dynamics of TS memristors, the neuromorphic chips based on memristors can perfectly solve the problems of complicated circuit design and limited integration density on the traditional CMOS technology. However, as the research on neuromorphic chips based on memristors is just in its infancy, there are still many challenges that need to be resolved:

a) For memristor-based neuron circuits, the functions that neurons can achieve are relatively simple. More systematic and in-depth research is needed, from the device function verification to the optimization design of peripheral auxiliary circuits using memristor neurons for demonstrations on a certain scale. In addition, reliability, large array integration, and variability of memristors limit their extensive use (up to now) [69,71]. The uniformity of device-level neurons due to the randomness of filament formation in redox memristors and the integration of crossover arrays and neuron circuits remain the main challenges for current memristor-based neuromorphic computing chips.
b) Efficient SNN algorithms are the inner soul of neuromorphic chips to realize intelligence, but the existing algorithms are not mature enough and are not proposed for the memristor-based hardware platform.
c) The memristor-based sensing system needs to be combined with the deep neuromorphic information processing system to build an artificial intelligence system that integrates consciousness, memory, and computation, which truly resembles the human brain.
d) Utilizing the advantages of easy three-dimensional integration of memristor devices in BEOL of the standard CMOS fabrication process to achieve high-density 3D neuromorphic chips is the goal to be pursued in the future.

Although most current memristor-based neuromorphic computing research is still in the laboratory stage and has much room for improvement, its development has been unstoppable. We believe that with the emergence of various new memristors and the improvement of the integration of memristors, neuromorphic computing based on memristors can feature dominant applications in certain fields over the traditional von Neumann computing system in the future.

Declaration of competing interest

No potential conflict of interest.

Acknowledgment

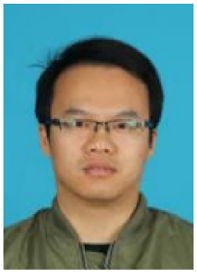
This work was supported in part by the Ministry of Science and Technology of China under Grant No. 2017YFA0206102, and in part by the National Natural Science Foundation of China under Grant No. 61922083, and the Strategic Priority Research Program of Chinese Academy of Sciences under Grant No. XDB44000000; the European Union's Horizon 2020 Research and Innovation Program with Grant Agreement No. 824164; the German Research Foundation Projects MemCrypto under Grant No. GZ: DU 1896/2-1 and MemDPU under Grant No. GZ: DU 1896/3-1.

References

[1] Y. LeCun, Y. Bengio, G. Hinton, Deep learning, Nature 521 (7553) (May 2015) 436–444.
[2] W. Rawat, Z.-H. Wang, Deep convolutional neural networks for image classification: a comprehensive review, Neural Comput. 29 (9) (Sept. 2017) 2352–2449.
[3] T. Young, D. Hazarika, S. Poria, E. Cambria, Recent trends in deep learning based natural language processing, IEEE Comput. Intell. Mag. 13 (3) (Aug. 2018) 55–75.
[4] D. Silver, A. Huang, C.J. Maddison, et al., Mastering the game of go with deep neural networks and tree search, Nature 529 (7587) (Jan. 2016) 484–489.
[5] O. Vinyals, I. Babuschkin, W.M. Czarnecki, et al., Grandmaster level in StarCraft II using multi-agent reinforcement learning, Nature 575 (7782) (Oct. 2019) 350–354.
[6] Q.-F. Xia, J.-J. Yang, Memristive crossbar arrays for brain-inspired computing, Nat. Mater. 18 (4) (Mar. 2019) 309–323.
[7] G.W. Burr, P. Narayanan, R.M. Shelby, et al., Large-scale neural networks implemented with non-volatile memory as the synaptic weight element: comparative performance analysis (accuracy, speed, and power), in: Proc. of IEEE Intl. Electron Devices Meeting, 2015, pp. 4.4.1–4.4.4. Washington.
[8] N.P. Jouppi, C. Young, N. Patil, et al., In-datacenter performance analysis of a tensor processing unit, in: Proc. Of ACM/IEEE the 44th Annual Intl. Symposium on Computer Architecture, 2017, pp. 1–12. Toronto.
[9] S.-M. Yu, Neuro-inspired computing with emerging nonvolatile memory, Proc. IEEE 106 (2) (Feb. 2018) 260–285.
[10] C. Li, M. Hu, Y.-N. Li, et al., Analogue signal and image processing with large memristor crossbars, Nat. Electron. 1 (1) (Jan. 2018) 52–59.
[11] Z. Sun, G. Pedretti, A. Bricalli, D. Ielmini, One-step regression and classification with cross-point resistive memory arrays, Sci. Adv. 6 (5) (Jan. 2020) 1–7, eaay2378.
[12] L. Chua, Memristor-the missing circuit element, IEEE Trans. Circ. Theor. 18 (5) (Sept. 1971) 507–519.
[13] D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, The missing memristor found, Nature 453 (7191) (May 2008) 80–83.
[14] Z.-R. Wang, H.-Q. Wu, G.W. Burr, et al., Resistive switching materials for information processing, Nat. Rev. Mater. 5 (3) (Jan. 2020) 173–195.
[15] M.J. Lee, C.B. Lee, D. Lee, et al., A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structures, Nat. Mater. 10 (8) (Jul. 2011) 625–630.
[16] W. Zhang, R. Mazzarello, M. Wuttig, E. Ma, Designing crystallization in phase-change materials for universal memory and neuro-inspired computing, Nat. Rev. Mater. 4 (3) (Jan. 2019) 150–168.
[17] J. Jiang, Z.-L. Bai, Z.-H. Chen, et al., Temporary formation of highly conducting domain walls for non-destructive read-out of ferroelectric domain-wall resistance switching memories, Nat. Mater. 17 (1) (Jan. 2018) 49–56.
[18] F.D. Natterer, K. Yang, W. Paul, et al., Reading and writing single-atom magnets, Nature 543 (7644) (Mar. 2017) 226–228.
[19] B.J. Choi, A.C. Torrezan, J.P. Strachan, et al., High-speed and low-energy nitride memristors, Adv. Funct. Mater. 26 (29) (2016) 5290–5296, Aug.
[20] S. Pi, C. Li, H. Jiang, et al., Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension, Nat. Nanotechnol. 14 (1) (Jan. 2019) 35–39.
[21] S. Deswal, A. Kumar, A. Kumar, NbO_x based memristor as artificial synapse emulating short term plasticity, AIP Adv. 9 (9) (Sept. 2019), 095022, 1-5.
[22] J. Lin, Annadi, S. Sonde, et al., Low-voltage artificial neuron using feedback engineered insulator-to-metal-transition devices, in: IEEE Intl. Electron Devices Meeting, 2016, pp. 34.5.1–34.5.4. San Francisco.
[23] Z. Wang, S. Joshi, S.E. Savel'ev, et al., Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing, Nat. Mater. 16 (1) (Jan. 2017) 101–108.
[24] S. Hao, X.-L. Ji, S. Zhong, et al., A monolayer leaky integrate-and-fire neuron for 2D memristive neuromorphic networks, Adv. Electron. Mater. 6 (4) (Apr. 2020), 1901335, 1-8.
[25] M. Farronato, M. Melegari, S. Ricci, S. Hashemkhani, A. Bricalli, D. Ielmini, Memtransistor devices based on MoS_2 multilayers with volatile switching due to Ag cation migration, Adv. Electron. Mater. 8 (8) (Aug. 2022), 2101161, 1-7.

[26] J.H. Yoon, S.-J. Song, I.H. Yoo, et al., Highly uniform, electroforming-free, and self-rectifying resistive memory in the Pt/Ta_2O_5/HfO_{2-x}/TiN structure, Adv. Funct. Mater. 24 (32) (2014) 5086–5095, Aug.
[27] D. Purves, G.J. Augustine, D. Fitzpatrick, et al., Neuroscience, third ed., Sinauer Associates Inc., Sunderland, 2004.
[28] C. Mead, Neuromorphic electronic systems, Proc. IEEE 78 (10) (1990) 1629–1636, Oct.
[29] W. Maass, Networks of spiking neurons: the third generation of neural network models, Neural Network. 10 (9) (Dec. 1997) 1659–1671.
[30] M. Pfeiffer, T. Pfeil, Deep learning with spiking neurons: opportunities and challenges, Front. Neurosci. 12 (Oct. 2018), 774:1-18.
[31] A.L. Hodgkin, A.F. Huxley, A quantitative description of membrane current and its application to conduction and excitation in nerve, J. Physiol. 117 (4) (Aug. 1952) 500–544.
[32] E.M. Izhikevich, Which model to use for cortical spiking neurons, IEEE Trans. Neural Network. 15 (4) (Sept. 2004) 1063–1070.
[33] M. Davies, N. Srinivasa, T.-H. Lin, et al., "Loihi: a neuromorphic manycore processor with on-chip learning," IEEE Micro, vol. 38, no. 1, pp. 82-99, Jan.-Feb. 2018.
[34] N. Imam, T.A. Cleland, Rapid online learning and robust recall in a neuromorphic olfactory circuit, Nat. Mach. Intell. 2 (3) (Mar. 2020) 181–191.
[35] P.A. Merolla, J.V. Arthur, R. Alvarez-Icaza, et al., A million spiking-neuron integrated circuit with a scalable communication network and interface, Science 345 (6197) (Aug. 2014) 668–673.
[36] B.V. Benjamin, P.-R. Gao, E. Mcquinn, et al., Neurogrid: a mixed-analog-digital multichip system for large-scale neural simulations, Proc. IEEE 102 (5) (May 2014) 699–716.
[37] M.A. Zidan, J.P. Strachan, W.-D. Lu, The future of electronics based on memristive systems, Nat. Electron. 1 (1) (Jan. 2018) 22–29.
[38] J.-J. Yang, D.B. Strukov, D.R. Stewart, Memristive devices for computing, Nat. Nanotechnol. 8 (1) (Jan. 2013) 13–24.
[39] S. Jain, A. Ankit, I. Chakraborty, et al., "Neural network accelerator design with resistive crossbars: opportunities and challenges," IBM J. Res. Dev., vol. 63, no. 6, pp. 10:1-13, Nov.-Dec. 2019.
[40] H. Lee, S.W. Cho, S.J. Kim, et al., Three-terminal ovonic threshold switch (3T-OTS) with tunable threshold voltage for versatile artificial sensory neurons, Nano Lett. 22 (2) (Jan. 2022) 733–739.
[41] M. Mahowald, R. Douglas, A silicon neuron, Nature 354 (6354) (Dec. 1991) 515–518.
[42] M.E. Beck, A. Shylendra, V.K. Sangwan, et al., Spiking neurons from tunable Gaussian heterojunction transistors, Nat. Commun. 11 (1) (Mar. 2020) 1565, 1-8.
[43] E. Covi, E. Donati, X.-P. Liang, et al., Adaptive extreme edge computing for wearable devices, Front. Neurosci. 15 (May 2021), 611300, 1-27.
[44] Q. Luo, X.-M. Zhang, J. Yu, et al., Memory switching and threshold switching in a 3D nanoscaled NbO_x system, IEEE Electron. Device Lett. 40 (5) (May 2019) 718–721.
[45] W. Yi, K.K. Tsang, S.K. Lam, X.-W. Bai, J.A. Crowell, E.A. Flores, Biological plausibility and stochasticity in scalable VO_2 active memristor neurons, Nat. Commun. 9 (Nov. 2018) 4661, 1-10.
[46] M.D. Pickett, G. Medeiros-Ribeiro, R.S. Williams, A scalable neuristor built with Mott memristors, Nat. Mater. 12 (2) (Feb. 2013) 114–117.
[47] S. Kumar, R.S. Williams, Z.-W. Wang, Third-order nanocircuit elements for neuromorphic engineering, Nature 585 (7826) (Sept. 2020) 518–523.
[48] L.-G. Gao, P.-Y. Chen, S.-M. Yu, NbO_x based oscillation neuron for neuromorphic computing, Appl. Phys. Lett. 111 (10) (Sept. 2017), 103503, 1-4.
[49] Z.-R. Wang, S. Joshi, S. Savel'ev, et al., Fully memristive neural networks for pattern classification with unsupervised learning, Nat. Electron. 1 (2) (Feb. 2018) 137–145.
[50] X.-M. Zhang, W. Wang, Q. Liu, et al., An artificial neuron based on a threshold switching memristor, IEEE Electron. Device Lett. 39 (2) (Feb. 2018) 308–311.
[51] X.-M. Zhang, J. Lu, Z.-R. Wang, et al., Hybrid memristor-CMOS neurons for *in-situ* learning in fully hardware memristive spiking neural networks, Sci. Bull. 66 (16) (2021) 1624–1633, Aug.
[52] T.-D. Fu, X.-M. Liu, H.-Y. Gao, et al., Bioinspired bio-voltage memristors, Nat. Commun. 11 (1) (Apr. 2020) 1861, 1-10.
[53] M. Prezioso, M.R. Mahmoodi, F.M. Bayat, et al., Spike-timing-dependent plasticity learning of coincidence detection with passively integrated memristive circuits, Nat. Commun. 9 (Dec. 2018) 5311, 1-8.
[54] Z.-R. Wang, M.-Y. Rao, J.W. Han, et al., Capacitive neural network with neuro-transistors, Nat. Commun. 9 (Aug. 2018), 3208:1-10.
[55] X.-M. Zhang, Z.-H. Wu, J.-K. Lu, et al., Fully Memristive SNNs with Temporal Coding for Fast and Low-Power Edge Computing, Proc. of IEEE Intl. Electron Devices Meeting, San Francisco, 2020, pp. 29.6.1–29.6.4.
[56] X.-Y. Li, J.-S. Tang, Q.-T. Zhang, et al., Power-efficient neural network with artificial dendrites, Nat. Nanotechnol. 15 (9) (Jun. 2020) 776–782.
[57] R. Midya, Z.-R. Wang, S. Asapu, et al., Artificial neural network (ANN) to spiking neural network (SNN) converters based on diffusive memristors, Adv. Electron. Mater. 5 (9) (Sept. 2019), 1900060, 1-14.
[58] X.-M. Zhang, Z.-R. Wang, W.-H. Song, et al., Experimental Demonstration of Conversion-Based SNNs with 1T1R Mott Neurons for Neuromorphic Inference, Proc. of IEEE Intl. Electron Devices Meeting, San Francisco, 2019, pp. 6.7.1–6.7.4.
[59] P.U. Diehl, M. Cook, Unsupervised learning of digit recognition using spike-timing-dependent plasticity, Front. Comput. Neurosci. 9 (Aug. 2015), 99:1-9.
[60] B. Rueckauer, I.A. Lungu, Y.-H. Hu, M. Pfeiffer, S.-C. Liu, Conversion of continuous-valued deep networks to efficient event-driven networks for image classification, Front. Neurosci. 11 (Dec. 2017), 682:1-12.
[61] J.A. Pérez-Carrasco, B. Zhao, C. Serrano, et al., Mapping from frame-driven to frame-free event-driven vision systems by low-rate rate coding and coincidence processing-application to feedforward ConvNets, IEEE Trans. Pattern Anal. Mach. Intell. 35 (11) (2013) 2706–2719, Nov.
[62] J. Pei, L. Deng, S. Song, et al., Towards artificial general intelligence with hybrid Tianjic chip architecture, Nature 572 (7767) (Jul. 2019) 106–111.
[63] A. Sengupta, Y.-T. Ye, R. Wang, C. Liu, K. Roy, Going deeper in spiking neural networks: VGG and residual architectures, Front. Neurosci. 13 (Mar. 2019), 95:1-10.
[64] M.M. Shulaker, G. Hills, R.S. Park, et al., Three-dimensional integration of nanotechnologies for computing and data storage on a single chip, Nature 547 (7661) (Jul. 2017) 74–78.
[65] H.-W. Tan, Q.-Z. Tao, I. Pande, et al., Tactile sensory coding and learning with bio-inspired optoelectronic spiking afferent nerves, Nat. Commun. 11 (Mar. 2020), 1369:1-9.
[66] Y.H. Jung, B. Park, J.U. Kim, T.I. Kim, Bioinspired electronics for artificial sensory systems, Adv. Mater. 31 (34) (Aug. 2019), 1803637, 1-22.
[67] P.D. Wall, M. Gutnick, Properties of afferent nerve impulses originating from a neuroma, Nature 248 (5451) (Apr. 1974) 740–743.
[68] Y. Kim, A. Chortos, W.-T. Xu, et al., A bioinspired flexible organic artificial afferent nerve, Science 360 (6392) (2018) 998–1003, Jun.
[69] B.-N. Yan, Y.-R. Chen, H. Li, Challenges of memristor based neuromorphic computing system, Sci. China Inf. Sci. 61 (6) (May 2018), 060425, 1-3.
[70] X.-M. Zhang, Y. Zhuo, Q. Luo, et al., An artificial spiking afferent nerve based on Mott memristors for neurorobotics, Nat. Commun. 11 (1) (Jan. 2020), 51:1-9.
[71] C. Sung, H. Hwang, I.K. Yoo, Perspective: a review on memristive hardware for neuromorphic computation, J. Appl. Phys. 124 (15) (Oct. 2018), 151903, 1-13.

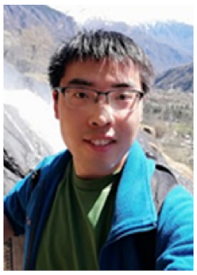
Yu-Hao Wang was born in Heilongjiang in 1997. He received his B.S. degree from Dalian University of Technology, Dalian, in 2019. He is currently pursuing the Ph.D. degree with the Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS), Beijing; also with University of Chinese Academy of Sciences (UCAS), Beijing. His research interest focuses on neuromorphic computing based on redox memristors.



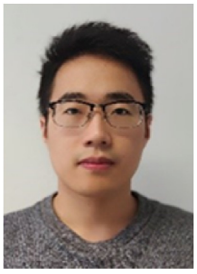
Tian-Cheng Gong was born in Anhui in 1992. He received the B.S. degree from Xidian University, Xi'an in 2010 and the Ph.D degree from UCAS in 2019. He is currently an associate professor with IMECAS; he also works with UCAS and also with Peng Cheng Laboratory, Shenzhen. His research interests include the reliability of emerging memories.

Ya-Xin Ding was born in Shandong in 1995. She received the B.S. degree from the Qingdao University, Qingdao in 2018. She is currently pursuing the Ph.D. degree with the Key Laboratory of Microelectronics Devices and Integrated Technology, IMECAS; also with UCAS. Her research interests include nonlinear selector devices and self-selective devices.

Yang Li received her M.S. degree in microelectronics and solid state electronics from IMECAS in 2016, and her Ph.D. degree from Technical University of Denmark, Denmark in 2020. From 2020 to 2021, she worked as a postdoctoral researcher at Department of Electrical Engineering, Israel Institute of Technology, Haifa. Currently, she is an assistant researcher at Peng Cheng Laboratory, Shenzhen. Her research interests include oxide materials, resistive switching devices, and device modeling.



Wei Wang received his B.S. degree in microelectronics from Nankai University, Tianjin in 2011, and his Ph.D. degree from IMECAS in 2016. From 2017 to 2020, he was a postdoctoral research assistant at the Department of Electronics, Information and Bioengineering, Politecnico di Milano, Milan. From 2020 to 2021, he continued his postdoctoral research at Israel Institute of Technology. Currently, he is an associated researcher with Peng Cheng Laboratory. His research interests include memristive switching devices and neuromorphic computing.



Zi-Ang Chen received his B.S. degree in microelectronics manufacturing engineering from Guilin University of Electronic Technology, Guilin in 2014. He received the M.S. degree in microsystems and microelectronics from Technical University of Chemnitz, Chemnitz in 2019. He is currently pursuing the Ph.D. degree at the Institute for Solid State Physics, University of Jena (Friedrich-Schiller-Universität Jena), Jena; is also with Leibniz Institute of Photonic Technology (IPHT), Jena. He research interests include in memristive devices, digital and analog electronic circuit design using the memristors and transistors, and development of Advanced-Encryption-Standard (AES) security system exploiting resistive switching devices.

Nan Du received the Diploma degree in electrical engineering from the Faculty of Electrical Engineering and Information Technology, Technical University of Dresden, Dresden in 2011, and the Ph.D. degree in electrical engineering from the Technical University of Chemnitz in 2016. Since 2008, she has been a member of the scientific staff at Helmholz Zentrum Dresden Rossendorf, Dresden. Between 2017 and 2019, she was a postdoc with Fraunhofer Institute for Electronic Nano Systems, Chemnitz, Germany. In October 2019, she leaded both the research group "MemDevice" at University of Jena (Friedrich-Schiller-Universität Jena), Jena and the research group "Radiometry" at IPHT, Jena. Since 2020, she has been a member of Coordination Board of Priority Program Nano Security in German Research Foundation (Deutsch Forschungsgemeinschaft, DFG) and has extended experience in leading fundamental research projects. Currently, she is a professor with University of Jena, Jena; also with IPHT, Jena.

Dr. Du is the corresponding author or co-author of more than 30 publications and 12 inventions (information from depatisnet.dpma.de). Her research interest focuses on the development of innovative unconventional computing systems exploiting resistive switching devices, such as, brain-inspired neuromorphic computing, in-memory computing, and probabilistic computing.

Erika Covi received her Ph.D. degree in microelectronics in 2014 from The University of Pavia, Pavia. She worked as a postdoctoral research fellow at National Research Council (CNR), Roma, then at Politecnico di Milano. She is currently a European Research Council (ERC) group leader at Nanoelectronic Materials Laboratory (NaMLab), Dresden. Her research interests include the intersection of emerging devices, circuit design, and brain-inspired computing. More specifically, she focuses on exploiting the intrinsic physical characteristics of memristive devices to reproduce computational primitives of the brain in mixed neuromorphic-memristive systems.

Matteo Farronato received his B.S and M.Sc. degrees in electronics engineering from Politecnico di Milano in 2017 and 2019, respectively. When he pursued his Ph.D. degree, he worked on the development of emerging nanoelectronic devices based on 2-dimensional (2D) materials for neuromorphic computing. Currently, he is working as a postdoctoral researcher with Politecnico di Milano. His research interest focuses on emerging devices based on 2D materials for memory and neuromorphic applications.

Daniele Ielmini received the Ph.D. degree from Politecnico di Milano in 2000. He held visiting positions at Intel Corporation and Stanford University, Stanford in 2006. His research interests include modeling and characterization of non-volatile memories, such as the phase change memory (PCM), resistive random-access memory (RRAM), and spin-transfer torque magnetic memory (STT-MRAM). Currently, he is a professor with Politecnico di Milano.

Prof. Ielmini authored/co-authored more than 400 papers in international journals and conferences. He is the Associate Editor with *IEEE Trans. on Nanotechnology* and *Semiconductor Science and Technology* (IOP Publishing). He received the Intel Outstanding Researcher Award in 2013, the ERC Consolidator Grant in 2014, the IEEE-Electron Devices Society (IEEE-EDS) Paul Rappaport Award in 2015, and the ERC Advanced Grant in 2021. He is the Fellow of IEEE.

Xu-Meng Zhang received his Ph.D. degree from IMECAS in 2020. He is currently an associated professor with the Frontier Institute of Chip and System, Fudan University, Shanghai. His current research interests include neuromorphic computing with nonlinear dynamical memristive devices to implement synapses, neurons, and their integrated chips based on neuroscience principles.

Qing Luo received his Ph.D degree from IMECAS in 2017. He is currently a professor with the Key Laboratory of Microelectronics Devices and Integrated Technology, IMECAS. His research interest focuses on new memory devices, including resistive RAM devices and ferroelectric memory devices.