40-nm SPAD-Array System for Ultra-Fast Raman Spectroscopy

H. Haka, A. A. Maurina, V. Storari, I. Cusini, F. Madonini and F. Villa

Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Piazza Leonardo da Vinci 32, 20133 Milano, Italy
ICFO-Institut de Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain
federica.villa@polimi.it

I. Introduction

The PoteinID (ProID) European project focuses on the development of a novel detection system that can perform ultra-fast Raman Spectroscopy (RS) with the aim of protein identification. The protein comprised of an amino acid (aa) chain is first denatured and then passed through a plasmonic nanopore. Each aa molecule is excited with a monochromatic laser and such excitation is followed by a Raman scattering process and subsequent autofluorescence. The goal of the detector developed by us, is to collect only the Raman photons while rejecting the fluorescence signal. By exploiting the fact that the fluorescence signal has a characteristic time constant in the order of few nanoseconds, while the Raman signal has a characteristic time constant in the order of few hundreds of picoseconds, we can reject the fluorescence signal by employing time-filtering techniques. The time-filtering technique used in this system is the Time-Gated Single-Photon Counting (TG-SPC). With this gating strategy we can define a temporal window (referred to as gate) where the SPADs are photosensitive and outside this window the photons are not detected. By using a sub-ns gate generated internally by the array, we can make the SPADs photosensitive only to the Raman photons. After the photons are detected and counted by each pixel, the sum of the four pixels inside a column is available at the output as an 8-bit word. The sums of the columns are outputted sequentially starting from the last one and then scanned in a shift-register pattern. Each column has a readout time of around 10 ns, so by using a 100 MHz reading clock, a full readout of 1.28 µs can be achieved. Thanks to the innovative jump readout modality, it is possible to select a specific subset of the column to read and thus reducing the overall readout time by 10 ns per each disabled column. By disabling 28 columns it is possible to reach sub-µs readout time. This technique was inspired by results shown presented in [1]. In this paper, we present the characterization of a detector developed as a preliminary version to the 128 x 4 SPAD array. The detector tested in this paper is based on a 16 x 4 SPAD array developed in the same 40 nm planar technology.

II. SPAD Array Architecture

The 128 x 4 SPAD array was designed in the 40 nm planar technology by STMicroelectronics to meet the high-speed readout performances of the ProID project. Each pixel is connected to a Variable-Load Quenching Circuit (VLQC) [2] frontend that actively quenches the SPAD detector. The events sensed by the pixel are counted by a 6-bit counter, so each column has four 6-bit counts. These counts are summed in a global adder to provide an 8-bit sum per each column. The columns counts are sent sequentially to the global adder.

The detector has an in-chip gate generation module that generates two gating signals referred to as “gate hardware” and “gate software”. The gate hardware signal is applied in the frontend circuits to physically turn off the SPADs, thus making them not photosensitive. The gate software signal is applied to the 6-bit pixel counters and all counts outside the gate software window are not considered, even if the SPAD outputs them as event. The purpose of the gate hardware is to lower the probability of afterpulsing for the SPADs, decrease energy consumption and acts as a first filtering effect to the fluorescence. However, with gate hardware alone it is not possible to achieve sub-nanosecond gate duration due to the limitations in the speed of changing the bias of the SPAD detector. By using the gate software, an additional filtering effect is introduced inside the gate hardware window, which does not have the limitations on speed and can be in the sub-nanosecond range. Both gate signals are generated by an internal Delay-Locked Loop (DLL) combined with a twin Voltage-Controlled Delay Line (VCDL) to produce 50 Process Voltage Temperature (PVT) insensitive pulses that are equally spaced. This module makes it possible to externally set the gate signals relative to a synchronization signal given externally, with a 200 ps resolution.

III. 16 x 4 Detector Characterization

At the time of writing this paper, the results for the 128 x 4 were not available, so the characterization of the preliminary 16 x 4 detector is presented. The 16 x 4 chip implements the same principles and modules as the 128 x 4 SPAD array detector. One of the main figures of merit for SPADs is Dark Count Rate (DCR), which expresses the number of thermically generated events in the absence of illumination. The DCR characterization of the array was carried out at 32.5 °C, with the SPADs biased with both a 1 V and a 1.5 V excess voltage (15.5 V and 16 V overall SPAD reverse voltage). The results are shown in as a Cumulative Distribution Function (CDF). The array displays a median DCR of 200 cps for 1 V excess bias and of 430 cps for 1.5 V excess bias. Setting a threshold at twice the median DCR, 17.2 % of the pixels are hot pixels, while this value reduces to 7.8 %, when the threshold is set at 100 times the median DCR. The Photon Detection Probability (PDP) of the SPAD array was measured including microlenses and for multiple wavelengths. It exhibited a peak at 540 nm with a value of 18.6% for V_{EX} = 1 V and of 22 % for V_{EX} = 1.5 V, which is among the best values available for Raman spectroscopy [3]. The afterpulsing probability of the SPAD detector was characterized using a free-running VLQC with adjustable hold-off time, that was included as a test structure in the chip sent to fabrication. This measurement gave a result below 0.1 % with no variation for different hold-off times. The SPAD timing jitter was also measured with Time-Correlated Single-Photon Counting (TCSPC) setup. For this measurement, the SPADs were biased at 1 V excess voltage and illuminated with an 850 nm laser. For this wavelength the PDP of the array is around 2 %, which accounts for the low number of counts in the characterization results. The SPAD pulse is shown in Figure 2 and exhibits a FWHM of 23 ps with a diffusion tail that has a time constant of about 1 ns. The diffusion tail starts one decade below the timing peak. To characterize the gate time performance of the 16 x 4 SPAD array detector, the laser pulse was scanned inside the user-set gate hardware and gate software windows. The minimal duration of gate hardware signal is 3 ns. The minimum gate software signal duration is roughly 300 ps. The shape of the gate hardware and minimal gate software signals are reported respectively in Figure 4 and Figure 6.

References

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[2] D. Bronzi, S. Tisa, S. Bellisai, A. Tosi and F. Zappa, "Fast Sensing and Quenching of CMOS SPADs for Minimal Afterpulsing Effects," *IEEE Photonics Technology Letters*, vol. 25, no. 8, pp. 776-779, 2013.

[3] A. Chiuri and F. Angelini, "Fast Gating for Raman Spectroscopy," *Sensors 21*, vol. 8, p. 2579, 2021.

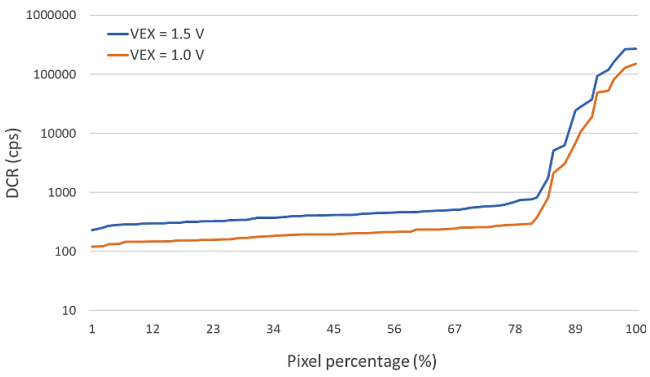

Figure 1. Cumulative Distribution Function (CDF) of the DCR for all the 16 x 4 SPADs at V_{EX} = 1 V and V_{EX} = 1.5 V, without cooling the array (operating at temperature 32.5 ºC)

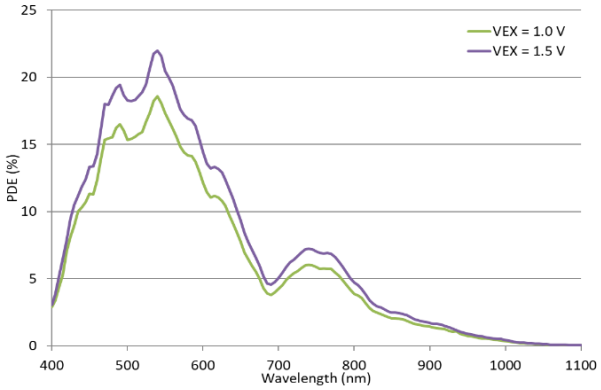

Figure 2. PDP plots measured at 1 V and 1.5 V excess bias

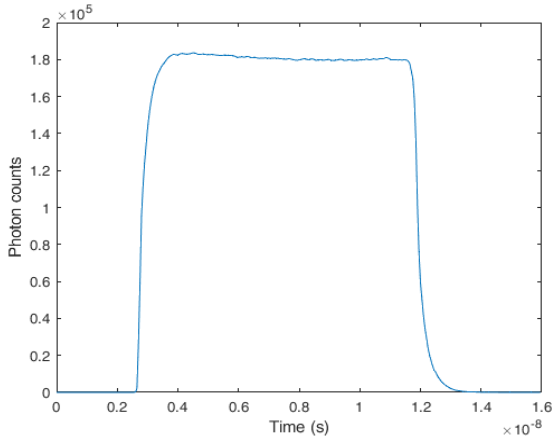

Figure 4. Gate hardware time performance activating only one pixel (10 ns gate)

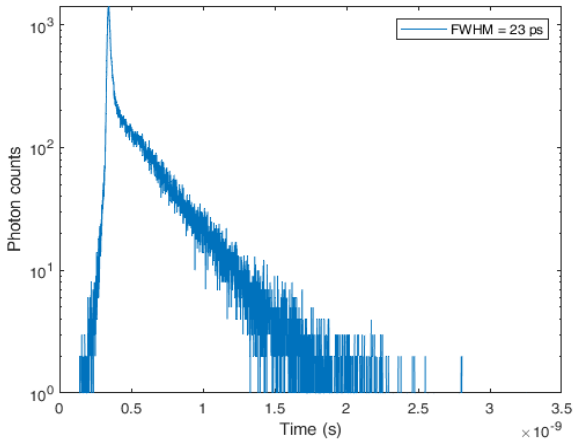

Figure 3. SPAD timing jitter measured with an 850 nm laser source

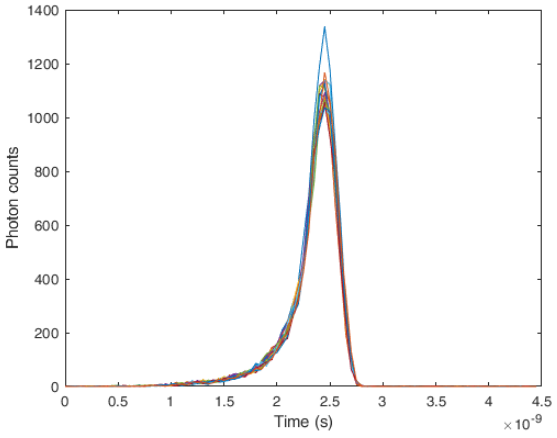

Figure 6. Minimum soft-gating window duration plotted for all 16 columns

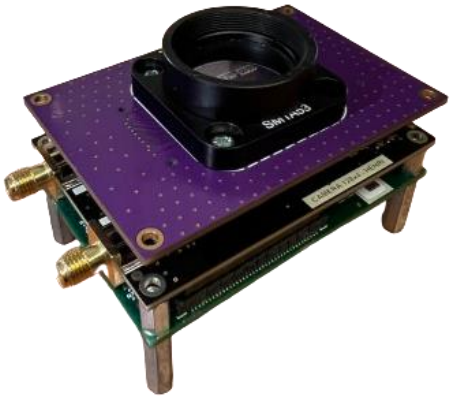

Figure 5. Assembled 128 x 4 SPAD array detection system (pending characterization)

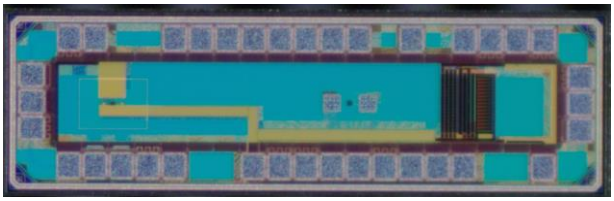

Figure 8. 16 x 4 chip micrograph

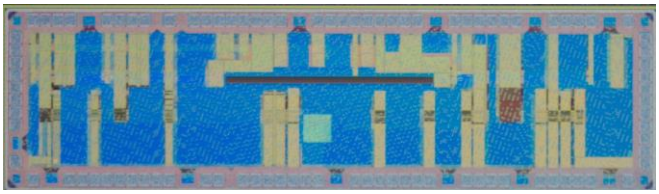

Figure 7. 128 x 4 chip micrograph