Fast-gated 16×16 SPAD array with on-chip 6 ps TDCs for non-line-of-sight imaging

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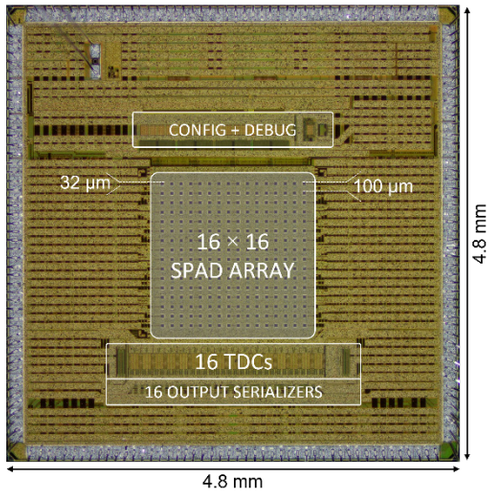

Fig. 1: Micrograph of the 16 × 16 SPAD array.

We present a 16 × 16 SPAD array fabricated in a 160 nm BCD technology and integrating 16 TDCs with 6 ps resolution. Such imager has been specifically designed for non-line-of-sight (NLOS) imaging applications, which both requires accurate single-shot precision, for not impairing the final image reconstruction quality, and time-gating capabilities, in order to filter-out direct light reflections and only acquire those photons that scattered multiple times from the hidden scene before reaching the sensor.

Our 16 × 16 SPAD array combines high photon detection probability (> 60% around 500 nm) with narrow time responses (average timing jitter is 62 ps - full width at half maximum) and SPAD activation times faster than 500 ps, with a gate repetition rate up to 100 MHz. Differential and integral non-linearities (rms values) are as low as 250 fs (0.04 LSB) and 22 ps (3.6 LSB), respectively, when 30 ns gate-windows are employed. Instrument response functions are consistent throughout the gate-window, with a time-dispersion of just 3.4 ps.

We implemented an event-driven readout approach that enables to time-tag up to 1.6 · 108 events per second while in time-tagged time-resolved (TTTR) mode, thus making possible to easily synchronize the array with any external scanning system for increasing the spatial resolution of reconstructed NLOS images and videos.

Simone Riccardo received the M.S. degree in Electronics Engineering in 2018 and he is currently pursuing the Ph.D. degree in Information Technology, both at Politecnico di Milano, Italy. His research activity focuses on the design of time-gated CMOS imagers based on single-photon avalanche diodes (SPADs) for 3-D ranging applications.