Improved Dynamic Range Charge-Sensitive Amplifier

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***Abstract*—Charge sensitive amplifiers (CSA) are key elements for the readout of charge signals produced by ionizing radiation and particle detectors. In nuclear microelectronics, these circuits are characterized by stringent requirements in terms of equivalent noise charge (*ENC*), and maximum input charge specification, which is tied to the voltage output swing capability of the amplifier itself. The need for periodic or continuous discharge of the feedback capacitance further constrains the design choices. In this work, a circuital solution that acts on the feedback discharge path to optimize the quiescent operating point of the CSA is presented, allowing an increase in the effective dynamic range of the CSA without affecting the spectroscopic resolution of the system. In addition, the proposed reset architecture allows to use a single power supply, avoiding the double supply generally used to increase the dynamic range, gaining in system compactness. Experimental measurements show an increase of + 107% in the dynamic range with respect to standard reset architectures of state-of-the-art CSAs for low-capacitance (≤ 0.1 pF) semiconductor radiation detectors, achieving a total maximum input charge of ≃ 3×10^5 el. (47 fC), corresponding to 1.08 MeV equivalent energy in silicon or 1.31 MeV in cadmium-zinc-telluride detectors. The preamplifier implements a fast feedback capacitance discharge rate of 2.5 fC/ns (t_{fall}^{90-10} = 18.8 ns over the full output range), and preserves an excellent intrinsic noise performance of 3.7 electrons rms, making it suitable for high-speed, high-energy-resolution spectroscopy applications.**

***Index Terms*—Charge sensitive amplifiers, nuclear electronics, radiation detector circuits, low-noise electronics, radiation instrumentation.**

I. Introduction

CHARGE sensitive amplifiers (CSAs) are electronic circuits that use a low-noise voltage amplifier with a capacitor in negative feedback, to integrate a pulse-like current signal at the input terminal, and produce a step-like output voltage signal proportional to the input charge. In X and γ-ray detection instrumentation, CSAs are the preferred front-end choice for signal processing within high-resolution spectroscopy applications, where the initial energy of the incoming radiation is measured by means of the total charge generated in a suitable radiation detector connected at the CSA input [1]. CSA are also widely used to readout detectors in high energy physics, astrophysics, charge detection mass spectrometry, and in several medical and industrial applications [2], [3], [4], [5]. In CSAs, typically modeled as in Fig. 1, the feedback capacitance C_f plays an important role in defining the charge-to-voltage conversion gain, which can be derived as:

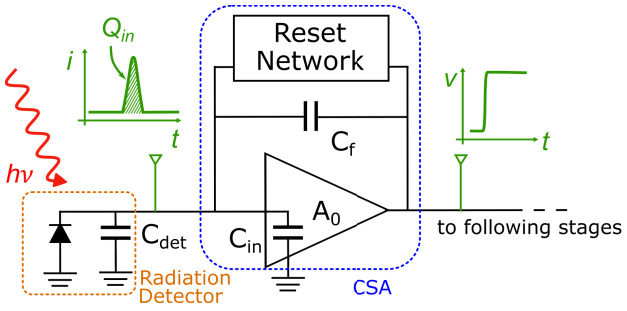

Fig. 1. Schematic model of a Charge Sensitive Amplifier (CSA) DC-coupled to a radiation detector.

$$G_{CSA} = \frac{v_{out}}{Q_{in}} = \frac{1}{C_f} \cdot \frac{1}{1 + \frac{C_{IL}}{C_f A_0}} \tag{1}$$

where v_{out} is amplitude of the small-signal output voltage step, Q_{in} is the small-signal input charge, A_0 is the modulus[1] of the DC open-loop small-signal gain of the amplifier, and C_{IL} is the total load capacitance at the CSA input node (in nuclear electronics C_{IL} is typically defined including both C_f, the detector capacitance C_{det}, the preamplifier C_{in} and any additional stray capacitance at the input, representing one of the most critical parameters for noise performance evaluation [6]).

For a sufficiently large loop-gain $\left(\frac{C_f A_0}{C_{IL}}\right)$, G_{CSA} can be conveniently assumed equal to the reciprocal of C_f, and independent from the A_0 variations over process, voltage and temperature (PVT), and can be considered constant and time-invariant. However, as the DC operating point of the CSA is continuously modified during the normal operation of the circuit (see next section and Fig. 2), the A_0 can significantly

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[1]To implement an overall negative feedback, A_0 must be negative in sign.

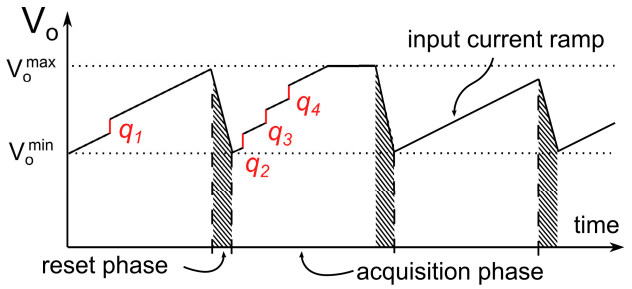

Fig. 2. A simplified graph showing the output voltage time diagram of a CSA for a fixed-frequency pulsed-reset configuration, showing a voltage ramp caused by the DC input current, and voltage steps in red are caused by input charge packets (q_1, q_2, q_3, q_4). Both the DC input current and the input charge packets contribute to the erosion of the CSA voltage headroom, until it reaches saturation for $V_o = V_o^{max}$.

drop as the output node approaches the supply voltage, resulting in an undesired variation of the G_{CSA} gain over time [7], [8].

By defining ΔV_o^{max} the maximum output voltage swing for which the gain variation is considered acceptable, the maximum input charge is $Q_{in}^{max} = \Delta V_o^{max} C_f$ and the input dynamic range (DR) can be computed as $DR = Q_{in}^{max}/ENC = \Delta V_o^{max} C_f/ENC$ where the equivalent noise charge (ENC) is, by definition, the input charge signal which leads to a unity signal-to-noise ratio [9]. In most applications, the largest DR with the highest linearity in the charge-to-voltage conversion gain is desired in order to cover the widest range of input energies with minimal spectral distortion. Provided the high-linearity requirements of CSA applications, a given voltage of the power supply sets the upper limit of ΔV_o^{max}, and Q_{in}^{max} can be made larger by increasing C_f. However, a higher C_f implies a worsening of the ENC because of: 1) the increase the total input capacitance C_{IL} and 2) the reduction of the CSA series noise gain (equal to C_{IL}/C_f), which de-multiplies the noise contribution of all following stages (e.g. shaping amplifier). Indeed, for low-noise applications, it is desirable to have a high noise gain ($C_{IL}/C_f \gg 1$), which sets an upper bound for C_f, i.e. $C_f \ll C_{IL}$, and consequently $C_f \ll C_{det}$. This constraint is particularly relevant in the case of low output capacitance detectors, such as semiconductor pixel or drift detectors, where C_{det} is smaller than 100 fF [10]. So, the increase of C_f, even though it always increases Q_{in}^{max}, has a limited or even a detrimental effect on the dynamic range, per consequence of the collateral increase of the system ENC.

In this work, an effective solution based on the modification of the reset path is proposed and experimentally verified to increase the dynamic range of charge sensitive amplifiers, without increasing C_f and without affecting the spectroscopic resolution of the system. For the circuit characterized within this work, the improvement resulted in a doubling of the output voltage swing, while keeping the optimum equivalent noise charge as low as 3.7 el. rms.

II. Limits to the Dynamic Range in Traditional CSA Architectures

As for every electronic circuit, the linearity assumption of the CSA is only valid in a given range of operating points (OPs); indeed, due to the non-linearity of the internal elements of the circuit, the charge-to-voltage relationship is inevitably lost when large signals are applied, or whenever multiple events pile-up in a short span of time. For this reason, in CSAs a reset network (see Fig. 1) is always present to continuously or periodically discharge the feedback capacitance, restoring a suitable OP for the following input charge signals. In continuous reset circuits, such discharge is obtained by providing a DC current path, by means of a high-value resistor, a forward biased JFET or diode [11], a MOSFET in ohmic region [12], or other constant current discharge circuits [13], [14]. In pulsed-reset CSAs, instead, the reset network is typically constituted by a CMOS switch in parallel to C_f, which periodically zeroes the charge accumulated during the acquisition time, short-circuiting C_f itself [15]. In this latter configuration, which optimizes noise and count-rate performances, multiple events are deliberately stacked on C_f, until a discharge is triggered by means of dedicated reset logic. In this case, even small charge signals can stack on the feedback capacitance across the acquisition phase, producing a voltage "staircase" which brings the CSA output node to saturation, as schematically shown in Fig. 2; also DC currents at the input of pulsed-reset CSAs, will result in a similar effect, appearing as a voltage "ramp" on the output node. As pointed out in the introduction, increasing the dynamic range requires increasing $Q_{in}^{max} = \Delta V_o^{max} C_f = (V_o^{max} - V_o^{min}) \cdot C_f$ without increasing C_f. While V_o^{max} can approach the CSA voltage supply with a proper design of the output stage, the minimization of V_o^{min} finds a fundamental limit and drawbacks in all the commonly used architectures of CSA, as described in the following. Let's consider a typical CMOS CSA shown in Fig. 3a with a p-MOSFET input which is the preferable choice when it is important to minimize the 1/f noise contribution [6], but specular considerations can be applied when a n-MOSFET input is used. If the CSA is designed for negative input charges, the ramp is positive (as in Fig. 2) and to increase the dynamic range is necessary to minimize V_o^{min}. But, at the end of the reset discharge, the voltage across C_f is approximately zero, so that the amplifier's output voltage is equal to its input voltage DC voltage $V_o^{min} = V_{IN}^{DC}$. Consequently, lowering V_o^{min} necessarily imposes to use two power supplies with $V_{DD1} < V_{DD2}$ (see Fig. 3) to decrease $V_{IN}^{DC} = V_{DD1} - V_{GS1}$ as much as possible. Filtering and routing V_{DD1} with extreme care is mandatory, due to the very low power-supply rejection ratio that the circuit shows toward noise sources from this node. Moreover, this widely used double supplies solution is not ideal for compact front-end assemblies, such as for detectors placed on spaceborne instruments, or cryostat setups [16], where the minimization of routing is preferred.

III. New Reset Architecture

Most of pulsed reset CSA implementations use the standard architecture of Fig. 3a, because the most immediate thought is that to discharge C_f it is necessary to short-circuit it, as done with SW_{RES}, being also the easiest solution. Our idea breaks this standard by considering that actually the discharge of C_f can be done by generating any loop across C_f, where the discharge current can flow, and this can be done using a node different from the preamplifier output as second

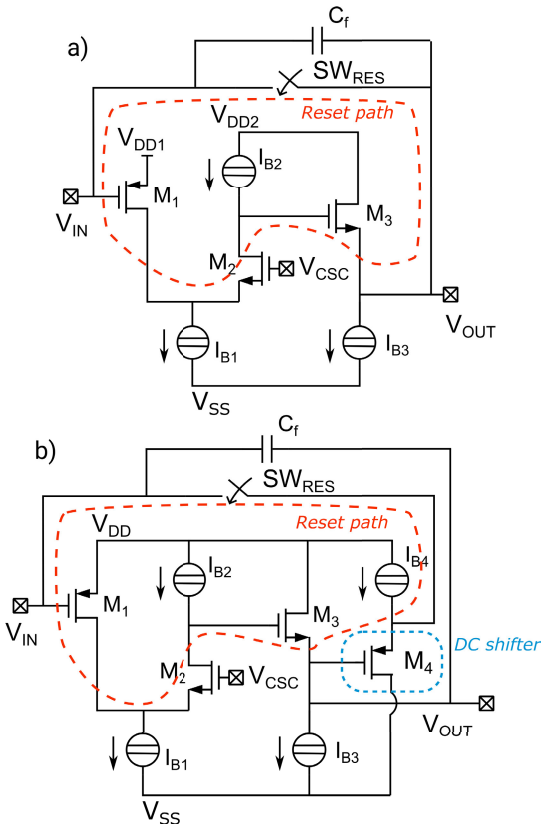

Fig. 3. In a), a standard implementation of a CMOS pulsed-reset CSA with separate supply voltages V_{DD1} and V_{DD2}. In b), an example of the proposed solution with the addition of the M_4 voltage shifter on the discharge path. The input terminal can be both DC or AC coupled to the sensor, according to the desired detector bias scheme.

node for the switch [17]. In this conception, during the reset phase C_f is pre-charged to a more convenient non-zero value, which can be positive or negative according to the collected charge polarity and to the specific preamplifier architecture. Figure 3b shows an implementation of the proposed solution, applied starting from the classical architecture of Fig. 3a, where the branch of the M_4 transistor has been added in series to the reset switch SW_{RES}. Thanks to M_4, the DC value on the V_{OUT} node at the end of the reset phase, will be $V_{OUT}^{min} = V_{DD} - V_{GS1} - V_{GS4}$, lower than the value obtainable without M_4 and with the additional advantage to use a single power supply at V_{DD}, avoiding V_{DD1}, with great advantages for the system economy and compactness. It is to be highlighted that M_4 and I_{B4} noises do not significantly contribute to the preamplifier ENC, in fact when the SW_{RES} is open, both I_{B4} and M_4 noise sources are disconnected from the input node, and contribute only minimally to the output noise through the parasitic coupling with the M_4C_{gs}. The presence of the voltage buffer M_4 leaves the reset-phase loop-gain mostly unaltered, with minimal impact on the reset speed and stability. If a low dispersion of the ramp starting voltage V_o^{min} is required across PVT - which might cause variation of serveral tens of mV, the V_{GS} spread of M_4 can be compensated regulating the I_{B4} current, or by implementing more controllable level-shifting solutions [18], or by finely tuning the baseline reset voltage using the architecture proposed in Fig. 4. In this case, the

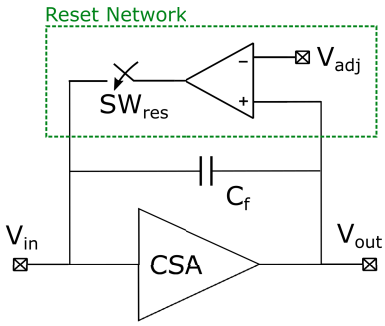

Fig. 4. Example of a general implementation of a pulsed-reset CSA with the addition of the V_{ADJ} voltage shifter on the discharge path. Despite increasing the circuit complexity, this solution helps keeping a consistent baseline reset voltage over process, voltage and temperature variations.

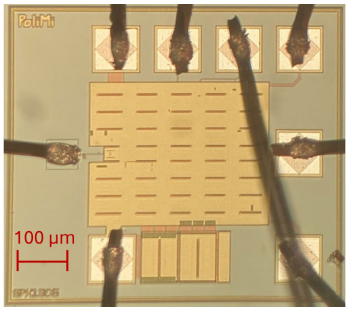

Fig. 5. A micrograph of the proposed circuit (dimensions: 675×600 µm^2).

reset network is realized with the help of an additional operational amplifier, which, with respect to other continuous-reset alternatives using a differential pair with a low-frequency loop for leakage compensation [19], allows a precise regulation of the reset baseline voltage to the V_{adj} value, even for the fast transient associated with pulse reset architectures. The V_{adj} voltage reference, whose noise spectral power density is also irrelevant for the CSA ENC performance, can be eventually implemented off-chip for better control at system level. The fundamental condition of the proposed solution, independent by the practical possible different implementations, is to drive the reset switch SW_{res} with a node following after V_{OUT}, so to guarantee the negative feedback during the reset phase, with a convenient DC shift. The proposed solution can be eventually implemented also in CSA operating with continuous reset network.

IV. Experimental Results

We produced a CSA in a 0.35 µm CMOS technology, based on the work presented in [20], including the modification shown in Fig. 3b to improve the output voltage swing. A micrograph of the chip is presented in Fig. 5. The implemented CSA features an extra pad to allow validation of the dynamic range enhancement solution in both pulsed and continuous reset configuration. A negative supply, is also present for legacy reasons, and can be grounded without affecting the CSA dynamic range. The CSA can be operated in reset or continuous mode by acting on two pads (RESET and CTRL). When the RESET pin is set to '1' (reset phase), a custom internal logic, in combination with an analog control pad

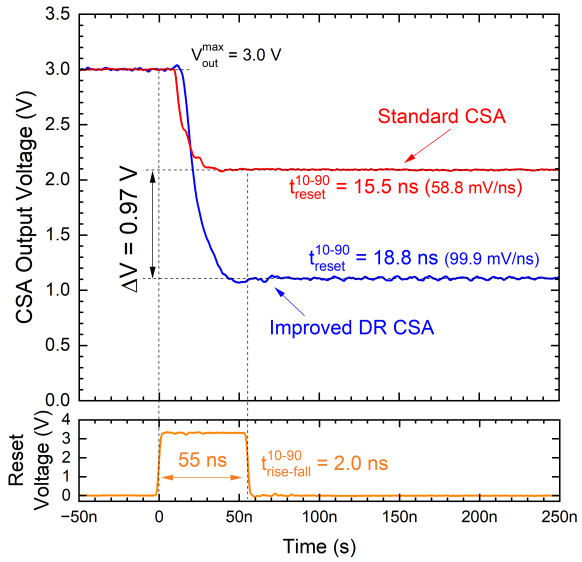

Fig. 6. Comparison between the reset phase of a standard preamplifier (red) and one with improved dynamic range (blue) connected to a semiconductor radiation detector. Despite the increased voltage swing, the reset speed remains almost unvaried, thanks to a further optimization in the output stage circuit. In the bottom part of the graph, the fast reset signal applied to the reset switch is reported (55 ns pulse width, 2.0 ns of rise-fall time).

(CTRL), is used to set a voltage-controlled reset discharge time constant on the feedback network. Consequently, by keeping the CSA in reset state, the CTRL voltage can be used to configure the circuit into continuous reset operation. In turn, whenever the CTRL pad is tied to the positive supply voltage V_{DD}, the discharge time constant is minimized, and the RESET pad can be used to digitally toggle between the CSA acquisition ('0') or reset ('1') phases, bringing the preamplifier into pulsed-reset operation.

The comparison between the reset transients of the standard (in red) and the improved DR (in blue) CSA implementations are shown in Fig. 6. Thanks to the modification, the output voltage swing has been increased from 0.91 V to 1.88 V, resulting in a net increase from 22.8 fC to 47.0 fC in the maximum input charge over a 25 fF feedback capacitance, corresponding to a total equivalent maximum input energy of 1.08 MeV in Si or 1.31 MeV in CdZnTe detectors. The same shift, in the DC output voltage, is observed in continuous operation as well, confirming the suitability of the proposed solution for both continuous and pulsed reset configurations. In addition, for pulsed-reset operation, it is shown that the new architecture does not slow-down the specific reset speed (i.e. the output node discharge rate, expressed in mV/ns), because of the fast response of the $M4$ follower. In our new implementation, the reset speed has been further increased from 58.8 mV/ns to 99.9 mV/ns by improving the output stage with respect to the classical older version, reaching comparable total reset times over a doubled output voltage swing. By keeping the reset time (10-90%) below 20 ns, the reset dead-time is made comparable with the acquisition time of a single photon pulse, minimizing the impact on the CSA count-rate capability in high-throughput applications [21], [22].

Figure 7 shows the intrinsic *ENC* obtained on four CSA samples using the presented dynamic range improvement

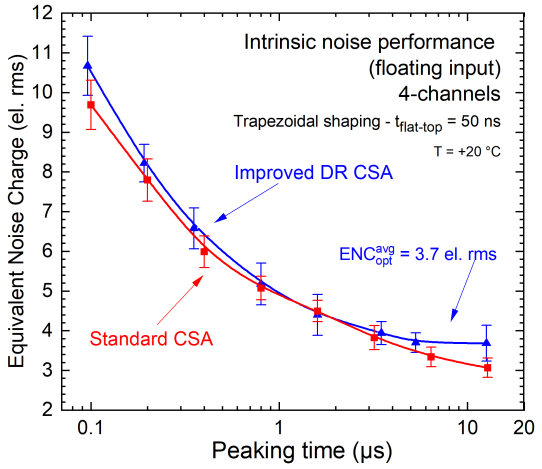

Fig. 7. In blue, the intrinsic *ENC*, without the detector, measured at room temperature (+20 ° C) on a set of four charge sensitive amplifiers with the proposed DR improvement solution. In red, the performance of standard CSA solution under the same conditions is shown for comparison.

TABLE I
STATE OF THE ART COMPARISON OF CSA FOR LOW-CAPACITANCE (≤ 0.25 FF) SEMICONDUCTOR RADIATION DETECTORS

Reference	Intrinsic *ENC* (el. rms)	Maximum Input charge (fC)	Voltage supplies (V)
This work	3.7	47	3.3, -5 (opt.)
Baseline CSA	3.1	23	3.3, -5 (opt.)
Sirio-6 [20]	3.2	15	3.3, -5
Cube [23]	3.3	50	3.3, 2, -6
IDeF-X [24]	17	40	N/A[1)]
DSSC-CSA [25]	40	88[2)]	1.6
SOIPIX-PDD [26]	11	1.4	3
HEXITEC-MHz [27]	<80	11	1.8

[1)] With internal current regulator.
[2)] With non-linear gain compression.

solution (in blue), and four CSA samples implementing the standard CSA architecture (in red) produced on the same wafer, for comparison purpose (on each curve, the bars represent the min-max of the four values). The results confirm the suitability of the proposed solution solution for very high-resolution spectroscopy applications with low-capacitance radiation detectors, obtaining an optimum *ENC* of 3.7 electrons rms. This is consistent with the fact that the additional circuitry required by the proposed solution is only acting during the reset phase, and not during the acquisition phase, where the noise analysis is relevant. This result effectively matches with the noise performances of the standard CSA circuit, and suitably fits into state-of-the-art CSAs circuits for low-capacitance detectors, as shown in the comparison Table I.

V. CONCLUSION

A novel approach to enhance the dynamic range of charge-sensitive amplifiers without compromising noise performance has been presented. By modifying the insertion point of the feedback discharge network, the proposed architecture achieves a significant increase in output voltage swing. For the prototype characterized, the modification resulted

in a doubling of the output voltage swing, from 0.91 V to 1.88 V, consequently improving the maximum input charge from 22.8 fC to 47 fC. As expected, experimental results confirm that the enhanced dynamic range does not significantly affect noise, maintaining an intrinsic ENC of 3.7 electrons rms, which is comparable to state-of-the-art CSAs, and resulting in an overall dynamic range of 98 dB. Alternatively, the proposed solution, increasing the useful output voltage swing, allows to employ smaller feedback capacitance, so improving the noise performance, by maintaining the same maximum input charge. It should be highlighted that the proposed DC-shifting solutions are not limited to the circuits shown in Fig. 3 and Fig. 4, and can be easily extended to different technology nodes and implementations of the core operational amplifier. Furthermore, the reset speed remains fast ($\simeq$ 20 ns), ensuring minimal dead time and suitability for high-throughput applications. The proposed solution eliminates the need for dual supply voltages, simplifying system design and improving compactness in high-density setups. Overall, this architecture provides a practical and scalable solution for next-generation nuclear electronics and high-resolution spectroscopy systems, combining improved dynamic range, low noise, and efficient implementation.

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