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The XGIS instrument on-board THESEUS: detector principle and read-out electronics

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Abstract: The functionality and experimental performance characterization of the latest four channel version of ORION ASIC, a very low noise multichip read out and processing electronics customized for the X and Gamma Imaging Spectrometer (XGIS) instrument onboard the Transient High-Energy Sky and Early Universe Surveyor (THESEUS) mission, is presented. XGIS is a set of two coded-masked wide field deep sky cameras using monolithic SDDs (Silicon Drift Detectors) and CsI:Tl (Thallium doped-Cesium Iodide) scintillator-based X-γ ray detectors. This paper highlights the design, working principle and the expected performances of the XGIS, on a small scale 2×2 prototype. Furthermore, the evolution timeline of different versions of ORION with detailed performance observations and analysis for spectroscopic resolution, electronic noise and the operational linear energy ranges of both X and the γ processors of the four-pixel ASIC version bonded to a 2×2 SDD array are emphasized. Each 2×2 SDD array element is electrically and dimensionally equivalent to single elements of the THESEUS 8×8 SDD array.

Keywords: Gamma detectors; On-board space electronics; Space instrumentation; X-ray detectors and telescopes

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Contents

1 The THESEUS mission

The *Transient High-Energy Sky and Early Universe Surveyor* (THESEUS) is a multi-instrument space mission concept proposed to the European Space Agency (ESA) for the medium size missions M7 call, within the Cosmic Vision Program, scheduled for launch in 2037. With the past heritage derived as one of the successful candidates from M5 Phase-Assessment (Phase-A) study conducted by ESA in 2018, THESEUS successfully qualified the M7 Phase-0 in 2022 and is now one of the three successful candidates selected in November 2023 for a M7 Phase-A study to be conducted over a period of the next 2.5 years. THESEUS is now foreseen to start a phase A study in the beginning of 2024 in alignment with the requirements specified by ESA.[1]

THESEUS essentially aims to explore the early Universe by providing a complete population of Gamma Ray Bursts (GRBs) in the first billion years, and also contribute to the next generation of multi-messenger and time-domain astrophysics by accomplishing an unparalleled deep monitoring of the X-ray transient Universe [1, 2].

These scientific goals require a combination of innovative technologies and on-board capabilities to perform wide-field X-ray imaging, to obtain broad bandpass X-ray spectra and to localise and characterise the high-energy transients in the optical-infrared domain. Good transient detection capability is achieved through very wide and deep sky monitoring in a broad energy band (0.3 keV–10 MeV) with the XGIS, while good focusing capabilities in the soft X-ray band (0.3–5 keV) with high positional accuracy ($\leq$ 2 arcmin) are achieved through the Soft X-ray Imager (SXI) and immediate transient identification, arcsecond localization, and redshift determination of these transients with a very high location accuracy ($<$ 1 arcseconds) is achieved with an onboard InfraRed Telescope (IRT).[2] These three instruments are combined in the THESEUS spacecraft as shown in figure 1. The XGIS is explained in detail in the following section.

[1] https://www.esa.int/Science_Exploration/Space_Science/Final_three_for_ESA_s_next_medium_science_mission.
[2] https://sci.esa.int/s/8Zb0RB8.

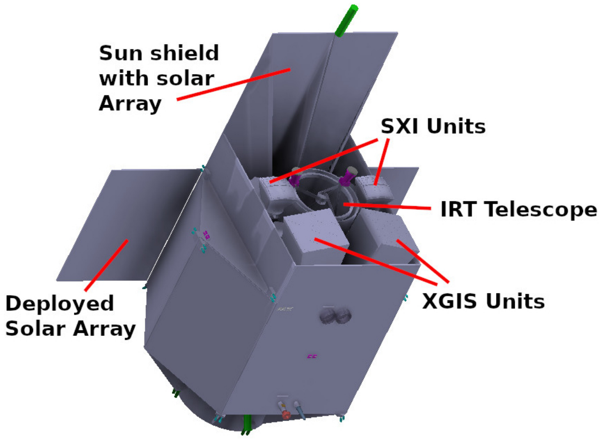

Figure 1. THESEUS Spacecraft with two SXI units, two XGIS cameras and the IRT.

2 The XGIS instrument on board THESEUS

The XGIS is a set of two coded-mask monitor cameras utilizing monolithic SDDs and CsI:Tl scintillator-based X-ray and γ-ray detectors with an expected operating range from 2 keV up to 10 MeV [3]. As a single instrument, the XGIS is capable of covering a Field of View (FoV) $\geq$2 sr with an unprecedented energy pass-band (from a few keV to a few MeV) with an effective area of a few hundred cm^2. This capability of XGIS makes it an extremely suitable instrument for the detection and localization of short GRBs to contribute to the multimessenger astrophysics, to supplement the SXI and IRT instruments for GRB detections through its high effective area in the soft γ energy range and for collecting unique information about the physics and geometry of X-ray transients and GRBs with a high spectroscopic and timing resolution [4].

XGIS exploits state-of-art technology, coupling SDDs with CsI:Tl crystal scintillator bars to acquire a broad energy band ranging from soft X-rays to γ-rays. Furthermore, a combination of a very low-noise distributed readout front and back-end electronics, equips XGIS with a position sensitive detection plane with a large effective area and a timing resolution up to a few µs.

As an imager, XGIS is based on the coded mask principle, with the mask shadowgram being recorded by a position sensitive detector, that can then be deconvolved into a sky image. The mechanical structure of XGIS consists of two identical partially coded masked X/γ-ray cameras (figure 2-left), two XGIS power Supply Units (XSU) and one Data Handling Unit (DHU). The XGIS cameras provide a FoV of 77×77 degrees^2 in an energy range of 15–150 keV and the inclination with respect to the satellite axis allows both FoVs to partially overlap and to incorporate the FoVs of both SXI and IRT onboard THESEUS resulting in a full FoV of 117×77 degrees^2.

The XGIS detector plane contains 10×10 modules arranged side by side with each module as a fundamental unit containing 8×8 monolithic SDD pixels (figure 2-right). A single XGIS module consists of two layers of 64 monolithic SDD pixels with 64 CsI:Tl crystals bars 30 mm long, sandwiched in between (figure 3). The modules on the whole XGIS detection plane are separated by 5 mm, resulting in 9 dead rows and 9 columns with width equivalent to one pixel. Therefore, each XGIS detector assembly has 6400 SDD pixels with a pitch of 5 mm for direct detection of X-rays and 6400 CsI:Tl crystals for γ-ray detection with a 5 mm pitch and 4.5×4.5 mm^2 cross section with each crystal 30 mm long.

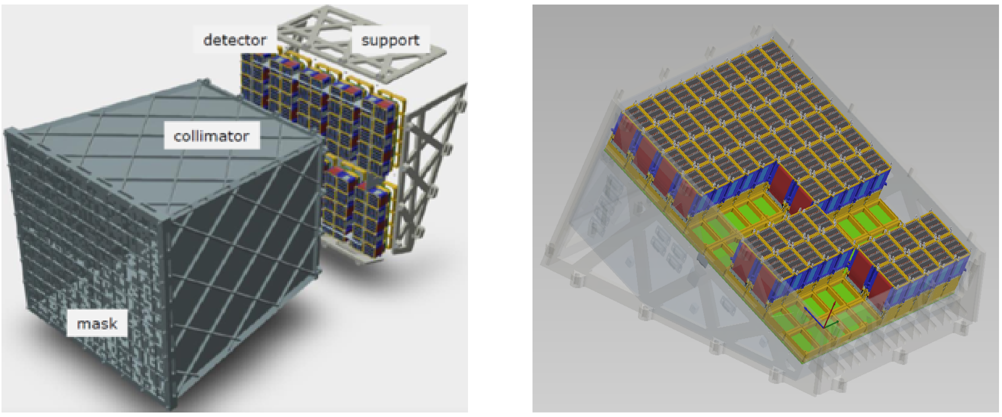

Figure 2. Left Panel: conceptual design of one XGIS camera (the detection plane and the collimator are shown separately). Right Panel: conceptual design of one XGIS detection plane.

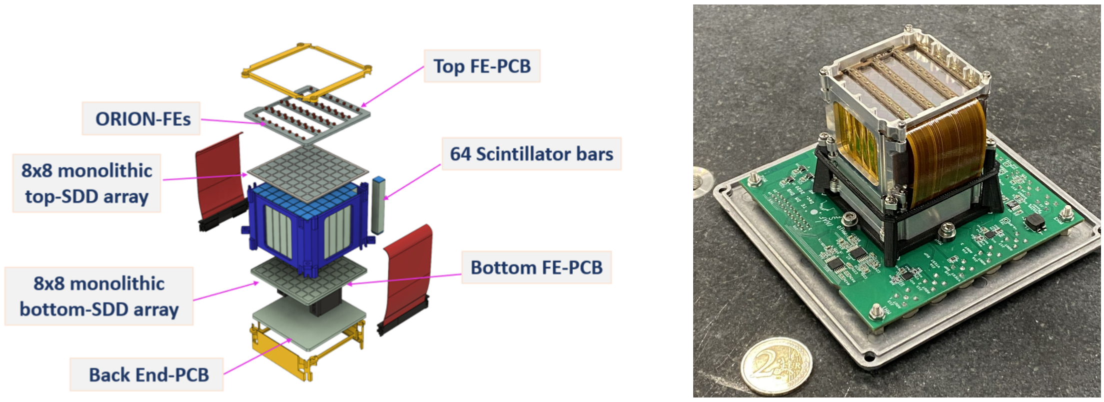

Figure 3. Left Panel: exploded view of one XGIS module. Right Panel: one XGIS demonstration module developed for the ESA M5 Phase A study conducted during 2018–2021 (Courtesy: OHB Italy).

3 Detector working principle: siswich

The key element of XGIS, a single pixel, is a sandwich of two top-bottom layers of 450 µm thick SDDs with a $4.5{\times}4.5{\times}30\,\text{mm}^3$ mid layer of CsI:Tl scintillator crystal, optically coupled with transparent silicone pads at both ends of the SDDs and wrapped with a reflective coating to guide scintillation light into the SDDs (see left panel of figure 4). Each XGIS pixel operates on the so-called *siswich* principle [5, 6], directly converting low energy X-ray photons ($\sim$ 2–30 keV) into charge in the SDD and converting scintillation light produced in the CsI:Tl crystals by hard X-ray and γ-ray photons (20 keV up to ~5 MeV) to produce an electronic charge signal. Considering all the XGIS modules as a whole detector and multiple time-coincident Compton interactions in the pixels, higher energy ranges up to 10 MeV or more are reachable.

The extremely small size of the anode with respect to the overall active area of the detector is a distinct feature of the SDDs which results in a very low device capacitance and low electronic noise [7, 8]. Therefore, this device is capable of providing a high energy resolution and a low-energy X-ray threshold. The CsI:Tl crystal instead offers high sensitivity in 30 keV up to 5 MeV with a high scintillation light output of $\sim$ 52,000 photons/MeV and an emission peak at 550 nm.

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As shown in figure 4, radiation with energy less than roughly 30 keV interacts in the top SDD, while higher energy photons pass through the thin SDDs and interact in the scintillator crystal bars producing optical photons. However, this unique combination of detectors poses a complex set of challenges for signal acquisition and processing. A suitable state-of-art electronic readout system is required to achieve X/γ signal differentiation, for low noise and good processing time performance. These requirements are met by a custom designed Application Specific Integrated Circuit (ASIC), named ORION [9–11] designed at the University of Pavia and Politecnico di Milano (PoliMi) which is capable of handling and discriminating the signals from both detector operating modes (i.e., direct interation in the SDDs or interaction in the scintillators).

When the signal is collected only from the top SDD, it is processed by an independent X-processor. Signals collected on both top and bottom SDDs are processed as γ-ray signals by an independent γ-processor (shown in the right image of figure 4).

The ORION FEs closely bonded to the top and bottom SDD anodes, provide preliminary pre-amplification, shaping and processing to the acquired charge signal by an integrated Charge Sensitive Amplifier (CSA) and forward this signal through a current conveyor to second shaping stages in X and γ processors of the BE with a shaping time of 1 µs and 3 µs, respectively [9, 12]. Output analog signals for all the pixels can be acquired directly from this stage by configuring the ORION ASIC in shaper operation mode. While in stretcher mode, additionally the shaped X signals and sum of shaped γ-Top and γ-Bottom signals are compared, in current mode, by respective X or γ amplitude discriminators, to user-defined, programmable threshold values. The toggling of the amplitude discriminator commands the peak stretcher [13] to hold the respective signal peaks and to issue a X or γ trigger with a specific timestamp assigned by time X or γ logic and time registers included in the processors. Analog to Digital conversion is then performed in digital domain by the three 16-bit ADCs depending on the triggered processors [10].

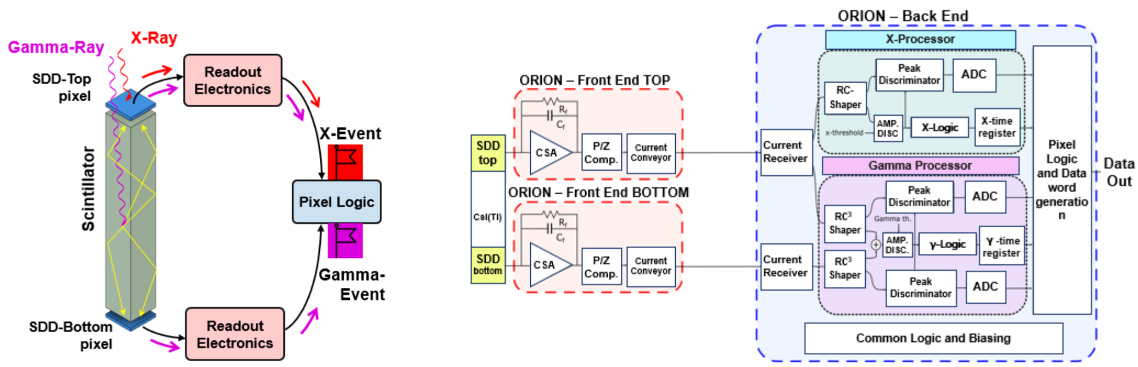

Figure 4. Left panel [9]: siswich principle: X-ray events are read only by the top SDD and γ-ray events are read by both top and bottom SDDs, through the scintillation light produced in the crystal. Right panel: schematic design of the ORION ASIC highlighting the main circuitry components of the top and bottom FE chipsets, connected to further receiver and shaping stages in the BE chipset.

4 Evolution of the ORION ASIC

The fabrication procedure utilizes a 0.35 µm Complementary Metal-Oxide Semiconductor (CMOS) technology. The design of the ORION ASIC requires the electronic chain of each detector to be split in two chips with the ORION-FE, essentially consisting of the preamplifier, placed near the detector, and

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the ORION-BE with the rest of the circuitry placed a few cm away from the ORION-FE. Additionally, the BE includes all the analog and digital functions related to signal processing [10].

Several development phases were required for the full implementation of the project. To save costs, the ORION development schedule was aligned with several Multi-Project Wafer (MPW) batch runs, which are summarized as follows.

1. **November 2019 MPW:** ORION-Analog to Digital Converter (ADC) chips are part of the ORION-BE ASIC chips. ADC chips were fabricated exclusively in the batch of November MPW run for performance and requirements investigations. Optimum performances were recorded during tests at University of Pavia [12].
2. **February 2020 MPW:** the first prototype of the ORION-FE and BE chipsets were manufactured in compliance with the electrical requirements and specifications of the single pixel of the XGIS module. This ORION-FE chipset prototype included two individual pre-amplifier circuits and a first stage of shaper circuit while a second receiving shaper stage of the pre-amplifier signal was mounted in the input part of the ORION-BE. The ORION-BE chipset prototype was also fabricated to include one complete channel circuitry for three independent processing channels (X, γ-Top and γ-Bottom), with 3 individual ADCs, time-stamping, event type with many accessible test points providing the digital data acquisition and parallel readout.
3. **June 2020 MPW:** the second prototype of the ORION-FE was manufactured, including two channels of individual pre-amplifier circuits with a topology to meet the requirements of European Cooperation for Space Standardization (ECSS) for space components compatible with the FE Printed Circuit Board (PCB) design for the foreseen XGIS flight model. The upper value of the energy range was adjusted to 5 MeV. The BE chip included the complete circuitry with logic, event type recognition, timing with data acquisition and parallel readout.
4. **October 2020 MPW:** the first prototype of ORION IV with both FE and BE, with the chips including four channels to serve four pixels onboard a XGIS module were fabricated. This latest ORION design consisted of the ECSS-compliant FE and mixed-signal BE with the complete logic chain, timing, analog and digital data processing channels with the possibility of data configuration and acquisition using both parallel (for laboratory testing purposes) and Serial Peripheral Interface (SPI) protocols.

5 Experimental characterization of ORION IV: four-pixel version

The performance and functionality tests reported here have been performed on the ORION IV prototype manufactured in October 2020. A prototype of the four-pixel version of this ASIC with the complete FE and BE chipsets was tested for the first time at INAF-OAS Bologna, Italy for its functionality and performance. This ASIC prototype board was designed by the National Institute of Astrophysics, within a collaboration between the Observatory of Astrophysics and Space Science of Bologna (OAS) and the Institute of Space Astrophysics and Cosmic Physics of Milan (IASF). As shown in figure 5, two sets of 2×2 monolithic THESEUS SDD matrices with 5 mm pitch are mounted on a test board. With this setup, it is possible to test a model electrically and geometrically representative of the monolithic 8×8 SDD matrices of an XGIS module (figure 6-left). These 5×5 mm^2, 450 µm thick SDDs were wire-bonded (figure 6-right) to the two FE chipsets on two ASIC boards to electrically and geometrically represent the top and bottom Printed Circuit Boards (PCBs) of an XGIS module.

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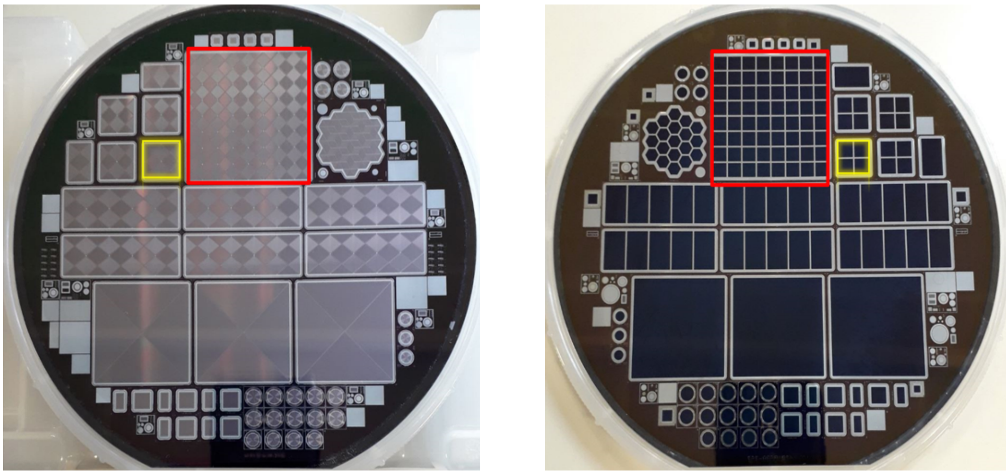

Figure 5. Two sides of a 6-inch wafer with 8×8 monolithic SDD matrices designed for THESEUS XGIS (highlighted in red) and a smaller SDD matrix (2×2) utilized to perform the 4-pixel ORION ASIC Characterization (highlighted in yellow). Left panel: anode and drift electrodes side (n), input side for X rays in XGIS. Right panel: entrance window side (p), input side for the scintillation light. [Courtesy: FBK within INFN-Research Drift for Soft X-Rays (RedSoX) collaboration 2019].

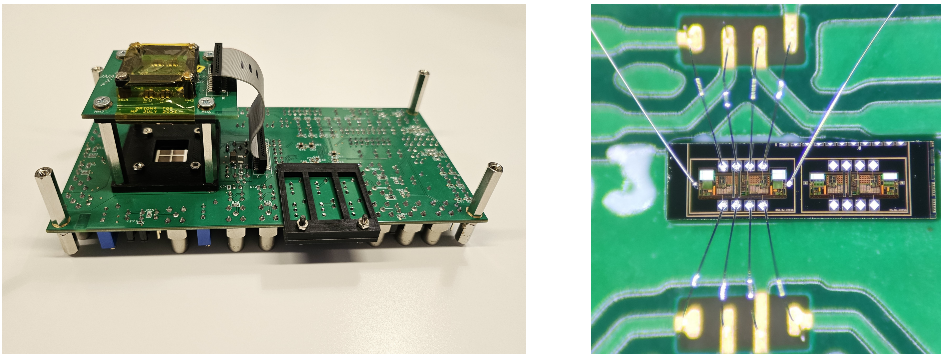

Figure 6. Left Panel: ORION IV prototype board with 2 sets of mounted 2×2 SDD matrices and without CsI:Tl crystals, utilized for experimental measures reported here. Four SDDs are visible on the bottom board, bonded to their respective bottom FE chips, with both the FE and the BE chips mounted on the opposite side of the bottom PCB, while a second 2×2 SDD array is mounted on the topmost mini PCB. Right Panel: wire bondings connecting the preamplifier of one pixel to the corresponding SDDs (Courtesy: FBK Trento).

A study of the ORION analog processors, for the electronic noise performance evaluation without the ORION-BE ADCs, has been performed by the Department of Electronics, Information and Bioengineering at Politecnico di Milano using ^{241}Am and ^{55}Fe calibration sources [9]. The FE chips of this prototype were wire bonded to a 2×2 THESEUS-SDD to electrically represent the 8×8 monolithic THESEUS SDD matrices per XGIS module. Following the analog performance characterization without the ADCs, a single pixel prototype with both the FE and BE chips was investigated for functional behaviour in absence of any SDDs with artificial electrical test pulse inputs for linearity, X/γ discrimination and time tag assignment for the three X, γ-top and γ-bottom processor branches [10].

This work reports the first experimental performance measurements of both X and γ-processing branches with the complete ORION-IV chipset prototype, investigated in terms of spectroscopic energy resolution, electronic noise, linearity and energy ranges for both X and γ processing branches. The spectroscopic analysis of this ASIC board using both artificial electrical impulses and radioactive sources ^{241}Am has been performed, to examine and study the performance of the shaper, stretcher, peak discriminator and Analog to Digital Converter (ADC). The performance measurements are listed in the next subsections.

5.1 Spectroscopic resolution

To measure the behaviour of the four pixel ORION SDD system in a broad energy range, the spectroscopic resolution of the four pixel ORION board bonded to the eight SDDs was analyzed with ^{241}Am and ^{55}Fe sources at room temperatures. The energy spectra for both sources were acquired in stretcher mode for an interval of 60 minutes as sampled output waveforms through the complete FE circuitry and the X and γ processing chains of the BE shown in the right image of figure 4.

The energy resolution of X-processing branch on the 13.7 keV peak of ^{241}Am is 434 eV Full Width at Half-Maximum (FWHM). The γ-processing branch has a spectroscopic performance similar to X processing branch. Figure 7 shows the spectra of ^{241}Am and ^{55}Fe for a representative pixel. Similar performances were observed for the other three pixels.

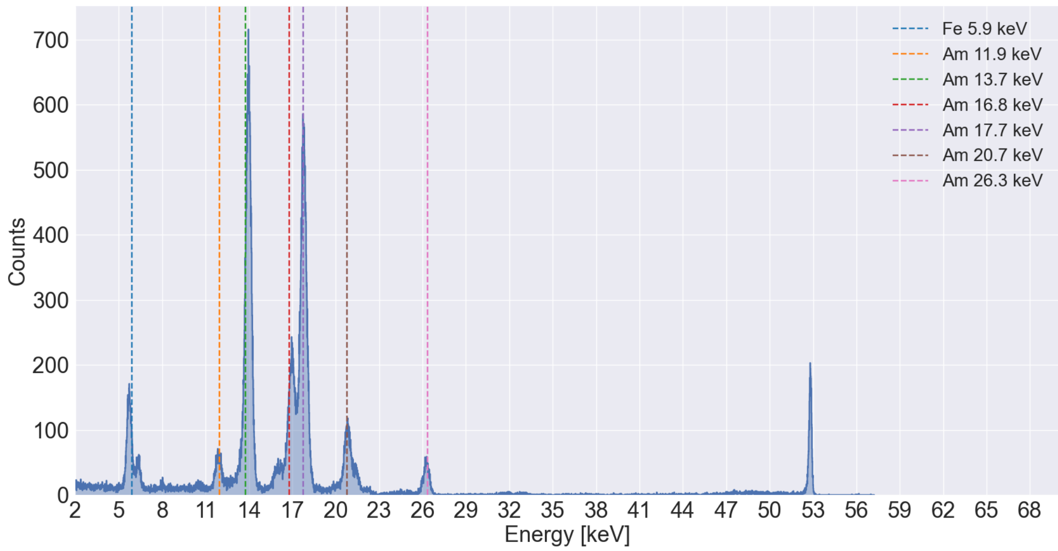

Figure 7. Energy spectra acquired with X-ray processor of the ORION for ^{241}Am and ^{55}Fe sources on a representative pixel of the SDD analyzed utilizing the MESCAL software [14] based on Gaussian least-squares curve fitting with centroid indicated by dotted lines for each peak.

5.2 Electronic noise

Combining the direct calibration with radioactive sources with the response achieved stimulating the FE via the test input, the test capacitance value at the test input stage is evaluated to be about ~18 fF for pixel 0, while other pixels connected to SDDs also demonstrate capacitance values in the range of ~17–18 fF.

For pixel 0, electronic noise corresponding to the 5.9 keV peak of ^{55}Fe was observed to be 44 electrons r.m.s. at room temperature and 30 electrons r.m.s at −20 °C. Values consistent with pixel 0 were also recorded for the other pixels. A minimum theoretical threshold equivalent to five times the noise level is required to be able to successfully discriminate a signal. The minimum theoretical threshold with this assumption is thus calculated to be 0.8 keV at room temperature.

The electronic noise for the γ-top and bottom processing branches for pixel 0 was estimated using again the ^{241}Am spectra processed and acquired from both the γ processors. For this pixel, the equivalent noise charge, on the 59.6 peak of ^{241}Am, is 75 electrons r.m.s. measured separately from both the top and bottom processors at room temperatures. Considering a typical coefficient for photon energy to charge conversion equivalent to 15 e-/keV on each SDD produced by scintillation events in CsI:Tl crystals, that the two γ processor circuits operate independently and that the amplitude peak discrimination of valid events is performed on the sum of γ-top and γ-bottom signals, the minimum detectable γ event in the scintillator (5 times the noise level) is estimated to be ∼ 20 keV at room temperatures.

5.3 Linear operating range

A significant drop in the efficiency of SDDs is observed for incoming energy ranges ≥ 30 keV due to their small 450 μm thickness. On the other hand, the γ-branch of the ORION chipset is required to accommodate charge signals corresponding to 5 MeV photons.

Higher energy ranges are measurable by reconstruction and post-processing of time-coincident signals detected in more than one pixel. Therefore, the XGIS requirements for the maximum energy range for linear operation of each pixel of ORION IV prototype corresponds to roughly 35 keV for the X-processor and up to 5 MeV for the top and bottom γ-processors. Hence, the X and γ processing branches have been designed for input charge ranges corresponding to energy ranges where both the SDDs and scintillators exhibit maximum operation efficiency to meet the XGIS requirements. The X-processor of the ORION SDD system is designed to accommodate an input charge range of 10,000 electrons (corresponding to X-rays of ≤ 30 keV from the top SDD) while the dynamic range of the two γ-processor branches is extended up to an input charge of 90,000 electrons from top and bottom SDDs [9].

A full-range-of-linearity measurement was performed by stimulating the X-ray processor with a test pulse on all the four pixels. Artificial charge pulses with amplitudes corresponding to 10^5 electrons were supplied to the ORION-SDD board. The linearity range of the X-processor observed for the pixel 0 is reported in the left panel of figure 8. Under room temperature conditions, the maximum signal processing capability of the X processing branch is estimated to be linear up to 40 keV. All four pixels demonstrated homogeneous linear energy ranges for the X-processor.

The top and bottom branches of γ-processor were also investigated for the operational linear range with a ^{241}Am source and with the test pulse. As shown in figure 8, the linearity range extends up to 80000 electrons, i.e., the maximum linear energy threshold is estimated to be 5.3 MeV for γ-top processor. Similar ranges were recorded and observed for γ-bottom processors.

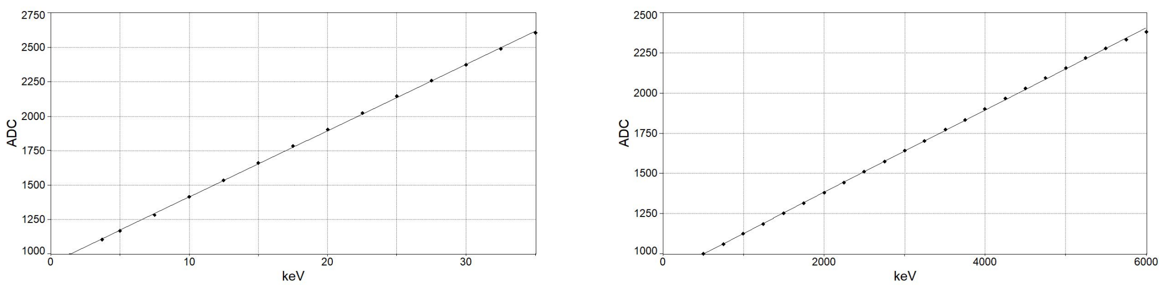

Figure 8. Left panel: linear variation of ADC values with energy from X-processor of Pixel 0. Right panel: linear variation of ADC values with energy from top branch γ processor of Pixel 0.

6 Conclusions and future work

The latest performance measurements recorded for the ORION IV prototype demonstrate the fulfilment of scientific and technical requirements for the optimum operation of four pixels of an XGIS module. Currently, investigation of this ASIC version with the CsI:Tl scintillators in γ-branch for energy and position resolution is ongoing. Future steps may also include Cerium-doped Gadolinium-Aluminium-Gallium Garnet (GAGG:Ce) scintillators that have previously shown to exhibit better performance (e.g., efficiency) than CsI:Tl. With the progress of the THESEUS mission to the next phases of the M7 call of ESA's Cosmic Vision programme, the development of the XGIS modules requires the operation of an 8-channel ORION Back End Chip, which is under revision for fabrication, performance testing and investigation.

Acknowledgments

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