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A Low-Spur and Low-Jitter Fractional-N Digital PLL Based on an Inverse-Constant-Slope DTC and FCW Subtractive Dithering

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***Abstract*—This work presents a low-spur and low-jitter fractional-N digital phase-locked loop (PLL). To reduce the fractional spurs caused by the non-linearity of the digital-to-time converter (DTC), two novel solutions are introduced. First, the inverse-constant-slope DTC achieves high-linearity thanks to its immunity to channel-length-modulation and non-linear parasitic capacitances. Second, the frequency-control-word (FCW) subtractive dithering technique randomizes the quantization-error of the $\Delta\Sigma$ modulator driving the PLL divider ratio without requiring an increased DTC dynamic range and pushing the fractional spurs outside the PLL bandwidth. The prototype, implemented in a 28-nm CMOS process, has an active area of 0.33 mm^2 and dissipates 17.2 mW. At fractional-N channels near 9.25 GHz, the measured in-band fractional spurs and the RMS jitter are below -70 dBc and 77 fs, respectively, leading to a jitter-power figure of merit of -249.9 dB.**

***Index Terms*—Fractional spurs, digital phase-locked loop, dithering, digital-to-time converter, constant-slope, quantization-error**

I. Introduction

HIGH-spectral purity and low-jitter frequency synthesizers are essential for both high data-rate wireless transceivers [1] and frequency-modulated continuous-wave radars [2]. Fractional-N phase-locked-loops (PLLs) can be effective solutions for these applications, thanks to their high frequency resolution and the excellent noise performance achieved by using a digital-to-time converter (DTC) to remove the quantization-error (Q-error) generated by the $\Delta\Sigma$ modulator driving the PLL divider ratio (Fig. 1) [3]–[13]. In DTC-based fractional-N PLLs, the Q-error sequence, $Q[k]$, extracted from the $\Delta\Sigma$ modulator, is fed to the DTC, after applying a least-mean-square (LMS) calibration block tracking the PVT spread of the DTC gain [14]. In this way, the DTC delay ($T_{dtc}[k]$ in Fig. 1) matches the $Q[k]$ pattern, resulting in the PD input time-error being only determined by the PLL random noise sources. This solution unlocks the adoption of a narrow input range PD, such as a bang-bang PD (BBPD) or a sampling PD in digital or analog PLL implementations, respectively, providing a significant jitter-power figure-of-merit (FoM) advantage [7]–[9], [11], [13]–[19]. Unfortunately, in practical implementations, the DTC non-linearity prevents to achieve a perfect Q-error cancellation and a distorted residue of the $Q[k]$ sequence is always present at the PD input (Fig. 2). Since the quantization of the PLL frequency-control-word (FCW) generated by the $\Delta\Sigma$ modulator follows a periodic pattern [20], also the $Q[k]$ residue is periodic, thus causing spurs to appear in the PLL spectrum (Fig. 2). These spurs, also referred to as *fractional spurs*, limit the PLL spectral purity and its integrated jitter.

To reduce their amplitude, two main strategies have been proposed so far in literature. They are summarized in Fig. 3. The first approach aims to modify the $\Delta\Sigma$ modulator to generate a randomized $Q[k]$ sequence with a reduced periodic behavior. Unfortunately, the $Q[k]$ sequence randomization is typically achieved at the cost of increasing its amplitude,

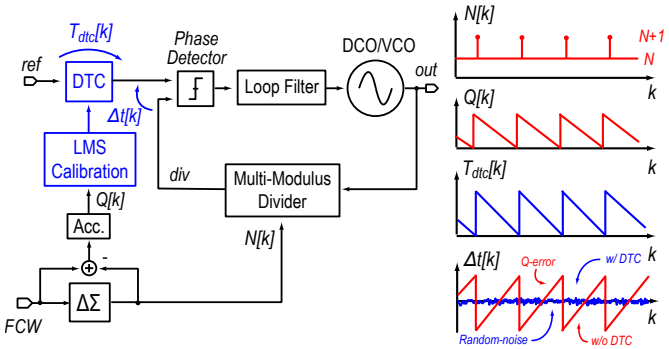

Fig. 1. Operation of the DTC in a fractional-N PLL.

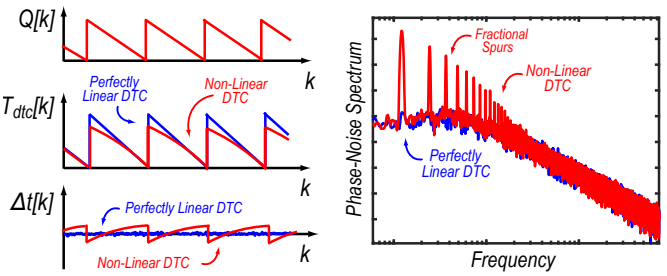

Fig. 2. Impact of the DTC non-linearity and insurgence of fractional spurs in the PLL spectrum.

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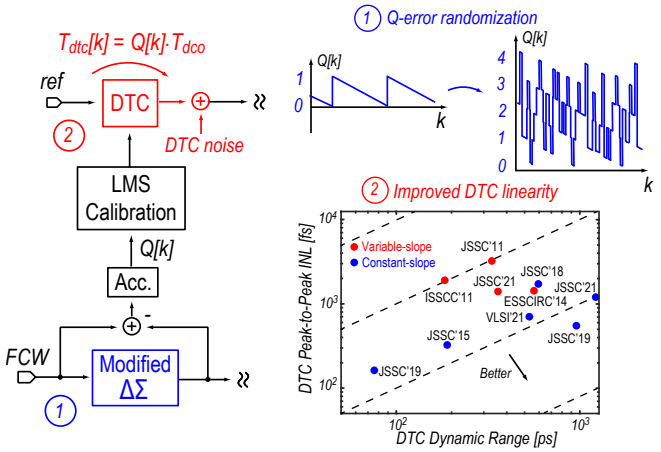


Fig. 3. Fractional spur reduction approaches adopted in DTC-based fractional-N PLLs: (i) modifying the $\Delta\Sigma$ quantizer to produce a randomized Q-error sequence and (ii) improving the DTC linearity at the circuit level.

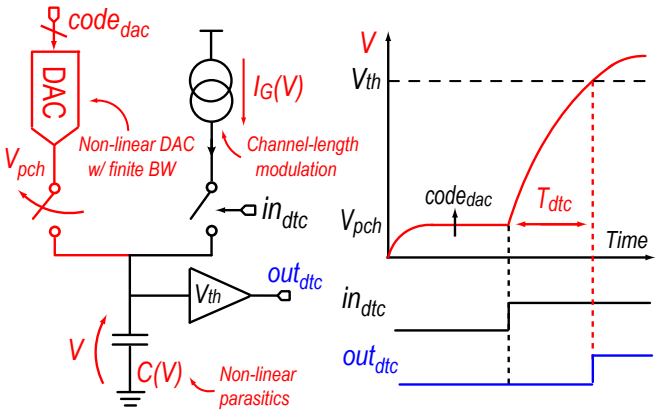


Fig. 4. Conceptual scheme of a CS-DTC, highlighting the sources of non-linearity.

thus requiring a wider DTC dynamic range. For example, the successive requantizer in [21] and the probability-density-shaping $\Delta\Sigma$ modulator in [22] generate a randomized $Q[k]$ sequence producing lower spurs, however they require at least four times the DTC dynamic range with respect to a first-order $\Delta\Sigma$ (MASH-1) modulator. Since the thermal noise of a DTC is proportional to its dynamic range [23], these solutions lead to a degradation of the PLL integrated jitter.

The second approach is to improve the DTC linearity at the circuit level. Figure 3 shows the peak-to-peak integral non-linearity (INL) as a function of the dynamic range (DR) of the variable-slope DTCs (VS-DTCs) [1], [14], [24], [25] and the constant-slope DTCs (CS-DTCs) adopted in state-of-the-art fractional-N PLLs [26]–[31]. Currently, the CS-DTC achieves the best linearity performance, with the stage in [30] reaching the lowest measured INL when normalized to the DTC DR, i.e., 0.12% with INL = 700 fs and DR = 530 ps. Unfortunately, in a CS-DTC, further linearity improvements are limited by the voltage dependence of the parasitic capacitances and the current-generators and by the non-idealities of the digital-to-analog converter (DAC) adopted in the circuit [27], [28].

In this work, we introduce a digital bang-bang PLL (BB-PLL) [32] achieving an integrated jitter (from 10 kHz to 100 MHz and including spurs) below 77 fs and in-band fractional spurs below -70 dBc at near-integer 9.25 GHz fractional-N channels, exploiting: (i) a highly-linear DTC circuit, denoted as *inverse-constant-slope DTC* (ICS-DTC), overcoming the linearity limitations of the CS-DTC and (ii) a Q-error randomization technique, denoted as *FCW subtractive dithering*, which reduces the fractional spurs without requiring a wider DTC dynamic range.

This article is organized as follows. Section II reviews the sources of non-linearity in a CS-DTC, introduces the ICS-DTC topology, highlights the properties leading to its improved linearity and describes its circuit implementation, including also an analysis of the ICS-DTC phase-noise performance. Section III presents the FCW subtractive dithering technique and its operating principle, while Section IV describes the overall BBPLL implementation. Section V reports the measurement results on the fabricated prototype covering the PLL performance and the characterization of the DTC non-linearity. Conclusions are then drawn in Section VI.

II. Inverse-Constant-Slope DTC

A. Limitations of the constant-slope DTC

Figure 4 shows the scheme of a conventional CS-DTC, originally introduced in [26]. A DAC initially charges the capacitor C to a precharge voltage V_{pch}. The DTC input signal then triggers a current-generator to charge the capacitor. When the voltage V across the capacitor exceeds the output buffer threshold, V_{th}, the DTC output signal, out_{dtc}, switches, with a delay T_{dtc} from the input. The DTC delay can be varied by changing V_{pch}. In this way, differently from a VS-DTC, the slope of the buffer input signal remains constant, suppressing the non-linearity caused by the slope-dependent buffer stage delay [26] and therefore achieving superior linearity performance.

The first source of non-linearity in a CS-DTC is the DAC non-linearity and its finite bandwidth. They affect the accuracy and the linearity of the V_{pch} generation, leading to a non-linear dependence of the DTC delay on the DAC input code, $code_{dac}$. A second limitation is given by the channel length modulation of the MOS transistors implementing the current-generator and the non-linear parasitic capacitances of the transistors connected at the DTC capacitor node. These non-idealities cause the generator current, I_G, and the capacitance C to be dependent on the voltage V, i.e., $I_G = I_G(V)$ and $C = C(V)$. The linearity degradation arising from these effects can be highlighted exploiting the capacitor constitutive relationship $I_G(V) = C(V) \cdot dV/dt$[1]. Starting from

$$dt = \frac{C(V)}{I_G(V)} \cdot dV, \tag{1}$$

[1]In this differential equation, the voltage-dependent capacitance term $C(V)$ is defined as $C(V) = {}^{dQ(V)}/_{dV}$, where $Q(V)$ is the total charge stored in the voltage-dependent capacitor [33].

the DTC delay can be derived as

$$T_{dtc} = \int_{V_{pch}}^{V_{th}} \frac{C(V)}{I_G(V)} dV. \quad (2)$$

Since $C(V)/I_G(V)$ depends on V, it follows that T_{dtc} non-linearly depends on V_{pch}. Solutions partially alleviating this dependence include limiting the DAC voltage swing, adopting cascoded current generators and/or reducing the parasitics [28], [30]. However, the effectiveness of these solutions is limited, particularly when implemented in a low-voltage and scaled CMOS technology, where these non-idealities are worse.

B. Inverse-constant-slope DTC concept

To overcome these limitations, the ICS-DTC circuit in Fig. 5 is proposed. The stage is fed with two signals: the DTC input, in_{dtc}, and an auxiliary signal, in_{pch}. The rising edge of in_{pch} precedes the one of in_{dtc} by a controllable time-duration T_{pch}, which can be programmed as an integer multiple of the dco period, i.e.,

$$T_{pch} = sel_{pch} \cdot T_{dco}, \quad (3)$$

where sel_{pch} is an integer number. The generation of the in_{pch} and in_{dtc} signals is perfomed by a dedicated circuit, the *precharge generator*, which will be discussed in detail in Section II-D. The in_{pch} signal triggers a current generator (CG_0), charging the capacitor C with a current I_G for a time duration T_{pch}, reaching a pre-charge voltage level V_{pch} (Fig. 5). At the arrival of the in_{dtc} edge, the current delivered to C is increased by a factor K, turning on an additional current generator (CG_1). When the capacitor voltage V exceeds the threshold of the output buffer V_{th}, the DTC output signal, out_{dtc}, switches with a delay T_{dtc} from in_{dtc}. The DTC delay can be varied by changing T_{pch}, i.e., by selecting a different multiple of T_{dco} acting on sel_{pch}. Since the slope of the voltage signal near V_{th} remains the same even at different T_{pch} values, the non-linear variation of the output buffer delay is suppressed, as in a CS-DTC. At a first sight, the ICS-DTC seems similar to the CS-DTC, as the capacitor is still charged to an initial V_{pch} level before the arrival of the DTC input. However, this is done by controlling the integration time of a current generator rather than using a DAC, thus avoiding the DAC non-idealities. Furthermore, the linearity of the ICS-DTC is immune to channel-length modulation and non-linear parasitic capacitances. To clarify this key property, let us rely on (1) to link T_{pch} to V_{pch} as

$$T_{pch} = \int_{0}^{V_{pch}} \frac{C(V)}{I_G(V)} dV. \quad (4)$$

Then, using a similar equation for the ICS-DTC voltage transient after the arrival of the in_{dtc} edge [i.e., $dt = C(V)/(K \cdot I_G(V)) \cdot dV$], the DTC delay can be written as

$$T_{dtc} = \frac{1}{K} \cdot \int_{V_{pch}}^{V_{th}} \frac{C(V)}{I_G(V)} dV. \quad (5)$$

By combining (4) and (5), it follows

$$K \cdot T_{dtc} + T_{pch} = \int_{0}^{V_{th}} \frac{C(V)}{I_G(V)} dV, \quad (6)$$

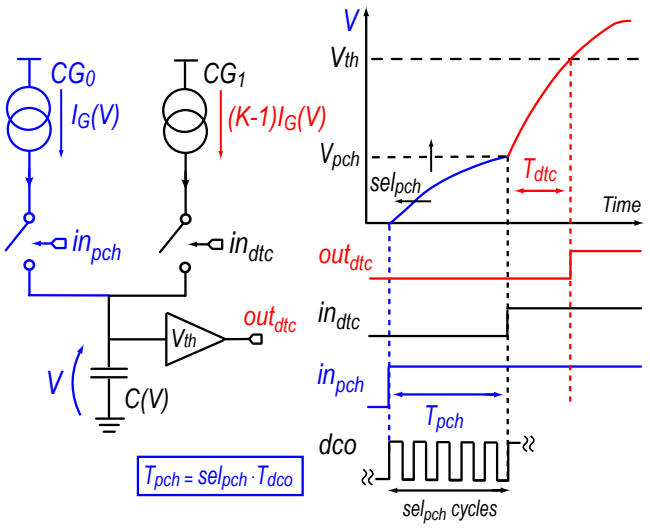


Fig. 5. Conceptual scheme of the proposed ICS-DTC and waveforms of the main signals involved in its operation.

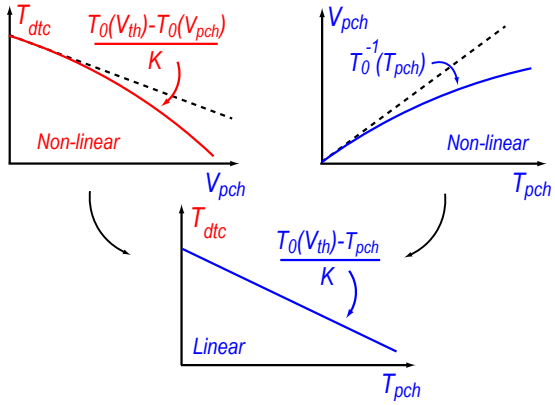


Fig. 6. ICS-DTC built-in predistortion mechanism: compensation of the non-linearities affecting the generation of V_{pch} and T_{dtc}.

which can be finally rewritten as

$$T_{dtc} = \frac{1}{K} \cdot \int_{0}^{V_{th}} \frac{C(V)}{I_G(V)} dV - \frac{T_{pch}}{K}. \quad (7)$$

From (7) it turns out that T_{dtc} features a linear dependence on T_{pch}, with a slope $1/K$. The sole effect of channel-length modulation and non-linear parasitics is to modify the integral expression in the right side of (7). Since the latter is just a constant term, as the integration bounds are fixed and do not depend on the DTC delay, the linear dependence on T_{pch} is not affected. For this reason, the ICS-DTC is expected to achieve superior linearity performance with respect to a CS-DTC, provided that T_{pch} is generated with high-linearity. However, this is not an issue, since T_{pch} is generated as a multiple of the dco period, which provides an accurate and precise *time reference* naturally embedded in the PLL system.

C. A built-in predistortion mechanism

In the following paragraphs, more insights into the ICS-DTC operation are given, leading to a more intuitive expla-

nation of its intrinsic linearity. To this aim let us define the non-linear function

$$T_0(V) = \int_0^V \frac{C(V)}{I_G(V)} dV \tag{8}$$

to express (5) as

$$T_{dtc} = \frac{T_0(V_{th}) - T_0(V_{pch})}{K}. \tag{9}$$

On the other hand, since $T_{pch} = T_0(V_{pch})$ from (4), it follows

$$V_{pch} = T_0^{-1}(T_{pch}), \tag{10}$$

where T_0^{-1} is the inverse function of T_0. Equations (9) and (10) highlight that T_{dtc} and V_{pch} are given by non-linear functions of V_{pch} and T_{pch}, respectively, which are graphically illustrated in Fig. 6. However, when substituting (10) in (9), the outcome is a perfectly linear function of T_{pch}, i.e.,

$$T_{dtc} = \frac{T_0(V_{th}) - T_0(T_0^{-1}(T_{pch}))}{K} = \frac{T_0(V_{th}) - T_{pch}}{K}. \tag{11}$$

The result coincides with (7), however, in the present form, it highlights that linearity is achieved by compensation between the non-linear dependence $T_0(.)$ linking the delay T_{dtc} to V_{pch} and the dependence $T_0^{-1}(.)$ linking V_{pch} to T_{pch} (Fig. 6). The ICS-DTC linearity therefore relies on a *built-in predistortion mechanism*, arising from the non-linear generation of V_{pch} through the integration of the CG_0 current over the capacitor. For this reason, the proposed DTC was denoted as *inverse-constant-slope* DTC.

D. Precharge generator

Figure 7(a) shows the precharge generator (PG) circuit, producing the signals in_{dtc} and in_{pch}. It is placed at the output of the PLL multi-modulus divider (MMD) and generates in_{dtc} as the output of a chain of 11 flip-flops (FFs), clocked by the dco signal. To generate in_{pch}, the first 9 FF outputs are multiplexed through the sel_{pch} control signal. By varying sel_{pch}, the in_{pch} rising edge can be therefore shifted over time with a T_{dco} resolution (Fig. 7(b)). Note that the delays of the different multiplexer paths in Fig. 7(a) are affected by circuit mismatches, thus making the multiplexer delay to feature a non-linear dependence on sel_{pch}. To solve this issue, an auxiliary FF is added at the multiplexer output (Fig. 7(a)). The latter acts as a retiming stage, synchronizing the multiplexer output signal to the dco rising edge, thus canceling the mismatches between the different multiplexer path delays[2]. A second FF, sampling the auxiliary FF output with the dco falling edge, and a multiplexer driven by the additional control signal mux_{pch} are used to improve the resolution in shifting the in_{pch} edge to $0.5 \cdot T_{dco}$ (Fig. 7(b)). To this aim the dco signal should have a 50% duty cycle, which is obtained, equivalently, by compensating the dco duty cycles errors with the LMS algorithm later discussed in Section IV.

The resulting dependence of T_{pch} on sel_{pch} and mux_{pch}

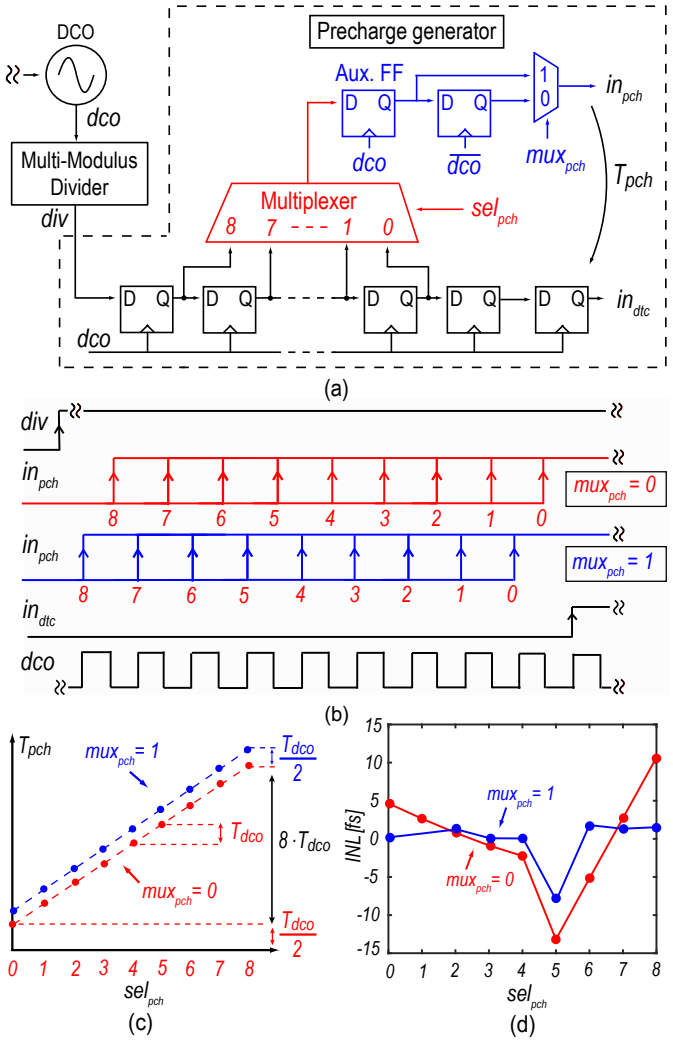


Fig. 7. Precharge generator: (a) block diagram, (b) waveform of the in_{pch} signal for $mux_{pch} = 0$ and $mux_{pch} = 1$ at different sel_{pch} values, (c) T_{pch} dependence on mux_{pch} and sel_{pch} and (d) INL of the implemented PG circuit obtained from post-layout simulations.

is linear, with a dynamic range equal to $8.5 \cdot T_{dco}$ (Fig. 7(c)). Note that only the last stage of the FF chain and the two FFs driving the multiplexer generating in_{pch} affect the PG noise performance, since the outputs of all the other blocks are resampled by at least a FF stage, thus eliminating their jitter contribution [35]. For this reason, the PG design is highly relaxed. To limit power consumption, the FFs were designed in TSPC logic, with small size devices for the non critical stages. The PG consumes less than 500 μW, with an RMS integrated jitter below 70 fs[3]. Being well below the ICS-DTC integrated jitter, the noise of the PG is not an issue[4]. Note that all the PG internal signals are synchronous with the DCO edge (apart from the small delay of the circuit stages), therefore all the PG signal paths correctly settle before being resampled

[2]The operation of the auxiliary FF is similar to the one of the retiming stage adopted in typical MMD circuits. In this case, a FF resamples the MMD output signal with the DCO rising edge to suppress the dependence of the MMD propagation delay on the divider ratio in fractional-N mode [34].

[3]This worst-case value refers to the SS corner condition.

[4]Note that, since a retiming stage clocked with the DCO edge is anyway needed at the MMD output in a fractional-N PLL [34], [35], a similar noise contribution would be present even in a conventional PLL design.

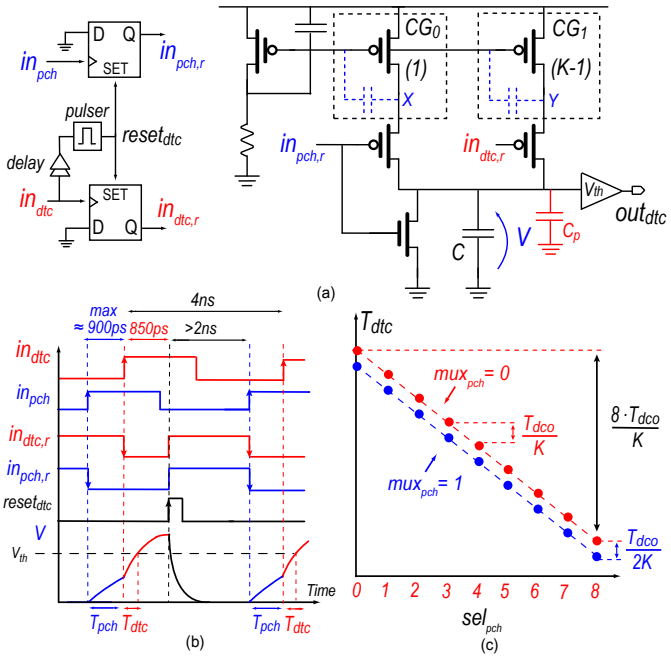


Fig. 8. ICS-DTC implementation: (a) circuit schematic, (b) waveforms of the main signals involved during its operation and (c) DTC delay dependence on the PG control signals.

by the FF stages, thus avoiding any metastability issue[5] [37]. Figure 7(d) shows the INL of the implemented PG, for both $mux_{pch} = 0$ and $mux_{pch} = 1$, which was simulated with a dco signal at 10 GHz and a div signal at 250 MHz, i.e., the center of the dco tuning range and the reference frequency in this design, respectively. The PG peak-to-peak INL is very small, i.e., below 25 fs in both cases, and it is mainly caused by layout parasitic effects. On top of that, the T_{pch} non-linearity is scaled down by a factor of K when referred to the generated ICS-DTC delay, as follows from (7), thus being negligible in practice[6].

E. ICS-DTC circuit implementation

Figure 8(a) shows the ICS-DTC circuit. It consists of two current generators, biased by a current mirror and implemented with single PMOS transistors. A capacitor of about 10 pF, connected between the 0.9V supply and the PMOS gates, stabilizes the generator currents across supply disturbances. The ratio K is set by the geometric ratio between the PMOS widths. Note that, based on (7), any mismatch in the K value only affects the DTC gain, without degrading the DTC linearity. On the other hand, since the DTC gain is calibrated in background with an LMS algorithm (discussed later in Section IV), the gain variations of the DTC are not an issue. The adoption of the simple current generator architecture in Fig. 8(a) is only possible thanks to the ICS-DTC immunity to the voltage dependence of the generator currents, highly relaxing the DTC design and making it a suitable candidate, differently from conventional CS-DTC circuits, even for ultra low-voltage and deeply scaled CMOS processes. The PMOS transitors at the drain nodes implement the switches turning on the generators, while the NMOS resets the capacitor before the next DTC inputs are applied. Two FFs, a delay and a pulser stage generate the $in_{dtc,r}$ and $in_{pch,r}$ signals driving the PMOS switches and the NMOS with the timing shown in Fig. 8(b). CG_0 and CG_1 are switched-on upon the in_{pch} and in_{dtc} rising edges, respectively, and turned-off with a delayed version of in_{dtc}, also used to reset the capacitor. A delay of about 850 ps was chosen to fully charge the capacitor. Considering the 4 ns period of the in_{dtc} signal and the maximum T_{pch} value of $9 \cdot T_{dco} \approx 900$ ps (at 10 GHz DCO frequency) provided by the PG in this design, this guarantees more than 2 ns for the capacitor to fully discharge before the application of the next in_{pch} edge, thus avoiding memory effects due to previously synthesized DTC delays. The output buffer, implemented with two CMOS inverters, was sized with $V_{th} \approx 0.5$ V. The DTC delay dependence on the PG control codes, sel_{pch} and mux_{pch}, is illustrated in Fig. 8(c). The DTC dynamic range is equal to $8.5 \cdot T_{dco}/K$, and the DTC resolution is $T_{dco}/(2K)$. The value of K was set to 3.5 to target a DTC dynamic range of $2.4 \cdot T_{dco}$, enough to handle with margins the Q-error generated by the MASH 1-1 $\Delta\Sigma$ modulator driving the MMD in this design. With this K value, the ICS-DTC resolution is about 15 ps (at a DCO frequency $\approx$ 10 GHz). Section IV discusses how to push the equivalent DTC resolution to hundreds of femtoseconds as required by the PLL system.

Figure 9(a) shows the simulated delay curve and the INL profile of the implemented ICS-DTC. In this simulation, T_{pch} was swept from 0 to about 1 ns, with high-resolution[7]. The peak-to-peak INL of the DTC is very small, i.e., only 75fs. The residual non-linearity of the ICS-DTC is mainly due to dynamic effects such as charge sharing, charge injection and transient behaviors occuring when turning on the current generators which are not taken into account in the static non-linearity analysis carried out in Section II-B and II-C.

For instance, the above analysis does not include the fact that the parasitic capacitance contribution to the DTC capacitor load given by the CG_1 branch, highlighted as C_p in Fig. 8, is time-variant. Indeed, before and after the rising edge of in_{dtc}, the value of C_p changes, depending on the PMOS switch in the CG_1 branch being off or on. Furthermore, when turned-off, CG_1 contributes some leakage current, which sum-up to the CG_0 current charging the capacitor, not accounted in the above analysis. However, as discussed later in Section II-F, to improve the DTC phase-noise, a large fixed capacitor of few pF is placed at the DTC capacitor node, while CG_0 is sized to carry a current in the order of several hundreds of μA. As a result, the contribution of the time-variant parasitic capacitances and the leakage currents is less relevant.

Another effect is the non-instantaneous switch-on of the

[5]To ensure that even the *div* signal is synchronous with the DCO rising edge, the MMD comprises an internal retiming stage, as it is typically done in MMD circuits [34], [35], together with the metastability avoidance technique discussed in [36].

[6]For the same reason, the impact of the in_{pch} signal jitter on the DTC delay is also scaled down by K.

[7]Even if the PG driving the DTC generates discrete values of T_{pch} with a $T_{dco}/2$ resolution, this allows to better characterize the DTC INL profile.

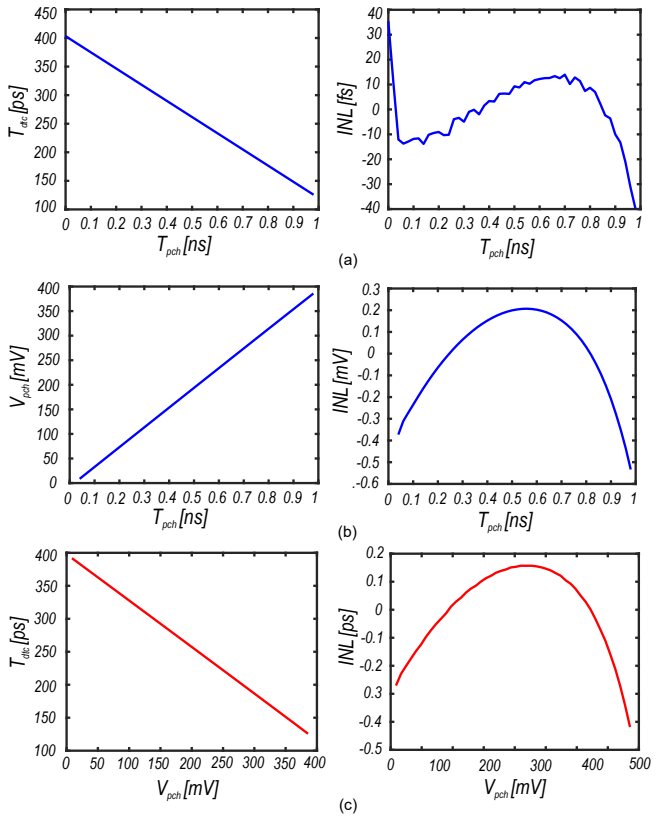


Fig. 9. Post-layout ICS-DTC circuit simulations: (a) DTC delay curve and resulting INL profile, (b) dependence of V_{pch} on T_{pch} and corresponding INL and (c) dependence of T_{dtc} on V_{pch} and corresponding INL.

current generators. When the PMOS switches are enabled, the voltages at the drain nodes of the current generators, denoted as X and Y in Fig. 8(a), are discharged while CG_0 and CG_1 move from the ohmic to the saturation region. This discharge transient has a time constant depending on the parasitic capacitances at those nodes, mainly determined by the CG_0 and CG_1 parasitics (highlighted in dashed lines in Fig. 8(a)), which limits the settling time of the generators' currents after the switch-on. Furthermore, the current flowing through these parasitics induces a disturbance on the bias voltage at the PMOS gates, temporarily perturbing the CG_0 and CG_1 currents. As a result, a significant portion of the residual ICS-DTC non-linearity arises at small T_{pch} values, i.e., $T_{pch} < 50$ ps (Fig. 9(a)), where the in_{pch} and in_{dtc} rising edges are so close that the CG_0 current does not have enough time to fully settle before CG_1 is turned on. A similar effect may also occur at small T_{dtc} values, where the CG_1 current does not have sufficient time to settle before the capacitor voltage crosses the threshold of the buffer stage and the DTC output signal switches. However, note that differently from CS-DTC circuits, where the channel length of the generators should be maximized to reduce channel length modulation, in the ICS-DTC, a much smaller length can be adopted, thanks to its immunity to the voltage dependence of the generators' currents. This allows to reduce the size of CG_0 and CG_1 and, in turn, the parasitic capacitances at the X and Y nodes, speeding up the turn-on transient of the generators and lowering the bias voltage disturbances. As a result, these transient effects have a modest impact on the overall ICS-DTC INL, which remains small. Furthermore, note that the implemented PG circuit provides a non-zero minimum T_{pch} value equal to $T_{dco}/2 \approx 50$ ps (at 10 GHz DCO frequency) (Fig. 7(c)). This always guarantees a minimum 50 ps time difference between the arrival of in_{pch} and in_{dtc}, thus giving the CG_0 current an extra time to settle before CG_1 is switched on. On the other hand, designing the ICS-DTC to achieve a non-zero minimum T_{dtc} value, e.g., about 120 ps in this design (see Fig. 9(a)), gives the CG_1 current a sufficient time to settle before the capacitor voltage crosses the output buffer threshold. Excluding the T_{pch} values less than 50 ps in Fig. 9(a), the resulting peak-to-peak DTC INL is approximately 55 fs, corresponding to 0.021% of the about 266 ps DTC delay swing[8].

The high-linearity performance achieved by the implemented ICS-DTC circuit is a result of the built-in predistortion mechanism discussed in Section II-C. To illustrate this point, Fig. 9(b)-(c) shows the simulated variation of the precharge voltage V_{pch} as a function of T_{pch} and the DTC delay curve expressed as a function of V_{pch}. The same figures also depict the corresponding INL profiles of these curves[9]. If the V_{pch} dependence on T_{pch} in Fig. 9(b) were linear, the INL of the ICS-DTC would be equal to the one of the T_{dtc} vs V_{pch} curve in Fig. 9(c), i.e., about 580 fs, corresponding to 0.215% of the DTC delay swing. The latter is mainly determined by the voltage dependence of the generator currents, which becomes more severe at large V_{pch} values (i.e., $V_{pch} > 300$ mV). However, the V_{pch} vs. T_{pch} curve is non-linear, due to the integration of the CG_0 current over the capacitor, with a INL profile similar to the one of the T_{dtc} vs. V_{pch} curve (Fig. 9(b)) and a comparable INL percentage when normalized to the V_{pch} variation, i.e., a peak-to-peak INL of 740 μV, which corresponds to 0.196% of the about 380mV voltage swing. As a result, thanks to the composition of the two similar non-linearity profiles, the overall ICS-DTC delay curve in Fig. 9(a) features a significantly lower INL, which is only limited by the dynamic effects discussed above.

To quantify the impact of circuit mismatches on the ICS-DTC linearity, Fig. 10(a) shows the INL profiles of the DTC obtained from Montecarlo simulations. The peak-to-peak DTC INL varies from 45 fs to about 70 fs across Montecarlo iterations (Fig. 10(b)), i.e., less than 20fs variation from the nominal value, and the INL shape remains substantially unchanged, as evident from Fig. 10(a). This resilience to circuit mismatches is expected, since the ICS-DTC linearity properties only rely on the hypothesis that the ratio $K-1$ between the currents of CG_1 and CG_0 is a constant, i.e., it is not voltage dependent. Due to circuit mismatches, the CG_0 and

[8]Note that this is a worst case analysis, since during the PLL operation only a $2 \cdot T_{dco}$ delay range (e.g., ≈ 200 ps at 10 GHz DCO frequency) would be actually used by the DTC to cancel the Q-error generated by the MASH1-1 modulator in this design.

[9]In these simulations, trying as much as possible to isolate only the static effects leading to the DTC non-linearities, only the T_{pch} values larger than 50 ps were considered.

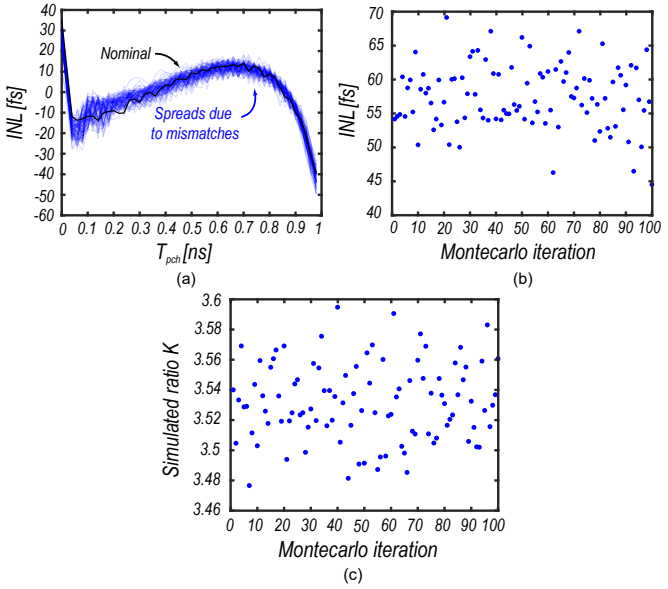


Fig. 10. Post-layout ICS-DTC Montecarlo simulations accounting for the impact of circuit mismatches: (a) DTC INL profile, (b) peak-to-peak DTC INL (exluding the T_{pch} values less than 50 ps) and (c) simulated K ratio over 100 Montecarlo iterations.

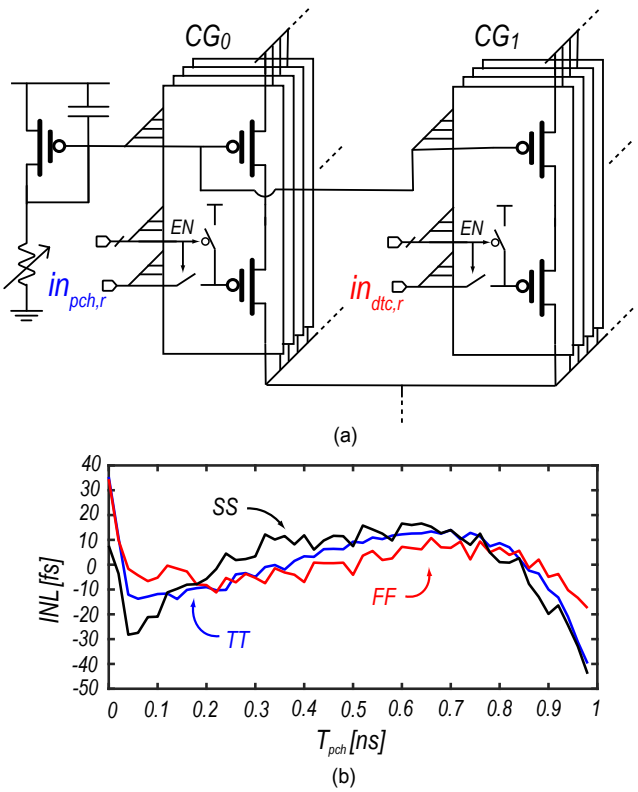


Fig. 11. ICS-DTC & process corners: (a) detailed ICS-DTC circuit implementation including the tuning scheme for controlling the generators' currents over process corners and (b) simulated DTC INL across SS, FF and TT process corner conditions.

CG_1 currents drift away from their nominal values, however, the only effect is that the actual value of K would be slightly different. As discussed before, a variation of K only affects the DTC gain but does not degrade the DTC linearity (see Eq. (7)). Figure 10(c) shows the simulated value of K across Montecarlo iterations, which, due to circuit mismathces, varies by less than 3% from the nominal value.

Since in this design the current generators of the ICS-DTC are biased by a simple resistive current mirror, their currents are sensitive to process corners and may experience large variations when moving from FF to SS corners (e.g., more than a factor of 2). For this reason, in this design, the CG_0 and CG_1 currents can be adjusted so that to achieve the same conditions across different corner conditions, while maintaining the same $K-1$ ratio between them. This was done by implementing CG_0 and CG_1 as the parallel of an integer number of an unit current generator cell, as shown in Fig. 11(a). The number of unit cells actually connected to the $in_{pch,r}$ and the $in_{dtc,r}$ signals depends on the EN control of the individual cells. When $EN=1$, the cell is connected, while $EN=0$ forces the gate of the PMOS switch at the supply voltage, disconnecting and turning-off the cell. In this way, the CG_0 and CG_1 currents can be tuned, while the K value is kept constant by maintaining the same ratio between the number of enabled cells in the CG_1 and the CG_0 branches, respectively. In addition, also the current of the bias circuit is made tunable through a variable resistance in the bias branch (see Fig. 11(a)). Note that also VS-DTC and CS-DTC circuits need a tuning across process corners, as discussed in [1], [8], [26], since in those cases the DTC dynamic range is inversely proportional to the current flowing in the capacitor load, thus being strongly sensitive to process variations. Figure 11(b) shows the simulated ICS-DTC INL across different process corner conditions, i.e., FF, SS and TT. Note that the DTC INL profiles and the INL peak-to-peak values are similar. Excluding the T_{pch} values below 50 ps, the peak-to-peak DTC INL remains always below 65 fs.

F. ICS-DTC noise performance

In a DTC-based fractional-N PLL, the DTC random jitter directly affects the PLL in-band phase-noise. Therefore it is useful to analyze the ICS-DTC phase-noise performance and the noise-power trade-offs arising in the DTC design. Figure 12 highlights the main sources of random jitter in the ICS-DTC, namely, the current noise of CG_0, CG_1 and the PMOS in the bias branch, denoted as CG_b, including both white and flicker contributions[10]. The latter are integrated over the capacitor C during the DTC output signal transition [38]; the noise of CG_0 and CG_b are integrated for a time duration equal to $T_{pch}+T_{dtc}$, while the CG_1 noise is integrated only for a T_{dtc} time interval (see Fig. 12). Following the noise analysis approach in [39], Appendix A derives the ICS-DTC phase-noise floor caused by the combination of the CG_0 and CG_1 white noise as

$$\mathcal{L}_{w,G} = 4\pi^2 F_r \cdot 2kT\gamma \frac{g_m}{I_G} \cdot \frac{T_{dtc,m}^2}{C \cdot V_{th}} \tag{12}$$

[10]The current noise of the PMOS switches is negligible since, when turned on, their currents are forced equal to the ones of either CG_0 or CG_1.

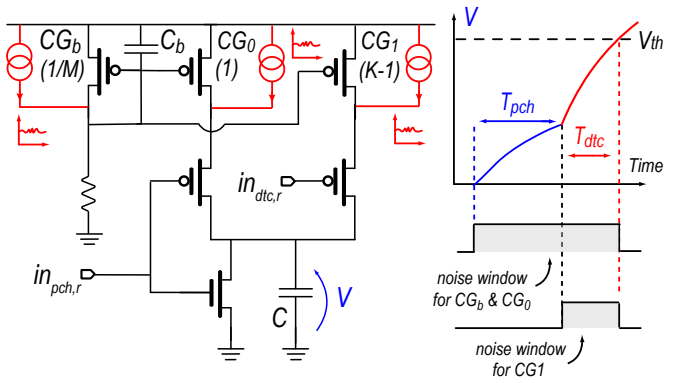


Fig. 12. Main sources of random jitter in the ICS-DTC and integration windows for the different noise sources.

where F_r is the reference frequency, $T_{dtc,m}$ is the maximum DTC delay (i.e., the DTC delay when $T_{pch} = 0$), k is the Boltzmann constant, γ is the noise excess factor, T is the temperature and g_m/I_G is the ratio between the transconductance and the current of CG_0. From (12), it turns out that reducing the maximum DTC delay $T_{dtc,m}$ and the g_m/I_G ratio, i.e., increasing the overdrive voltage V_{ov} of the current generators[11], results in a lower the DTC phase-noise. However, the supply voltage limits the maximum achievable V_{ov}. Furthermore, in a fractional-N PLL, the DTC should achieve a minimum dynamic range set by the order of the $\Delta\Sigma$ modulator driving the MMD, e.g., $2 \cdot T_{dco}$ for the MASH1-1 adopted in our design, therefore setting a limitation on $T_{dtc,m}$. On the other hand, it follows from (12) that scaling up the capacitor load C and the current I_G by the same factor, while keeping the same ratio $K-1$ between the CG_1 and CG_0 currents, allows to achieve a lower DTC phase-noise at the cost of a higher power consumption[12], while not affecting the DTC delay (see (7)). A similar trade-off is also met when designing a VS-DTC or a CS-DTC [23]. In this design, to lower the DTC phase-noise at the expense of power consumption, the capacitor load C is increased to about 1.8 pF by loading the DTC with a fixed metal-on-metal (MOM) capacitor, while I_G was set to approximately 700 μA.

To limit the power consumption of the ICS-DTC, the size of CG_b was set to be M times smaller than CG_0 (see Fig. 12), resulting in a bias current equal to I_G/M. This choice leads to an amplification by a factor M^2 of the CG_b current noise when mirrored to the CG_0 and CG_1 branches, before being integrated on the capacitor C[13]. However, the presence of the large capacitor C_b placed at the gate nodes helps to filter-out this noise thus reducing its impact on the DTC phase-noise. Appendix B shows that the DTC phase-noise induced by the white-current noise of CG_b is given by

$$\mathcal{L}_{w,b}(f) = \mathcal{L}_{w,G} \cdot \frac{K \cdot M \cdot T_{dtc,m} \cdot F_r}{(1 + \frac{f^2}{f_p^2})}, \tag{13}$$

[11]For a transistor in strong-inversion, neglecting higher order effects, the ratio g_m/I_G is inversely proportional to V_{ov}.

[12]Since the capacitor C is charged and discharged to the supply voltage V_{dd} at each clock cycle, it dissipates a power equal to $P = C \cdot V_{dd}^2 \cdot F_r$.

[13]Note that the CG_b current noise already undergoes a $(K-1)^2$ amplification when mirrored to the CG_1 branch.

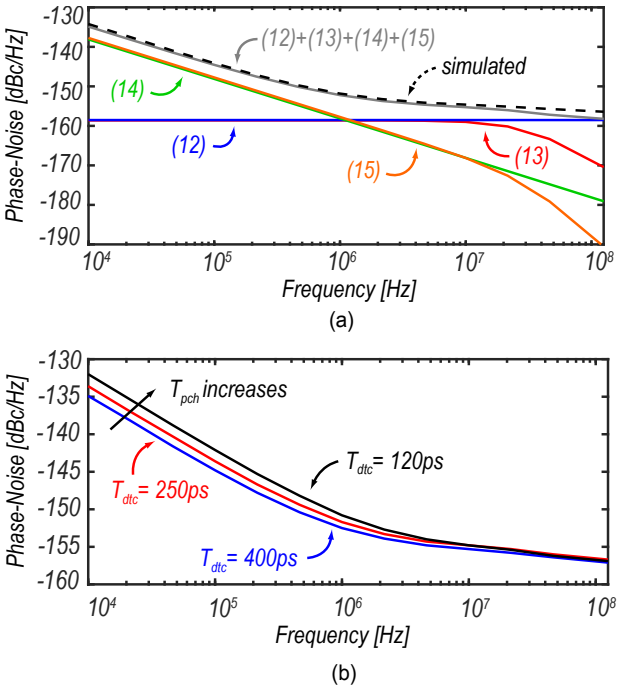


Fig. 13. ICS-DTC phase-noise simulations: (a) comparison between theoretical and simulated ICS-DTC phase-noise for $T_{dtc} = 400$ ps and (b) simulated ICS-DTC phase-noise spectra at different T_{dtc} values.

where f is the offset frequency, $f_p = g_{m,b}/(2\pi C_b)$ is the pole introduced by the capacitor C_b and $g_{m,b}$ is the transconductance of CG_b. As expected, (13) has a low-pass filter shape and, more importantly, at low-frequencies, i.e., $f \ll f_p$, it is a scaled version of (12). The scaling factor contains the term $T_{dtc,m} \cdot F_r \ll 1$ that helps to reduce the phase-noise[14], while the term $K \cdot M$ leads to a noise amplification, reflecting the discussion made above. In our design, the bias circuit was sized with a current of about 250 μA, i.e., $M \approx 2.8$, while the pole frequency f_p is around 30 MHz. With these values, (13) gives $\mathcal{L}_{w,b}(0) \approx \mathcal{L}_{w,G}$, making the bias circuit and the current generators contributing almost equally to the DTC phase-noise floor.

For what concerns the impact of the flicker sources, Appendix C derives the contribution of the phase-noise due to the combination of the CG_0 and CG_1 flicker current noise. It is

$$\mathcal{L}_{f_n,G}(f) = \mathcal{L}_{w,G} \cdot \frac{f_n \cdot T_{dtc,m} \cdot F_r \cdot [1 + (K-1)(1 - \frac{T_{dtc}}{T_{dtc,m}})^2]}{f}, \tag{14}$$

while the contribution of CG_b is

$$\mathcal{L}_{f_n,b}(f) = \mathcal{L}_{w,b}(f) \cdot \frac{f_{n,b}}{f}, \tag{15}$$

where f_n and $f_{n,b}$ are the flicker corner frequencies of the CG_0/CG_1 and the CG_b current noise, respectively. From (14) and (15), we can observe that, once $\mathcal{L}_{w,G}$ and $\mathcal{L}_{w,b}(f)$ are

[14]This is because the reference period, i.e., 4 ns, is much larger than the maximum DTC delay $T_{dtc,m} \approx 400$ ps, as shown in Fig. 9(a).

set, to lower the DTC flicker noise, the corner frequencies f_n and $f_{n,b}$ should be reduced, for instance using non-minimum channel lengths when sizing CG_0, CG_1 and CG_b. Furthermore, the adoption of a DTC architecture based on PMOS rather than NMOS, as in the presented design, should be preferred, since PMOS typically exhibit a lower flicker noise corner frequency [40].

Figure 13(a) shows the simulated ICS-DTC phase-noise when $T_{dtc} = 120$ ps, i.e., at $T_{pch} = 0$ (see Fig. 9(a)). The same plot also shows the theoretical phase-noise predictions from (12), (13), (14) and (15), demonstrating a good agreement between simulations and theory. In these equations, the values of g_m/I_G, f_n and $f_{n,b}$ were obtained from simulations. Given the channel lengths of 300 nm and 100 nm for CG_b and CG_0/CG_1 used in this design, respectively, it turns out that $f_{n,b} \approx 1$ MHz and $f_n \approx 11$ MHz, while $g_m/I_G \approx 10$ V^{-1}. The simulated ICS-DTC phase-noise at 1 MHz offset frequency is about -152.5 dBc/Hz, and the contributions of the white and flicker sources at 1 MHz is approximately equal, as shown in Fig. 13(a). Figure 13(b) shows, instead, the simulated ICS-DTC phase-noise across different T_{dtc} values, i.e., when varying T_{pch}. Note that, at lower T_{dtc} values, the DTC flicker noise increases and the phase-noise at 1 MHz offset reaches a maximum of about -151 dBc/Hz at the minimum T_{dtc} value of about 120 ps (i.e., $T_{pch} = 1$ ns). This is in agreement with (14), which predicts an higher flicker noise contribution from CG_0 and CG_1 at lower T_{dtc} values, i.e., at higher T_{pch}[15]. The DTC random jitter, integrated from 10 kHz up to the 125 MHz Nyquist band, varies from 158 fs to 170 fs when moving from the maximum to the minimum DTC delay. The power consumption of the ICS-DTC is about 900 μW, leading to a jitter-power figure-of-merit of about -255.8 dB. Including the power dissipation of the PG, the jitter-power figure-of-merit (FoM) of the ICS-DTC is about -254 dB[16]. This is in line with the prior-art CS-DTC and VS-DTC designs in [11], [24], [26], [28], achieving a jitter-power FoM in the range from -256 dB to -251 dB.

III. FCW SUBTRACTIVE DITHERING

As discussed in Section I, fractional spurs arise from the periodicity of the Q-error sequence generated by the $\Delta\Sigma$ modulator. These spurs are more intense at near-integer channels, i.e., when the fractional part of the FCW, FCW_{frac}, is close to 0. This is because, being the period of the $Q[k]$ sequence equal to $1/FCW_{frac}$ cycles [20], the time-error perturbation caused by the DTC non-linearity has a long period (see Fig. 14(a)), causing the spurs to be located at low-frequency, thus falling within the PLL bandwidth without being filtered by the PLL low-pass response. Therefore, a technique to reduce the spurs is to avoid the long periodicities of the Q-error pattern occurring at near-integer channels. This can be achieved, in principle, by subtracting 0.5 from the FCW when close to an integer (Fig. 14(b)). In this way, FCW_{frac} is increased, thus reducing the period of the $Q[k]$ sequence and of the corresponding time-error perturbation (Fig. 14(b)), so that the fractional spurs are pushed at high-frequency, falling out-of-band where they are filtered-out by the PLL response. The key advantage of this approach is that it does not increase the amplitude of the $Q[k]$ sequence, since the reduction of the fractional spurs is achieved by speeding up the pattern of the Q-error rather than directly randomizing it[17], therefore it does not require to increase the DTC dynamic range, thus avoiding to worsen the PLL integrated jitter[18].

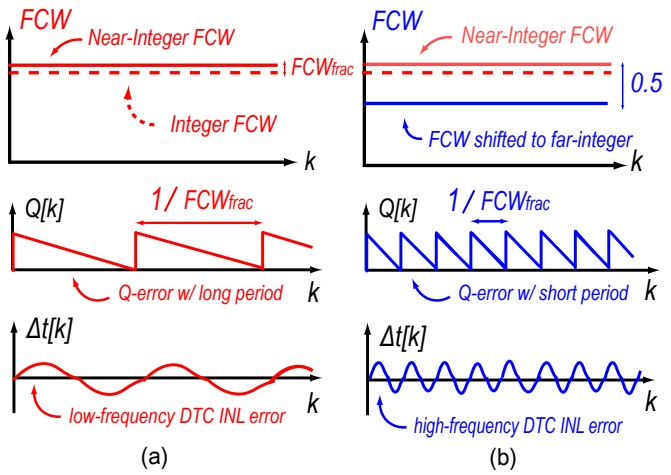


Fig. 14. Illustration of the effects of subtracting 0.5 from the FCW at near-integer channels: the pattern of the $Q[k]$ sequence and the time-error induced by the DTC non-linearity feature a lower periodicity, leading to out-of-band fractional spurs.

Figure 15 shows the concept implementation in a generic DTC-based fractional-N PLL. Instead of adding a static 0.5 offset to the FCW, the FCW dithering block in Fig. 15(a)-top randomly subtracts 0.5 from the FCW based on the output of an uniform 1b pseudo-random number generator (PRNG), i.e., 0.5 is subtracted only when the PRNG output is equal to 1. In this way, the average of the FCW is still shifted from the near-integer value, in this case by 0.25 rather than 0.5, while, at the same time, the randomization of the FCW acts as a dithering signal which helps to scramble the pattern of the $Q[k]$ sequence and randomize the time-error induced by the DTC non-linearity (Fig. 15(a)-bottom left). However, this dithering scheme has some issues to be solved. For a locked PLL, the FCW is expected to be a constant, therefore anytime the FCW value is dithered by the PRNG, the MMD produces a wrong division ratio, and injects a time-error at the PD input. In practice, anytime 0.5 is subtracted from the FCW, a time-error equal to $0.5 \cdot T_{dco}$ is injected and

[15]This is intuitive, since the flicker noise can be thought as a low-frequency perturbation and therefore its effect is expected to be maximized when integrated for a long time, i.e., when T_{pch} is maximum.

[16]This is a worst-case estimate, as the power consumption of the PG should not be included as a whole in this calculation, since in any fractional-N PLL a low-noise resampling stage clocked with the DCO signal is anyway needed at the MMD output.

[17]More formally, the amplitude of the $Q[k]$ sequence generated by a $\Delta\Sigma$ modulator is the same at different FCW values.

[18]In [41], a similar concept is applied to a fractional-N charge-pump (CP) PLL without DTC, however with some limitations: (1) the adoption of a divider prescaler led to a factor of 2 increase of the Q-error amplitude, (2) a wide range CP is required to handle the large Q-error at the PD input, (3) the Q-error cancellation is achieved in the analog domain with a DAC, thus suffering from mismatches between the DAC and CP current pulses.

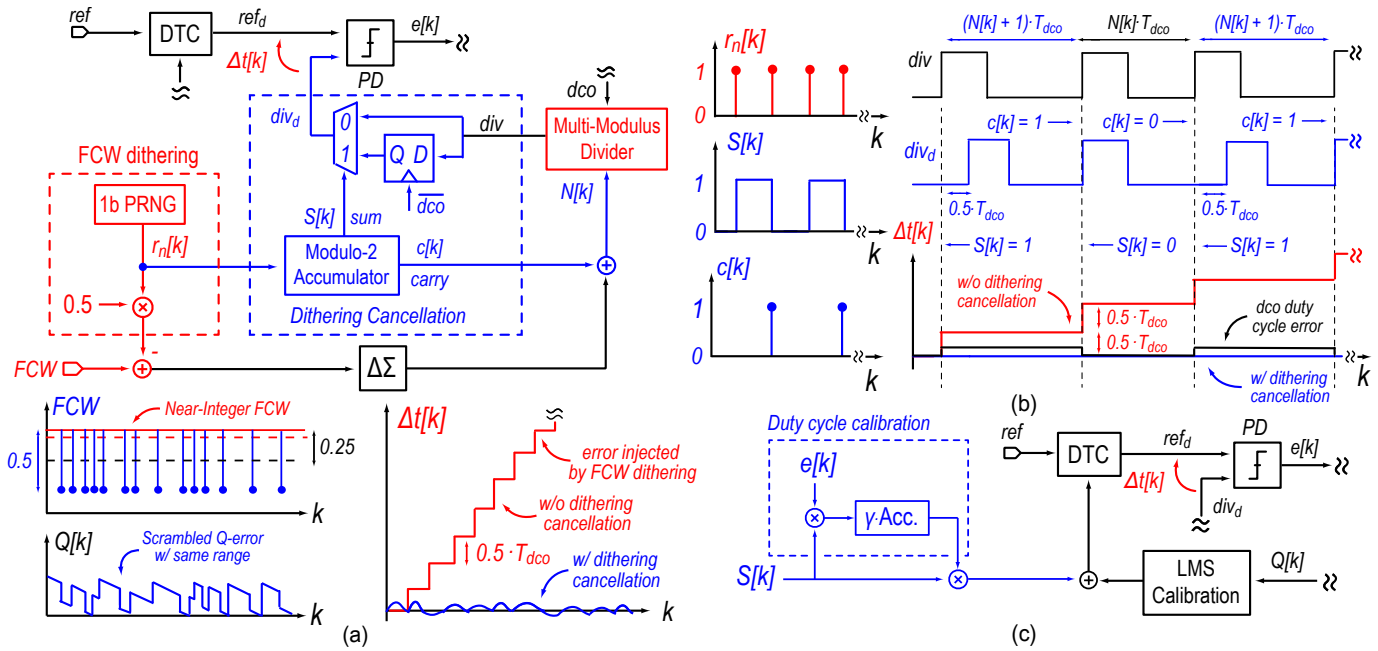


Fig. 15. FCW subtractive dithering: (a) block diagram including the dithering cancellation block and illustration of its impact on the $Q[k]$ sequence and $\Delta t[k]$, (b) waveforms of $r_n[k]$, $S[k]$, $c[k]$, div, div_d and $\Delta t[k]$ during the operation of the dithering cancellation block, highlighting the impact of the dco duty cycle errors (black $\Delta t[k]$ line) and (c) algorithm adopted for the correction of the non-50% dco duty cycle.

accumulated at the PD input, $\Delta t[k]$ (Fig. 15(a)-bottom right). The result is that the PD is eventually saturated and the PLL integrated jitter is highly degraded. To remove this time-error, a dedicated dithering cancellation block is included, which directly cancels the injected dithering at the PD input (Fig. 15(a)-bottom right). Since the dithering is first injected and then removed, this technique is denoted as *FCW subtractive dithering*. The scheme of the dithering cancellation block is shown in Fig. 15(a)-top, while its operation is illustrated in Fig. 15(b). It comprises a modulo-2 accumulator, fed with the output of the PRNG, $r_n[k]$. In this way, the first time the dithering is applied, i.e., $r_n[k] = 1$, the output of the accumulator, $S[k]$, switches from 0 to 1, while, at the same time, a time-error equal to $0.5 \cdot T_{dco}$ is injected at the PD input (see the first $0.5 \cdot T_{dco}$ step of $\Delta t[k]$ in Fig. 15(b)). To remove this time-error, a FF stage, clocked with the DCO falling edge, and a multiplexer controlled by $S[k]$ are added at the MMD output (Fig. 15(a)-top). In this way, when $S[k] = 1$, a delay equal to $0.5 \cdot T_{dco}$ (assuming a 50% dco duty cycle) is added on the divider path, thus cancelling the injected time-error. At the subsequent dithering pulse, the accumulator overflows, generating the carry signal $c[k]$ and resetting $S[k]$ back to zero (Fig. 15(b)). At the same time, the dithering injects an additional $0.5 \cdot T_{dco}$ time-error in the loop. Therefore, $\Delta t[k]$ in Fig. 15(b) reaches an overall time-error equal to T_{dco} that should be removed by the dithering cancellation block. Note that, since $S[k]$ is reset to zero, the multiplexer state is changed and the $0.5 \cdot T_{dco}$ delay that was previously added on the div path is now released. To cancel the overall T_{dco} time-error, the carry signal $c[k]$ is added to the divider ratio (Fig. 15(a)-top), causing the divider to increase its period by T_{dco} for a single reference cycle, thus removing the time-error at the PD input (Fig. 15(b)). The process goes on according to this scheme. Anytime the PRNG provides a dithering pulse, $S[k]$ and $c[k]$ toggle accordingly, so that the time-error injected by the dithering is cancelled by alternatively controlling the multiplexer on the divider path through $S[k]$ or by adding $c[k]$ to the divider ratio (Fig. 15(b)). Note that the FCW subtractive dithering technique can be naturally applied to whichever digital or analog PLL, indipendently of the order and type of the $\Delta\Sigma$ modulator used[19].

Since the dithering cancellation exploits the dco falling edge, the cancellation is precise only if the dco duty cycle is perfectly 50%, otherwise time-errors will be anyway generated at the PD input (see the $\Delta t[k]$ black line in Fig. 15(b)). Note that these time-errors are strongly correlated with the $S[k]$ sequence, as they only appear when $S[k] = 1$, i.e., when the FF path of the multiplexer is selected. To remove these errors, a LMS algorithm, similar to the one used to calibrate the DTC gain [14], is adopted. The scheme in Fig. 15(c) estimates the correlation between the $S[k]$ sequence and the PD error signal $e[k]$ by computing their product. The correlation estimate is fed to an accumulator, after scaling by a gain γ. The signal $S[k]$ is then scaled by the accumulator output and added at the main DTC input. At steady state, the accumulator settles so that the scaled $S[k]$ sequence cancels the time errors due to the non 50% dco duty cycle and no correlation between $S[k]$ and $e[k]$ is observed. Since these errors are expected to be small, being mainly due to circuit mismatches and asymmetries, the solution does not significantly increase the DTC dynamic

[19]This is different from the phase-dithering technique in [42], devised for a dividerless all-digital PLL (ADPLL) with a snapshot circuit, which also breaks the Q-error pattern periodicity but it cannot be readily extended to a PLL adopting an MMD driven by a generic $\Delta\Sigma$ modulator.

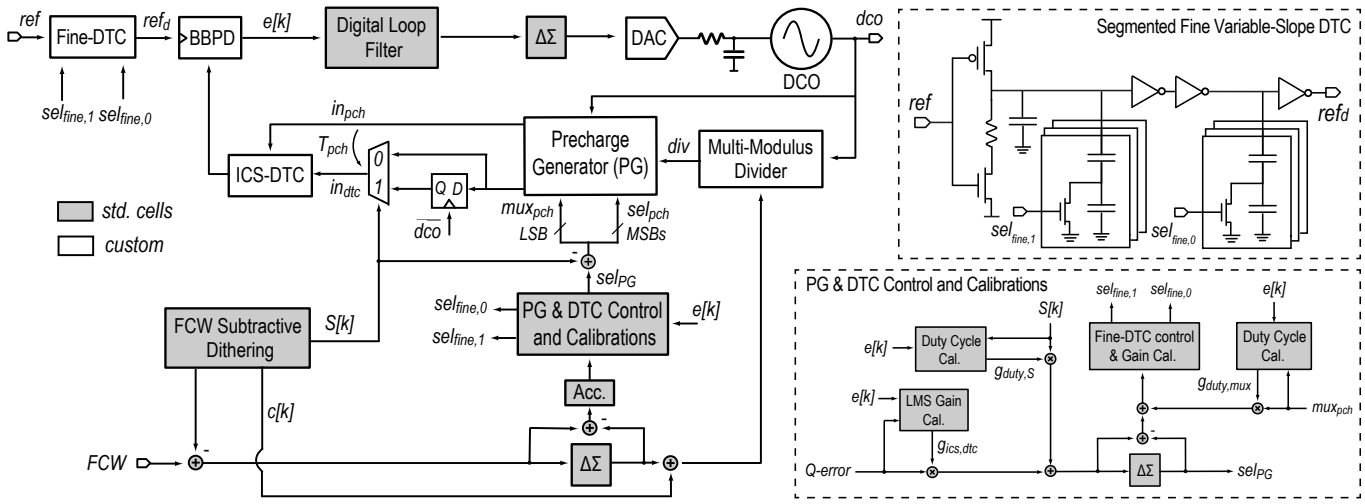


Fig. 16. Implemented BBPLL with ICS-DTC and FCW subtractive dithering. Schematic structure of the fine VS-DTC on the reference path and of the circuit providing the control signals for the PG and the DTC and implementing the LMS calibrations

range.

IV. PLL IMPLEMENTATION

Figure 16 shows a block diagram of the implemented fractional-N BBPLL, comprising both the ICS-DTC, the PG and the FCW subtractive dithering blocks. Note that a limitation of the ICS-DTC is its delay resolution, i.e., about 15 ps in this design as discussed in Secton II-E. To achieve a resolution in the order of hundreds of femtoseconds, required to push the residual Q-error below the random noise at the BBPD input, a fine VS-DTC is added on the PLL reference path. Since the VS-DTC circuit, shown in Fig. 16, should only cover the small range of the residual Q-error left by the ICS-DTC, its non-linearity is greatly reduced with respect to the one of a VS-DTC covering the whole range. The VS-DTC is segmented in two stages, driven by the $sel_{fine,1}$ and $sel_{fine,0}$ control signals. The first stage is used to cover a range of about 40 ps with a resolution around 1 ps, while the second stage improves the resolution to about 150fs and covers a much smaller range (i.e., about 5 ps). In the first stage, a resistor is added in series to the NMOS to reduce the DTC flicker noise [24] and a fixed capacitance is added to further reduce the DTC INL [1]. Note that a trade-off between the ICS-DTC noise, the ICS-DTC resolution and the VS-DTC non-linearity exists. Increasing the ICS-DTC resolution leads to a smaller VS-DTC dynamic range, thus further reducing its non-linearity. To do so, an higher value of K should be adopted (since the ICS-DTC resolution is $T_{dco}/(2K)$), while, to keep the same ICS-DTC dynamic range, the maximum value of T_{pch} and, correspondingly, the number of FFs within the PG, should be increased (as evident from (7)). However, a larger K leads to an increased contribution of noise from the bias circuit and the flicker noise of CG_0 and CG_1, as evident from (13), (14) and (15)[20]. On the contrary, to reduce these noise contributions, a lower K should be used, resulting in a worsening of the ICS-DTC resolution and requiring an higher VS-DTC dynamic range, thus increasing its non-linearity. In this design, as a compromise between these two effects, the ICS-DTC resolution was limited to around 15 ps, as discussed before. This, in combination with the targeted $2.4 \cdot T_{dco}$ ICS-DTC dynamic range, justifies the choice of using $K = 3.5$ and a maximum T_{pch} of $8.5 \cdot T_{dco}$ (i.e., 9 FF stages for the PG multiplexer in Fig. 7(a)) that were previously introduced Section II-D and II-E[21].

The PG and the fine DTC input codes are generated by the control and calibration logic shown in Fig. 16. The Q-error produced by the MASH 1-1 $\Delta\Sigma$ modulator driving the MMD is fed to a first order $\Delta\Sigma$ quantizer generating the PG input code, sel_{PG}, after the application of a LMS gain calibration block, used to track the ICS-DTC gain spreads. The sel_{PG} signal is split into its LSB and MSBs to obtain the PG control signals, mux_{pch} and sel_{pch}, respectively. To derive the $sel_{fine,1}$ and $sel_{fine,0}$ control signals, instead, the quantization error of the first-order $\Delta\Sigma$ quantizer is extracted and fed to the fine-DTC through a dedicated logic accounting for both the DTC segmentation and the DTC gain calibration across PVT spreads, as the one used in [14] or [22]. The latter exploits two LMS algorithms to individually calibrate the gains of the two fine-DTC stages. Note that, thanks to the $\Delta\Sigma$ quantizer driving the PG, the quantization-error sequence fed to the fine-DTC is randomized, which helps to further reduce the fractional spurs induced by its non-linearity, which, however, are already expected to be small due to its reduced range.

To enable the use of the FCW subtractive dithering technique in combination with the ICS-DTC, the FF and the multiplexer adopted for the dithering cancellation are placed on the in_{dtc} path at the PG output, as shown in Fig. 16. Note that the $S[k]$ signal controlling the multiplexer is also subtracted from sel_{PG}. This is done to ensure that, whenever

[20]This can be also understood by noticing that the higher maximum T_{pch} value results in a larger integration time for these noise sources.

[21]As shown later in Section V-B, with this choice, the non-linearity of the implemented VS-DTC and the ICS-DTC are comparable.

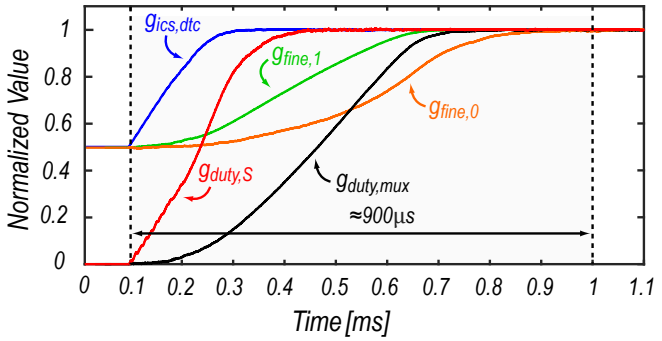


Fig. 17. Simulated convergence dynamics of the various LMS calibration gains adopted in this design. All the gains are normalized by their respective steady state values.

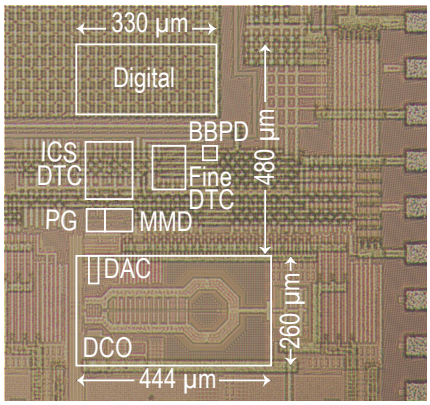
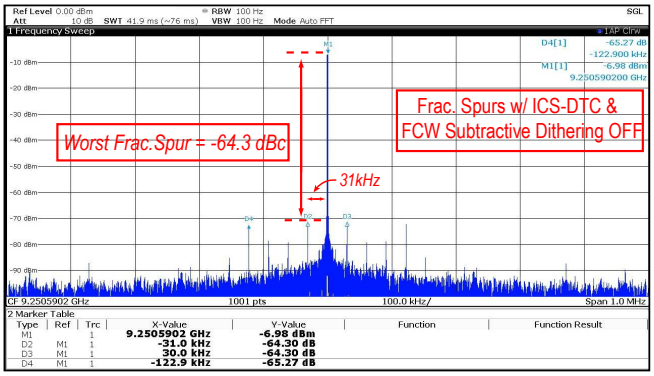
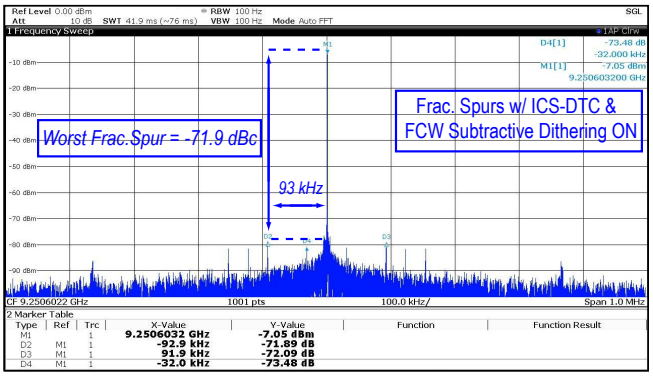


Fig. 18. Die Micrograph.



(a)



(b)

Fig. 19. Measured PLL spectra at a near-integer fractional-N channel with a 30 kHz offset from the 9.25 GHz integer-N channel: (a) with and (b) without enabling the FCW subtractive dithering technique.

a $0.5 \cdot T_{dco}$ delay is added on the in_{dtc} path to cancel the injected dithering, the same delay is also applied to the in_{pch} signal, to keep constant the time-duration T_{pch} fed to the ICS-DTC. The duty cycle calibration stage driven by $S[k]$ in Fig. 16, already introduced in Section III, is used to cancel the dco duty cycle errors occouring during the FCW subtractive dithering operation. The other duty cycle calibration block, fed with the mux_{pch} control signal, is used to cancel the errors caused by the non-50% dco duty cycle induced by the FF clocked with the dco falling edge within the PG circuit, via the fine-DTC.

Figure 17 shows the convergence dynamics of the various LMS calibration gains used in this design, obtained from behavioral simulations of the overall PLL system. In this plot, as highlighted in the scheme of Fig. 16 (bottom right), $g_{ics,dtc}$ is the ICS-DTC LMS gain, while $g_{duty,S}$ and $g_{duty,mux}$ are the LMS gains provided by the $S[k]$ and mux_{pch} duty cycle calibration blocks, respectively. Figure 17 also includes the convergence of the two LMS gains $g_{fine,1}$ and $g_{fine,0}$ used to individually calibrate the gains of the first and second stage of the fine-DTC, respectively (see [14] or [22]). In these simulations, a 10% DCO duty cycle error was enforced and the initial values of $g_{duty,S}$ and $g_{duty,mux}$ were set to 0, while $g_{ics,dtc}$, $g_{fine,1}$ and $g_{fine,0}$ were initialized with a 50% error from their steady state values. As shown in Fig. 17, it takes approximately 900 μs to fully settle all the LMS algorithms to steady state. Settling time improvements may be achieved by exploiting gear-shifting techniques, i.e., temporarily boosting the bandwidth of the LMS algorithms to speed-up their settling as in [1] and [43].

Figure 18 shows a die micrograph of the PLL, fabricated in a 28nm CMOS process. The PLL occupies an active area of 0.33 mm^2 and consumes 17.2 mW, excluding the input and output buffers, divided as follows: 12.5 mW for the DCO, 2.3 mW for the digital section, 1.4 mW for the ICS- and VS-DTCs, while the rest is dissipated by the combination of the MMD, PG and PD. The PLL output frequency ranges from 9.25 GHz to 10.5 GHz, while the input reference signal is provided by a 250 MHz low-noise off-chip SAW oscillator (i.e., Crystek CCSO-914X), which exhibits a phase-noise floor of about -170 dBc/Hz at 1 MHz offset[22].

V. Measurement Results

A. PLL performance

Figure 19(a) shows the measured PLL spectrum at a near-integer fractional-N channel with an offset of about 30 kHz from the 9.25 GHz integer-N channel. In this measurement, the FCW subtractive dithering technique was turned-off to assess the spur performance achieved thanks to the ICS-DTC only. The measured worst-case fractional spur is equal to

[22]The off-chip oscillator does not limit the PLL performance in this design, being well below the simulated ICS-DTC phase-noise.

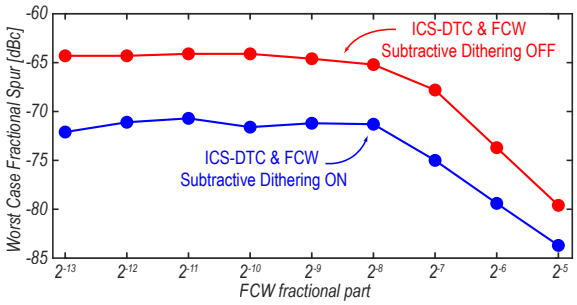
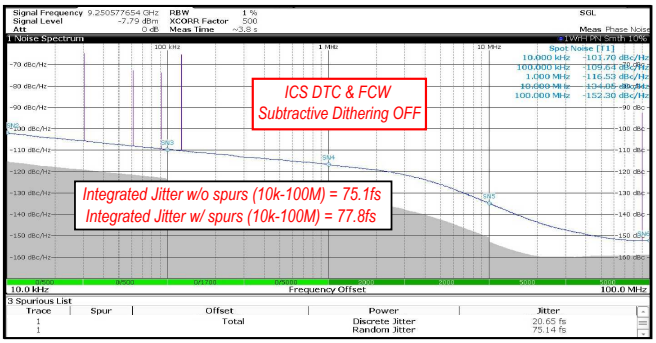
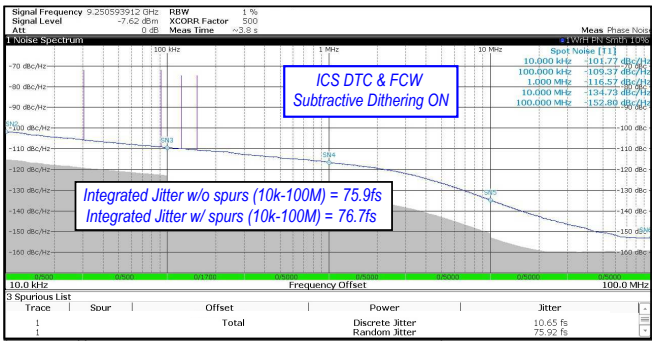


Fig. 20. Measured worst case fractional spurs as a function of the FCW fractional part at frequency channels near 9.25 GHz, with and without enabling the FCW subtractive dithering technique.



(a)



(b)

Fig. 21. Measured PLL phase-noise spectra at a near-integer fractional-N channel with an offset of about 30 kHz from the 9.25 GHz integer-N channel: (a) with and (b) without enabling the FCW subtractive dithering technique.

-64.3 dBc. When the FCW subtractive dithering technique is enabled, the measured worst case fractional spur reduces by about 8 dB, reaching a value of -71.9dBc (Fig. 19(b)). Figure 20 shows the measured worst case fractional spur as a function of the fractional frequency offset from the 9.25 GHz integer-N channel, with and without enabling the FCW subtractive dithering technique. When the technique is enabled, the worst case fractional spur always remains below -70 dBc.

Figure 21(a) shows the measured PLL phase-noise spectrum at the same (9.25 GHz + 30 kHz) near-integer channel presented above, when the FCW subtractive dithering technique is turned off. The RMS jitter, integrated from 10 kHz to 100 MHz and including the spurs, is equal to 77.8 fs. When the FCW subtractive dithering is turned on, the fractional spurs are reduced, as discussed above, while the PLL phase-noise

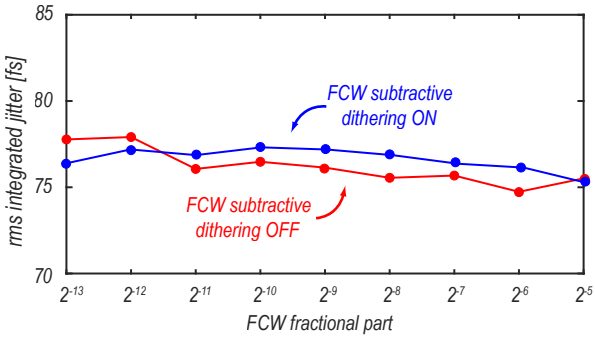
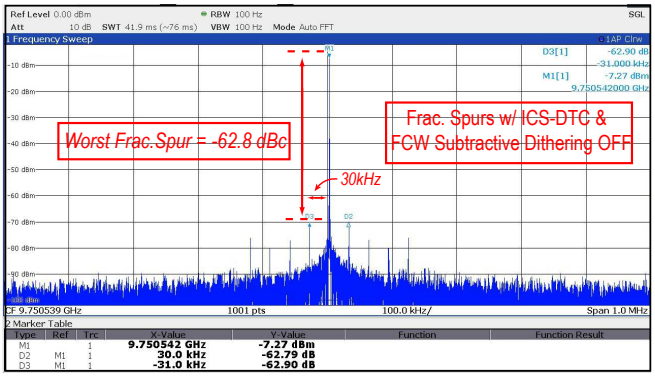
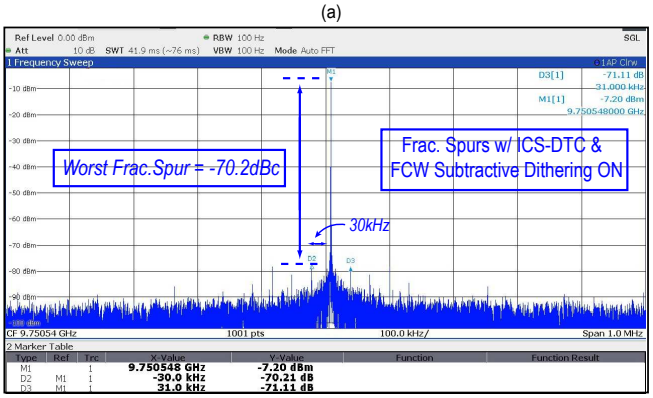


Fig. 22. Measured PLL integrated jitter as a function of the FCW fractional part at frequency channels near 9.25 GHz, with and without enabling the FCW subtractive dithering technique.



(a)



(b)

Fig. 23. Measured PLL spectra at a near-integer fractional-N channel with a 30 kHz offset from the 9.75 GHz integer-N channel: (a) with and (b) without enabling the FCW subtractive dithering technique.

remains almost unchanged, as shown in Fig. 21(b), with an RMS jitter of 76.7 fs. This measurement demonstrates the effectiveness of the proposed technique in reducing the spurs without increasing the PLL jitter, as it retains the same DTC dynamic range. Similar results are also obtained at different fractional-N channels near the 9.25 GHz integer-N channel, as shown in Fig. 22(a), where the measured integrated jitter level remains about the same when enabling the technique. In this design, the dominant in-band PLL phase-noise contribution comes from the ICS-DTC noise. This was verified by scaling up the simulated ICS-DTC phase-noise spectrum by $20 \cdot log_{10}(\text{FCW})$ and comparing it with the measured close-in

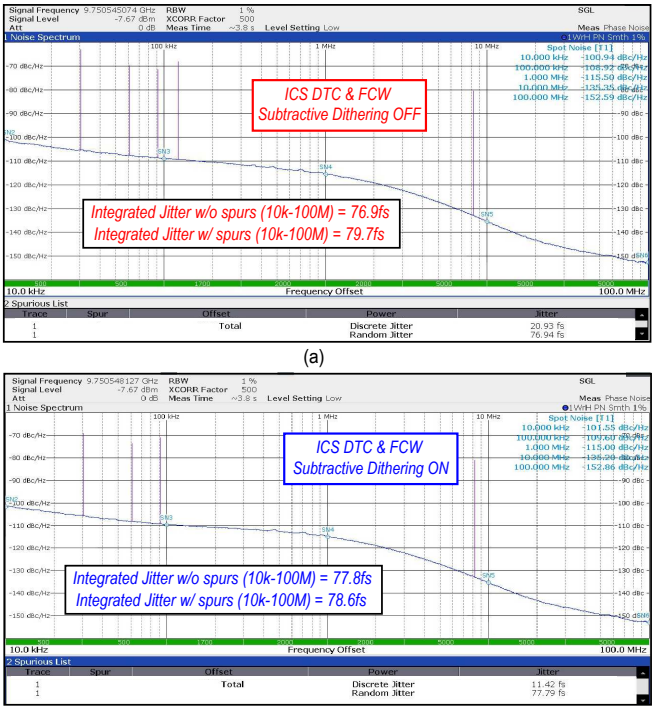


Fig. 24. Measured PLL phase-noise spectra at a near-integer fractional-N channel with an offset of about 30 kHz from the 9.75 GHz integer-N channel: (a) with and (b) without enabling the FCW subtractive dithering technique.

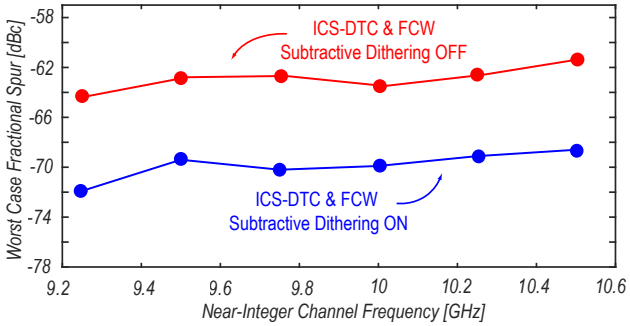


Fig. 25. Measured worst case near-integer fractional-N spurs across the PLL tuning range. The fractional part of the FCW was kept to 2^{-13} while the integer part was swept from 37 to 42 during the measurements.

PLL phase-noise, showing a good agreement[23].

Similar measurements were also performed at different channel frequencies across the PLL tuning range. Figure 23 shows the measured PLL spectra at a fractional-N channel with 30 kHz offset from the 9.75 GHz integer-N channel, with and without enabling the FCW subtractive dithering. The worst case fractional spur varies from -62.8 dBc to -70.2 dBc when enabling the technique, leading to about 7 dB reduction. On the other hand, the corresponding measured

[23]For instance, scaling up the simulated ICS-DTC phase-noise in Fig. 13(b) at $T_{dtc} = 250$ps, i.e., about mid range, gives an estimated close-in PLL phase-noise of -102.3 dBc/Hz at 10 kHz offset, while the measured value is -101.7 dBc/Hz.

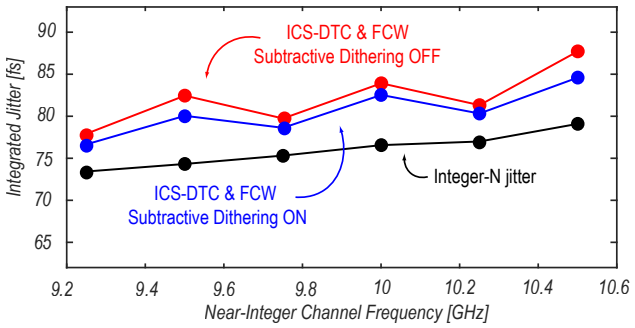


Fig. 26. Measured integrated jitter at near-integer fractional-N channels across the PLL tuning range. The fractional part of the FCW was kept to 2^{-13} while the integer part was swept from 37 to 42 during the measurements. The plot also shows the measured PLL integrated jitter in integer-N mode (i.e., when FCW$_{frac}$ is set to zero).

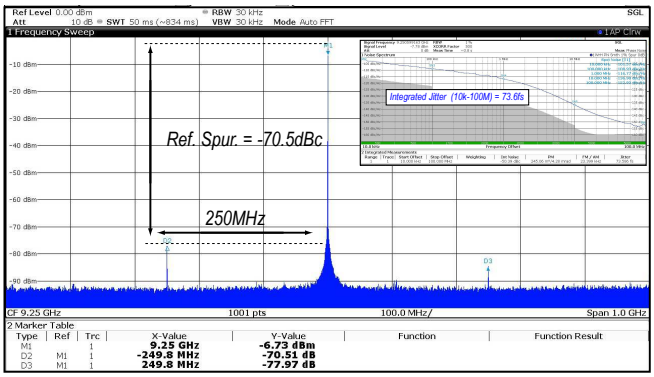


Fig. 27. Measured PLL phase-noise spectrum and reference spurs at the 9.25GHz integer-N channel.

PLL phase-noise spectra shown in Fig. 24 remain almost invariant, as expected, with an integrated jitter (including the contribution of spurs) varying from 79.7 fs to 78.6 fs. The measured PLL performance in near-integer fractional-N mode across the whole tuning range are reported in Fig. 25 and Fig. 26. In these measurements, the integer part of the FCW was swept from 37 to 42, while the fractional part was kept equal to 2^{-13}. In particular, Fig. 25 reports the measured worst case fractional spurs, with and without enabling the FCW subtractive dithering technique, demonstrating an at least 6 dB spur reduction across the PLL tuning range. Figure 26 reports instead the measured PLL integrated jitter (including the contribution of spurs), which stays below 90 fs across the tuning range and, as expected, remains essentially unchanged when enabling the FCW dithering technique.

The PLL performance in integer-N mode were also characterized. In Fig. 26, the measured PLL integrated jitter at the different integer-N channels within the PLL tuning range is highlighted, while Fig. 27 shows the measured PLL phase-noise spectrum and reference spurs at the 9.25 GHz integer-N channel. In the integer-N measurements, the input codes of the PG and the fine DTC were fixed at mid range.

Table I shows the performance comparison with state-of-the-art low-jitter fractional-N PLLs. Thanks to the proposed spur reduction solutions, this work achieves the lowest in-

TABLE I. Performance Summary and Comparison to State-of-the-Art Low-Jitter Fractional-N PLLs.

	This Work	Wu [8] JSSC '21	Kim [9] ISSCC '21	Mercandelli [44] ISSCC '21	Santiccioli [11] JSSC '21	Gao [15] JSSC '22	Park [22] JSSC '22	Liu [28] JSSC '18	Dartizio [6] JSSC '22	Geng [45] CICC '23
Architecture	BBPLL	SPLL	SSPLL	SBBPLL	BBPLL	ADPLL	OT-TDC PLL	ADPLL	BBPLL	TA-CPLL
Fractional Spur Suppression Method	**ICS-DTC+FCW Subtractive Dithering**	DTC Range Reduction	VDAC+INL Predistortion	DTC Gain Calibration	DTC Replica + Retiming	TAU + INL Predistortion	DTC-NC+ PDS-DSM	Constant Slope DTC	DTC Range Reduction	DTC INL Predistortion
Output frequency [GHz]	**9.25-10.5**	6.2	14-16	12.9-15.1	12.8-15.2	2.56-4.1	5.2-6	2-2.6	8.5-10	24-28
Reference frequency [MHz]	**250**	76.8×2	150	250	500	40	100	26×2	250	250
RMS jitter w/o Spurs [fs]	**75.9**	80	N/A	79.5	66.2	N/A	N/A	N/A	57.2	N/A
RMS jitter w/ Spurs [fs]	**76.7**	93.2	104	107.6	N/A	182	365	530	68.6	45.6
Integration Bandwidth [Hz]	**10k-100M**	10k-40M	10k-30M	1k-100M	1k-100M	10k-40M	10k-30M	N/A	1k-100M	10k-30M
Reference spur [dBc]	**-70.5**	-66***	N/A	-73.2	-80.1	-73.5	-77	-72	-70.2	-72
In-band fractional spur [dBc]	**-71.9**	-66.4***	-61	-50.4	-61	-59	-63	-56	-58.2	-59
Power dissipation [mW]	**17.2**	14.2	7.3	10.8	19.8	3.48	9.27	0.98	20	23.88
FoM_J* [dB]	**-250**	-250.4	N/A	-251.7	-250.6	N/A	N/A	N/A	-251.8	N/A
FoM_S** [dB]	**-249.9**	-249.1	-251	-249	N/A	-249.4	-239.1	-246	-250.3	-253
Area occupation [mm^2]	**0.33**	0.31	0.21	0.16	0.17	0.31	0.146	0.23	0.23	0.47
CMOS process	**28**	14	65	28	28	40	65	65	28	65

*$FoM_J = 10\log_{10}\left[\left(\frac{\text{Jitter}_{\text{w/o Spurs}}}{1\text{s}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$ **$FoM_S = 10\log_{10}\left[\left(\frac{\text{Jitter}_{\text{w/ Spurs}}}{1\text{s}}\right)^2 \cdot \left(\frac{\text{Power}}{1\text{mW}}\right)\right]$ ***Normalized to DCO frequency

band fractional spur level. This is achieved while guaranteeing a state-of-the-art FoM of about -250 dB and a competitive integrated jitter below 77 fs.

B. DTC non-linearity characterization

To assess the linearity performance of the implemented DTCs, the phase-modulation method in [46] was exploited. This approach can be directly applied to the measurement of the fine DTC non-linearity. However, it cannot be used for the ICS-DTC, as it requires the DTC under measurement to be fed with an external input signal, while the ICS-DTC, to properly work, requires the internal signals in_{dtc} and in_{pch} generated by the PG. To solve this problem, the BBPLL is configured as in the experimental setup shown in Fig. 28(a). The BBPLL is set in integer-N mode, while the fine DTC, the ICS-DTC and the PG are bypassed. In this scheme, the BBPLL is only used to provide the div and the dco signals to the PG, so that it can correctly produce the in_{dtc} and the in_{pch} signals required by the ICS-DTC. The ICS-DTC output is then divided by 2 and sent off-chip. The DTC measurement routine consists in applying a square wave modulation to the PG sel_{pch} control signal, varying between $sel_{pch,0}$ and $sel_{pch,0}+1$ with a period of N_{clk} clock cycles (Fig. 28(a)). As a result, the DTC delay is modulated by a square wave with an amplitude equal to the DTC LSB, which appears in the spectrum of the signal sent off chip as two sidebands with a strength proportional to the DTC LSB. By repeating the same measurement at different $sel_{pch,0}$ values and collecting the sideband amplitude values, the DTC INL profile can be reconstructed [46]. Figure 28(b)-(c) shows the measurement results. The ICS-DTC non-linearity was characterized with the BBPLL locked at 9.25 GHz, i.e., $T_{dco} = 108ps$. The ICS-DTC has a peak-to-peak INL of about 80 fs (Fig. 28(b)) over the 246 ps delay range swept during the measurement. This corresponds to 0.032% when normalized to the DTC range, thus outperforming state-of-the art CS-DTC implementations by about a factor of 4 in terms of linearity [30]. Instead, the fine DTC, thanks to the reduced range, has a peak-to-peak INL of only about 50 fs over a range of around 40 ps (Fig. 28(c)).

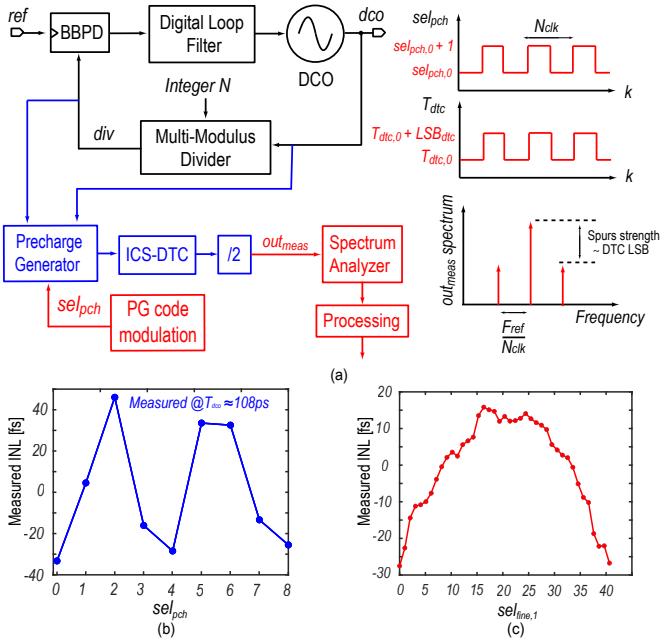


Fig. 28. DTC non-linearity measurements: (a) Experimental setup used to characterize the INL of the fabricated ICS-DTC and measured INL profiles of (b) the ICS-DTC and (c) the fine VS-DTC.

VI. Conclusions

This work presents a 9.25-to-10.5 GHz fractional-N bang-bang PLL implemented in a 28 nm CMOS technology. The PLL achieves 76.7 fs and -71.9 dBc in-band fractional spur by exploiting: (i) the inverse-constant-slope DTC architecture to improve the DTC linearity and (ii) the FCW subtractive dithering technique to randomize the quantization-error without worsening the PLL integrated jitter. Thanks to the proposed techniques, this work achieves the lowest in-band fractional spur level among low-jitter fractional-N PLLs.

Appendix A

This appendix is devoted to derive the ICS-DTC phase-noise induced by the white-noise of CG_0 and CG_1. To this aim, let us denote as σ_v^2 the voltage noise variance on the ICS-DTC

capacitor load C. The white phase-noise floor $\mathcal{L}_G$ caused by CG_0 and CG_1 can be derived as

$$\mathcal{L}_{w,G} = 4\pi^2 F_{ref} \cdot \frac{\sigma_v^2}{SL^2}, \tag{16}$$

where F_r is the reference frequency and $SL = K \cdot I_G/C$ is the slope of the capacitor voltage near the output buffer threshold [39]. The noise variance σ_v^2 can be computed by noticing that the CG_0 and CG_1 current noise are integrated over the capacitor for a time duration equal to $T_{pch} + T_{dtc}$ and T_{dtc}, respectively, (see Fig. 12), resulting in[24]:

$$\sigma_v^2 = \frac{S_I \cdot (T_{pch}+T_{dtc}) + (K-1) S_I \cdot T_{dtc}}{C^2} = \frac{S_I \cdot K \cdot T_{dtc,m}}{C^2}, \tag{17}$$

where S_I and $(K-1) \cdot S_I$ are the bilateral white current noise power spectral densities (PSDs) of CG_0 and CG_1, respectively[25]. In the last step of (17), the sum $T_{pch} + K \cdot T_{dtc}$, which is a constant term as evident from (6), was replaced by $K \cdot T_{dtc,m}$, where

$$T_{dtc,m} = \frac{1}{K} \int_0^{V_{th}} \frac{C(V)}{I_G(V)} dV \approx \frac{C \cdot V_{th}}{K \cdot I_G}, \tag{18}$$

is the maximum ICS-DTC delay, i.e., the value of T_{dtc} when $T_{pch} = 0$. Substituting (17) in (16), rearranging the terms and using the expression for the white current noise PSD of a MOS transistor, i.e., $S_I = 2kT\gamma g_m$, we get

$$\mathcal{L}_{w,G} = 4\pi^2 F_r \cdot 2kT\gamma \frac{g_m}{I_G} \cdot \frac{T_{dtc,m}^2}{C \cdot V_{th}}. \tag{19}$$

APPENDIX B

The analysis in Appendix A cannot be applied to the phase-noise induced by the CB_b white-noise, since the latter is low-pass filtered by the capacitor C_b before being mirrored to the CG_0 and CG_1 branches, therefore it cannot be modelled as a white-noise integrated over a capacitor [39]. As discussed in [39], noise sources with low-frequency components, such as a low-pass filtered or flicker noise, cause a phase-noise given by

$$\mathcal{L}(f) = 4\pi^2 F_r^2 \cdot \frac{S_v(f)}{SL^2}, \tag{20}$$

where $S_v(f)$ is the PSD of the voltage noise induced on the capacitor C while noise folding effects are neglected. Denoting by $i_{n,b}$ the low-pass filtered current noise component from CG_b, the voltage noise $v_{n,b}$ on the capacitor at the instant of the buffer threshold crossing can be derived as[26]

$$v_{n,b} = \int_0^{T_{pch}+T_{dtc}} \frac{M \cdot i_{n,b}(t)}{C} dt + \int_{T_{pch}}^{T_{pch}+T_{dtc}} \frac{M \cdot (K-1) \cdot i_{n,b}(t)}{C} dt. \tag{21}$$

[24]The voltage noise variance induced by a white current noise with bilateral power spectral density S_I integrated for a time duration T_w over a capacitor C is equal to $S_I \cdot T_w/C^2$.

[25]The CG_1 PSD is $(K-1)$ times larger than the one of CG_0 because CG_1 carries a current larger by a factor $(K-1)$.

[26]This equation was obtained by mirroring $i_{n,b}$ to the CG_0 and CG_1 branches and integrating it over the capacitor. The contributions from the CG_0 and CG_1 branches should be integrated for a time duration equal to $T_{pch} + T_{dtc}$ and T_{dtc}, respectively.

Since $i_{n,b}$ is a low-pass filtered noise, it is slowly varying, and therefore can be approximated as a constant term in (21), leading to

$$v_{n,b} \approx \frac{M \cdot (T_{pch} + K \cdot T_{dtc}) \cdot i_{n,b}}{C} = \frac{M \cdot T_{dtc,m} \cdot i_{n,b}}{C}. \tag{22}$$

Computing the PSD $S_{v_b}(f)$ of $v_{n.b}$ from (22) we get

$$S_{v_b}(f) = \frac{M^2 \cdot T_{dtc,m}^2}{C^2} \cdot \frac{S_{I,b}}{1 + \frac{f^2}{f_p^2}}, \tag{23}$$

where $S_{I,b}$ is the white current noise of CG_b, $f_p = g_{m,b}/(2\pi C_b)$ is the pole frequency due to the capacitor C_b and $g_{m,b}$ is the transconductance of CG_b. By substituting (23) in (20), noticing that $S_{I,b} = S_I/M$[27], and comparing the result with (19) after rearranging the terms we get

$$\mathcal{L}_{w,b}(f) = \mathcal{L}_{w,G} \cdot \frac{K \cdot M \cdot T_{dtc,m} \cdot F_r}{(1 + \frac{f^2}{f_p^2})}, \tag{24}$$

which gives the phase-noise contribution $\mathcal{L}_{w,b}$ caused by the CG_b white-noise.

APPENDIX C

This Appendix derives the ICS-DTC phase-noise caused by the flicker noise of CG_0, CG_1 and CG_b by using the approach discussed in Appendix B. For what concerns CG_0 and CG_1, the corresponding voltage noise perturbation $v_{f_n,G}$ can be derived as

$$v_{f_n,G} = \int_0^{T_{pch}+T_{dtc}} \frac{i_{f_n,CG_0}(t)}{C} dt + \int_{T_{pch}}^{T_{pch}+T_{dtc}} \frac{i_{f_n,CG_1}(t)}{C} dt, \tag{25}$$

where the CG_0 and CG_1 flicker current noise, i_{f_n,CG_0} and i_{f_n,CG_1}, were integrated for a time duration $T_{pch} + T_{dtc}$ and T_{dtc}, respectively. Due to the slowly varying nature of flicker noise, the terms i_{f_n,CG_0} and i_{f_n,CG_1} can be regarded as constant, leading to

$$v_{f_n,G} \approx \frac{(T_{pch} + T_{dtc}) \cdot i_{f_n,CG_0} + T_{dtc} \cdot i_{f_n,CG_1}}{C}. \tag{26}$$

Computing the PSD $S_{v_f,G}$ of $v_{f_n,G}$ we get

$$S_{v_f,G}(f) = \frac{(T_{pch}+T_{dtc})^2 \cdot S_{I,f_n}(f) + T_{dtc}^2 \cdot (K-1) S_{I,f_n}(f)}{C^2}, \tag{27}$$

where $S_{I,f_n}(f)$ and $(K-1)S_{I,f_n}(f)$ are the PSDs of the flicker current noise of CG_0 and CG_1, respectively[28]. By substituting (27) in (20), with $S_{I,fn}(f) = S_I \cdot f_n/f$, where f_n is the flicker corner frequency of the CG_0 current noise, and comparing the result with (19) we get

$$\mathcal{L}_{f_n,G}(f) = \mathcal{L}_{w,G} \cdot \frac{f_n \cdot T_{dtc,m} \cdot F_r \cdot [1 + (K-1)(1 - \frac{T_{dtc}}{T_{dtc,m}})^2]}{f}, \tag{28}$$

which gives the phase-noise $\mathcal{L}_{f_n,G}$ induced by the CG_0 and CG_1 flicker noise. Note that the analysis of the CG_b flicker

[27]This is true since CG_b carries a factor of M less current with respect to CG_0.

[28]This is because CG_1 carries a current $K-1$ larger with respect to CG_0.

noise can be carried out by following the same steps discussed in Appendix B. Therefore the PSD of the corresponding voltage noise $S_{v_f,b}(f)$ can be derived substituting $S_{I,b}$ in (23) with the flicker current noise PSD $S_{I_f,b}(f) = S_{I,b} \cdot f_{n,b}/f$, where $f_{n,b}$ is the flicker corner frequency of the CG_b current noise, and then using $S_{v_f,b}(f)$ in (20). After rearranging the terms and comparing the result with (24), we get

$$\mathcal{L}_{f_n,b}(f) = \mathcal{L}_{w,b}(f) \cdot \frac{f_{n,b}}{f}, \tag{29}$$

which gives the phase-noise $\mathcal{L}_{f_n,b}$ induced by the CG_b flicker noise.

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