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Interleaved SAR 20-bit ADC Architecture for Direct Sampling in X-ray Spectroscopy

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Abstract

We present a novel digital signal processing technique for X-ray detectors, particularly silicon drift detectors (SDDs), optimized for high-count rate applications without compromising energy resolution. Traditional approaches employing transistor reset preamplifiers encounter significant limitations due to the dominant voltage ramp at the preamplifier output, which can obscure low-amplitude signals of interest. To overcome this, we adopted a high-resolution 20-bit successive approximation register (SAR) ADC capable of directly sampling the preamplifier output, offering a dynamic range exceeding 1:1,000,000 and enabling effective signal acquisition despite the ramp.

To achieve high throughput, we implemented a system architecture based on four interleaved ADCs, providing an aggregate sampling rate of 160 Msps. Signal readout and control are handled by a Zynq System-on-Chip (SoC), which also manages phase alignment, gain calibration, digital filtering via a trapezoidal algorithm, and PC interfacing.

Initial experimental validation was carried out using the multipixel SDD ARDESIA detector developed at Politecnico di Milano. Despite the prototypal status, our system demonstrated superior resolution compared to conventional analog reshaping techniques. Specifically, we achieved a full width at half maximum (FWHM) resolution of 128 eV at 2 µs peaking time, and 140 eV at an event rate of 1 Mcps using a faster shaping configuration.