A Saturated Higher Order Sliding Mode Control Approach for DC/DC Converters

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***Abstract*— This paper presents a novel approach of designing saturated Higher-Order Sliding Mode (HOSM) controllers for a class of DC/DC converters. Specifically, the proposed controller aims at guaranteeing boundedness and smoothness of the duty cycle feeding the Pulse-Width-Modulator. The novel control architecture consists of the so-called Bounded Integral Control (BIC) combined with a discontinuous HOSM control algorithm. The main strength of the proposed approach is its general applicability to a large class of DC/DC converters. Numerical results testify the effectiveness of the proposed approach.**

I. Introduction

DC/DC converters are electronic devices able to convert a source of direct current from a voltage level to another. Due to their wide range of possible power levels, they have been widely adopted in several applications such as microgrids [1], transportation systems [2] or photovoltaic systems [3]. These devices are controlled by properly acting on the power electronic switches through a periodic, high-frequency switching signal generated by a Pulse-Width Modulator (PWM) to obtain the desired output voltage. Therefore, switching dynamics generated by such elements can be modeled as the action of a discontinuous input taking values either 0 (switch open) or 1 (switch closed).

The control design of power converters has been an interesting challenge during the past two decades. Several different theoretical frameworks have been adopted to solve this task. For instance, in [4] a hybrid systems approach was applied to the analysis and control of switched converters with PWM inputs. Discontinuous sliding mode control for DC/DC converters control was deeply discussed in [5], where the discontinuous signal generated by first-order Sliding Mode Control (SMC) is directly applied to the converter switches, avoiding the PWM modulation. Furthermore, assuming high switching frequency, it is possible to design the control strategy through analysis of the so-called average model [6]. While the hybrid approach offers rigorous and elegant tools to solve the control problem, the analysis through its framework is not straightforward. On the other hand, the discontinuous SMC approach cannot guarantee a fixed switching frequency, which is crucial for many power electronics applications. Hence, the most frequently adopted approach, which is also considered in this work, consists in approximating the high-frequency switching signal, generated by a PWM, with its average value in a period, that is the duty cycle, and design a smooth control input to drive the PWM.

Due to converter parameters uncertainties and measurement noise, robustness is one of the key points when designing control algorithms for DC/DC converters. Continuous Higher-Order Sliding Mode (HOSM) algorithms obtained as a time integration of a discontinuous signal (e.g., as in [7]) have been successfully proved to be a valid approach for this kind of applications (see [8] for instance). Nevertheless, if on the one hand a continuous signal is fed into the plant allowing chattering alleviation, on the other hand its amplitude could be time varying and overcoming the intrinsic saturation of the duty cycle for which meaningful values are only those belonging to the set $[0, 1]$. Several HOSM controllers with embedded saturation strategies have been investigated. Specifically, a modified Suboptimal Second-Order Sliding Mode (SSOSM) approach with desaturation strategy has been proposed in [9]. In [10], instead, a saturated Super-Twisting Sliding Mode (STSM) control has been introduced, proving finite time convergence and saturation fulfilment relying on Lyapunov theory provided that perturbations do not exceed half of the control input bounds. This requirement has been then removed in [11]. In [12] both state and input constraints are instead taken into account for designing HOSM control laws with optimal reaching.

Differently from [9], [10], [11], in this paper a novel approach for HOSM saturation is proposed. The proposed control architecture is based on the combination of a discontinuous HOSM strategy with the so-called Bounded Integral Control, initially introduced in [13] and then enhanced in [14]. It is worth highlighting that, while in [13], [14], BIC is used to replace classical integral control, in this paper it is instrumental for developing a generic sliding mode control with desaturation properties. Furthermore, while in [9], [10], [11] a specific saturation strategy had to be designed for the specific considered

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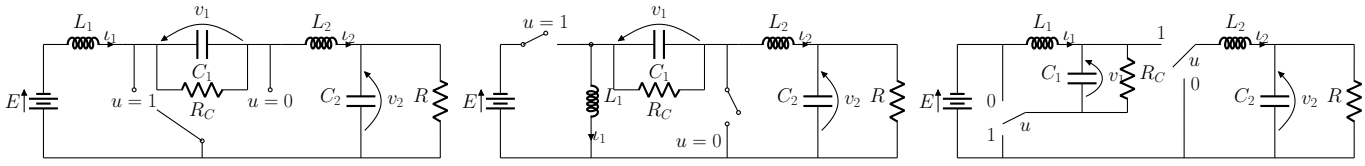

(a) Cúk Converter (b) Zeta Converter (c) Quadratic Buck Converter

Fig. 1: Cúk, Zeta and Quadratic Buck converter.

HOSM laws, the approach proposed in this work aims at being applicable to generic r-order HOSM control algorithms. Further details regarding the combination of discontinuous HOSM and BIC can be found in [15].

The combination of BIC and HOSM control is here applied to the control of a class of DC/DC converters characterized by some common properties such as number of control inputs, order of the system and relative degree with respect to the selected sliding function.

II. DC/DC Power Converter Models

In the following, a class of power converters, that can be obtained as a combination of the basic converter topologies representing the Buck, the Boost and the Buck-Boost converters, are introduced and their common properties are discussed.

A. Cúk converter

The Cúk converter (see Figure 1a) is obtained as the cascade connection of the Boost and the Buck converter. In fact, the input circuit in the Cúk converter is a Boost converter and the output circuit is seen to be a Buck converter. This converter amplifies and reduces the input voltage with polarity inversion.

Its dynamics is described by the following set of differential equations

$$\begin{aligned}
\dot{\iota}_1 &= \frac{1}{L_1}\left[-R_S\iota_1 - (1-u)v_1 + E\right] \\
\dot{v}_1 &= \frac{1}{C_1}\left[-\frac{v_1}{R_C} + (1-u)\iota_1 + u\iota_2\right] \\
\dot{\iota}_2 &= \frac{1}{L_2}\left[-R_S\iota_2 - uv_1 - v_2\right] \\
\dot{v}_2 &= \frac{1}{C_2}\left[\iota_2 - \frac{v_2}{R}\right],
\end{aligned} \tag{1}$$

where $u \in [0,1]$ is the converter duty cycle, ι_1 is the current flowing through the inductor L_1, v_1 is the voltage on the capacitor C_1, ι_2 is the current flowing through the inductor L_2, and v_2 is the converter output voltage over the capacitor C_2. The resistors R_S and R_C represent the switches resistance and the capacitor inner resistance, respectively. Finally, the input voltage source and the connected resistive loads are indicated with E and R, respectively.

B. Zeta converter

Similarly to the Cúk converter, the Zeta converter (see Figure 1b) can be modeled as a fourth order bilinear system. This converter can both amplify and reduce, without polarity inversions, the value of the input source voltage E.

The equations describing the dynamics of the converters are

$$\begin{aligned}
\dot{\iota}_1 &= \frac{1}{L_1}\left[-R_S\iota_1 - (1-u)v_1 + uE\right] \\
\dot{v}_1 &= \frac{1}{C_1}\left[-\frac{v_1}{R_C} + (1-u)\iota_1 - u\iota_2\right] \\
\dot{\iota}_2 &= \frac{1}{L_2}\left[-R_S\iota_2 - uv_1 - v_2 + uE\right] \\
\dot{v}_2 &= \frac{1}{C_2}\left[\iota_2 - \frac{v_2}{R}\right],
\end{aligned} \tag{2}$$

where the notation is the same as the one adopted for the Cúk converter in (1).

C. Quadratic Buck converter

The Quadratic Buck converter (see Figure 1c) represents a valid alternative to the more commonly known Buck converter and it owes its name to the quadratic nature of its static function.

The equations of this converter are

$$\begin{aligned}
\dot{\iota}_1 &= \frac{1}{L_1}\left[-R_S\iota_1 - v_1 + uE\right] \\
\dot{v}_1 &= \frac{1}{C_1}\left[-\frac{v_1}{R_C} + \iota_1 - u\iota_2\right] \\
\dot{\iota}_2 &= \frac{1}{L_2}\left[-R_S\iota_2 + uv_1 - v_2\right] \\
\dot{v}_2 &= \frac{1}{C_2}\left[\iota_2 - \frac{v_2}{R}\right],
\end{aligned} \tag{3}$$

where, again, the notation is the same as the one adopted for the Cúk converter in (1).

The above converters share some common interesting properties. First, their topologies can all be modeled as fourth order bilinear dynamical systems. Moreover, they share a common control objective, that is the regulation of the output voltage v_2 to a given reference $\bar{v}_2$. Then, for all the above systems, the control input, i.e., the duty cycle, does not directly affect the differential equation describing the behavior of v_2. Finally, denoting $x \coloneqq [x_1, x_2, x_3, x_4]^\top = [\iota_1, v_1, \iota_2, v_2]^\top$, equations (1), (2) and (3) can be synthetically rewritten as affine systems of the form

$$\begin{cases} \dot{x}(t) = a(x(t)) + b(x(t))u(t) & \text{(4a)} \\ y(t) = x_4(t) - \bar{v}_2, & \text{(4b)} \end{cases}$$

where $a(x(t))\colon \mathbb{R}^4 \to \mathbb{R}^4$ and $b(x(t))\colon \mathbb{R}^4 \to \mathbb{R}^4$. These commonalities allow for a unified design of the output voltage control for the above converters.

III. Problem Formulation and Stability Properties

A. Problem Formulation

An important aspect of power converters control is the boundedness of the control input. In fact, meaningful values of the duty cycle are only those belonging to the interval $[0, 1]$. Furthermore, in some cases the set of acceptable values of the duty cycle can be further shrunk to limit the converter currents. Thus, more generally, the control input constraint can be stated as

$$u(t) \in [0, \bar{u}], \ \ \forall t \geq t_0, \tag{5}$$

with $\bar{u} \in (0, 1]$.

Most control algorithms dealing with input constraint usually consider symmetric input bounds. Therefore, it is useful to perform an input linear transformation to define a new input variable characterized by symmetric bounds as

$$\tilde{u}(t) = \frac{u(t) - \bar{u}}{\bar{u}} 2U + U, \tag{6}$$

with U being a positive constant selected by the designer. Such transformation guarantees that if the newly defined input $\tilde{u}$ belongs to the symmetric set $[-U, U]$, then constraint (5) is fulfilled. Thus, system (4) can be equivalently reformulated as

$$\begin{cases} \dot{x}(t) = \tilde{a}(x(t)) + \tilde{b}(x(t))\tilde{u}(t) & \text{(7a)} \\ y(t) = x_4(t) - \bar{v}_2. & \text{(7b)} \end{cases}$$

subject to $\tilde{u}(t) \in [-U, U]$ with $\tilde{a}(x(t)) \coloneqq a(x(t)) + \frac{1}{2} b(x(t))\bar{u}$ and $\tilde{b}(x(t)) \coloneqq \frac{\bar{u}}{2U} b(x(t))$.

For the sake of control design, let us now define the sliding variable

$$\sigma_1(t) = y(t) = x_4(t) - \bar{v}_2, \tag{8}$$

which is required to be steered to zero. Considering such choice of the sliding function, a common property of the above converters is their relative degree, that is the smallest constant value r such that

$$\frac{\partial}{\partial u} \sigma_1^{(i)} = 0, \ \ i = 1, \ldots, r-1; \ \ \frac{\partial}{\partial u} \sigma_1^{(r)} \neq 0.$$

In fact, considering the sliding function (8) and its time derivatives, systems (1), (2) and (3) have a time-invariant relative degree equal to 2. Such condition inhibits the possibility to adopt first order sliding mode control, since the control input has no direct effect on the sliding variable. Therefore, a second order sliding mode naturally applies. However, this might generate the so-called chattering phenomenon due to the discontinuous nature of the input. A possible solution aimed at chattering alleviation is given by the adoption of a third order sliding mode control algorithm for an auxiliary system of augmented order. Specifically, the latter approach is based on the addition of an integrator dynamics which increases the relative degree and allows the adoption of a discontinuous third order sliding mode control strategy on the auxiliary system while actually providing a continuous signal to the plant. This work will mainly focus on this solution.

Computing the first, second and third time-derivatives of (8) along the trajectories of system (7), the auxiliary system with relative degree 3 can be written as

$$\begin{cases} \dot{\sigma}_1(t) = \sigma_2(t) & \text{(9a)} \\ \dot{\sigma}_2(t) = \sigma_3(t) & \text{(9b)} \\ \dot{\sigma}_3(t) = f_1(x(t), \tilde{u}) + f_2(x(t))v(t) & \text{(9c)} \\ \dot{\tilde{u}}(t) = v(t), & \text{(9d)} \end{cases}$$

where v is the auxiliary input, and f_1 and f_2 are continuous uncertain vector fields, with f_1 being different for each converter, while $f_2 = -\frac{\bar{u}}{2UC_2L_2} v_1$ for the Cúk and Zeta converter, and $f_2 = \frac{\bar{u}}{2UC_2L_2} v_1$ for the Quadratic Buck converter.

Relying on the above discussion, the control problem to solve can be stated as follows.

Problem 1. *(Finite time regulation with saturated input) Design a discontinuous-time robust feedback control law $v(t)$ able to regulate $(\sigma_1(t), \sigma_2(t), \sigma_3(t))$ to zero in finite time while ensuring boundedness of the overall converter dynamics and fulfilling constraint $\tilde{u}(t) \in [-U, U]$.*

B. Stability Properties

Prior to investigating the control design for the above converters, their stability properties are analyzed.

Indeed, it can be formally proved that systems (1), (2) and (3) cannot undergo any unstable behavior for any trajectory of the control input $u \in [0, 1]$ (as it happens, for instance, in the case of the ideal Boost converter). Specifically, this result can be achieved by resorting to the Input-to-State Stability (ISS) property and its Lyapunov characterization [16].

Lemma 1. *Systems* (1), (2) *and* (3) *are ISS with respect to the external input E for any input trajectory $u(t)$.*

Proof. Similarly to the proof of [17, Lemma 1], the Lemma can be proved by choosing the Lyapunov function candidate

$$V = \frac{1}{2} L_1 \iota_1^2 + \frac{1}{2} C_1 v_1^2 + \frac{1}{2} L_2 \iota_2^2 + \frac{1}{2} C_2 v_2^2,$$

and computing its time derivative along the trajectories of systems (1), (2) and (3), respectively. □

Lemma 1 proves that the upper-bound of the state norm can be obtained as the sum of two terms: a function of the converters initial condition, and a function of the magnitude of E. This in turn implies that there exist constants I_1^+, I_1^-, V_1^+ V_1^-, I_2^+, I_2^-, V_2^+ and V_2^- such that $I_1^- \leq \iota_1 \leq I_1^+$, $V_1^- \leq v_1 \leq V_1^+$, $I_2^- \leq \iota_2 \leq I_2^+$ and $V_2^- \leq v_2 \leq V_2^+$. Noting that v_1 represents the voltage over capacitor C_1, it is expected that its sign

never changes. Therefore, it can be safely assumed that constants V_1^- and V_1^+ have the same sign. The same reasoning can be applied to the voltage v_2 and its upper and lower bound V_2^- and V_2^+.

Boundedness of the converters states has a dual importance. Firstly, having proved that the system trajectories are always bounded for any input trajectory $u(t)$ guarantees that the residual dynamics (that is the dynamics of the system when $v_2(t) \equiv \bar{v}_2$) is bounded. Furthermore, boundedness guarantees the existence of positive constants K_m, K_M and C such that

$$K_m \leq f_1(x(t), u) \leq K_M, \quad |f_2(x(t))| \leq C. \tag{10}$$

The above condition is a fundamental hypothesis for many higher-order sliding mode control algorithms (see for instance [7], [12]).

IV. Saturated HOSM control design

A. The proposed control scheme

In this paper, to solve the problem formulated in Section III, we propose a general approach based on the combination of a discontinuous HOSM strategy and the so-called BIC, exploited in place of the traditional integrator to account for the input saturation limits and to smooth the discontinuous control provided by the HOSM control.

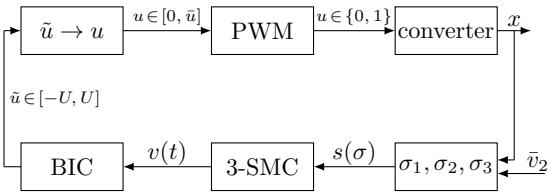

Fig. 2: Representation of the proposed control scheme with 3-SMC control and BIC mechanism.

The considered control scheme in Figure 2 includes six key blocks: the PWM modulator, the converter, the block computing an augmented vector of the sliding variable and its derivatives, the block implementing the discontinuous 3-SMC, the one with the BIC mechanism and the one implementing the linear input transformation. The sliding variable σ_1 is selected as in (8), while its derivatives can be measured or retrieved for instance by the so-called Levant's differentiator of the suitable order [18]. The vector of the sliding variable and its derivatives suitably augmented is then used by the 3-SMC law, which generates a discontinuous signal. The latter is directly transmitted to the BIC block, which generates a smooth input in the interval $[-U, U]$. Then, such input is transformed in the duty cycle taking values in the set $[0, \bar{u}]$ and it is finally sent to the PWM to regulate the converter switches. In the following, the 3-SMC and the BIC mechanism are detailed.

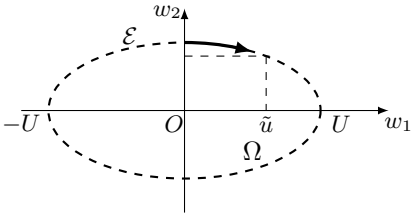

Fig. 3: BIC working principle.

B. Third order sliding mode control component

According to the HOSM control literature, since the relative degree of the auxiliary system (9) is 3, a 3-SMC can be therefore applied. Specifically, in the following any sliding mode control method of the type

$$v(t) = -\alpha \cdot \mathrm{sgn}(s(\sigma(t))), \tag{11}$$

is assumed eligible, with $\sigma(t) \coloneqq [\sigma_1(t), \sigma_2(t), \sigma_3(t)]^\top$. The discontinuous control law is such that the amplitude α satisfies $\alpha > C/K_m$. Specifically, α has to be properly selected depending on C and K_m to enforce a sliding mode in a finite time on the sliding manifold $s(\sigma(t)) = 0$. The expression of $s(\sigma(t))$ depends on the particular choice of the 3-SMC algorithm. For instance, a possible choice of $s(\sigma(t))$ is the one presented in [19], i.e.,

$$s_L(\sigma) = \sigma_3 + \beta_2 (|\sigma_2|^3 + \sigma_1^2)^{\frac{1}{6}} \times \mathrm{sgn}\Big(\sigma_2 + \beta_1 |\sigma|^{\frac{2}{3}} \mathrm{sgn}(\sigma_1)\Big). \tag{12}$$

Alternatively, in [20] a 3-SMC control law with optimal reaching was proposed, with $s(\sigma(t))$ as

$$s_{OR}(\sigma) = \sigma_1 + \frac{\sigma_3^3}{3\alpha_r^2} + \frac{\rho}{\sqrt{\alpha_r}} \left(\rho\sigma_2 + \frac{\sigma_3^2}{2\alpha_r} \right)^{\frac{3}{2}} + \frac{\rho\sigma_2\sigma_3}{\alpha_r} \tag{13}$$

$$\rho = \mathrm{sgn}\left(\sigma_2 + \frac{\sigma_3 |\sigma_3|}{2\alpha_r} \right).$$

Remark 1 (Choice of the sliding manifold). It is worth highlighting that the proposed approach can be applied for any r-th order sliding mode control, independently of the choice of the sliding variable $\sigma_1(t)$, and of the sliding manifold $s(\sigma(t))$. □

C. BIC component

In this section the enhanced BIC mechanism introduced in [14] is recalled and recast according to the HOSM formulation. Let $-U$ and U be the lower and upper bounds of the input signal, and w_1 and w_2 the additional controller state variables. Consider now the closed curve in Figure 3 represented by the following set

$$\mathcal{E} \coloneqq \big\{ (w_1,\, w_2) \in \mathbb{R}^2 \;:\; \epsilon(w_1, w_2) = 0 \big\} \tag{14a}$$

$$\epsilon(w_1, w_2) \coloneqq \frac{w_1^2}{U^2} + w_2^{2m} - 1, \tag{14b}$$

with m being a positive integer greater or equal than one. The integration and desaturation strategy combined with

the previous 3-SMC control laws then becomes

$$\tilde{u} = w_1 \tag{15a}$$

$$\begin{bmatrix} \dot{w}_1 \\ \dot{w}_2 \end{bmatrix} = \begin{bmatrix} -k\epsilon(w_1,\, w_2) & k_I v(t) w_2^{2m-1} \\ -k_I v(t) \frac{w_2}{U^2} & -k\epsilon(w_1,\, w_2) \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \end{bmatrix}, \tag{15b}$$

where k and k_I are suitable positive constant gains.

Specifically, the idea underlying the BIC approach is to make the controller state variables $(w_1(t), w_2(t))$ move towards the closed curve $\mathcal{E}$ and remain on it over times to ensure that the control input $\tilde{u}$ is constrained in the set $[-U, U]$. Once $(w_1(t), w_2(t)) \in \mathcal{E}$, then the BIC algorithm approximates the behavior of an integrator while embedding an intrinsic saturation strategy. In fact, it is possible to observe that for $(w_1(t), w_2(t)) \in \mathcal{E}$ (i.e. $\epsilon(w_1, w_2) = 0$) the BIC algorithm reduces to

$$\dot{w}_1 = k_I v(t) w_2^{2m} \tag{16}$$

$$\dot{w}_2 = -k_I v(t) \frac{w_1 w_2}{U^2}. \tag{17}$$

For high values of m, the closed curve in Figure 3 approximates a rectangle, thus yielding $w_2 \approx 1$ when w_1 is far from the saturation limits. In this case, (16) approximates the behavior of an integrator with gain k_I. If the controller state w_1 (equivalently $\tilde{u}$) approaches the saturation limit, then the state w_2 tends to zero thus slowing down the integration in (16) and guaranteeing that w_1 does not overcome the saturation bounds.

Three constants must be designed to implement this algorithm: the integer m sets the sharpness of the closed curve $\mathcal{E}$, thus regulating the saturation behavior, k regulates the convergence rate of $(w_1(t), w_2(t))$ towards the curve $\mathcal{E}$, and k_I is the integral gain.

Remark 2 (Anti-windup property). Note that, as indicated also in [14], [15], the BIC strategy intrinsically has an anti-windup property, which can be suitably enhanced by a proper choice of the parameter m. □

V. Case Study

In order to verify the effectiveness of the proposed saturated HOSM control approach, the Cúk converter, shown in Figure 1a, has been implemented in a simulation environment. The converter parameters are presented in Table I, where f_{PWM} is the switching frequency of the PWM regulating the converter switches.

TABLE I: Cúk converter parameters

E	270 [V]
L_1	10 [mH]
L_2	10 [mH]
C_1	800 [μF]
C_2	400 [μF]
R_S	100 [mΩ]
R_C	1 [MΩ]
R	10 [Ω]
f_{PWM}	100 [kHz]

The control task is to regulate the output voltage v_2 to a given piecewise constant reference $\bar{v}_2$. For stability reasons, i.e., to avoid relatively high values of the inductor

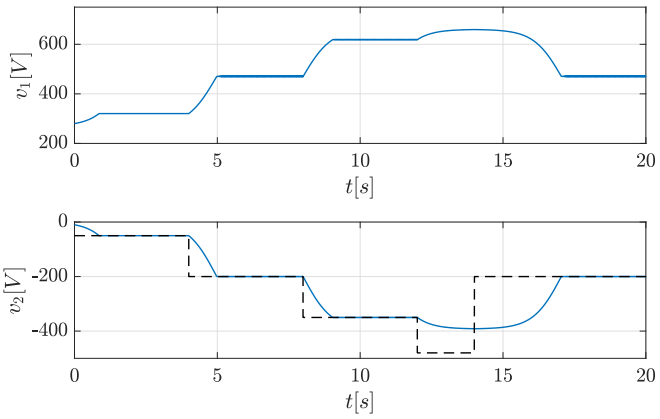

Fig. 4: From the top: time evolution of the voltage v_1; time evolution of the voltage v_2 (blue solid line) and reference voltage $\bar{v}_2$ (black dashed line)

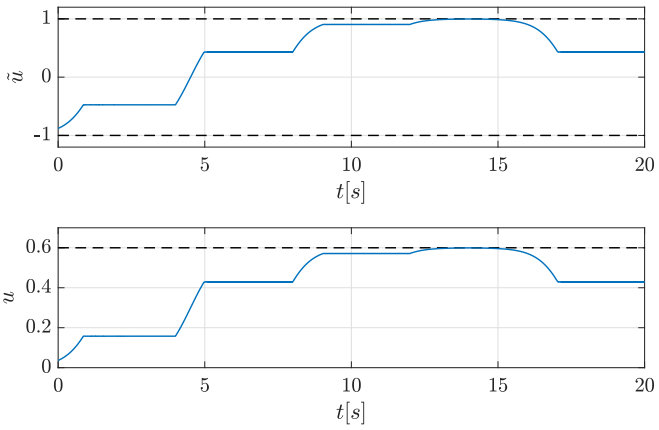

Fig. 5: From the top: time evolution of the BIC output $\tilde{u}$ (blue solid line) with upper/ lower bound (black dashed line); time evolution of the duty cycle u (blue solid line) with upper/lower bound (black dashed line)

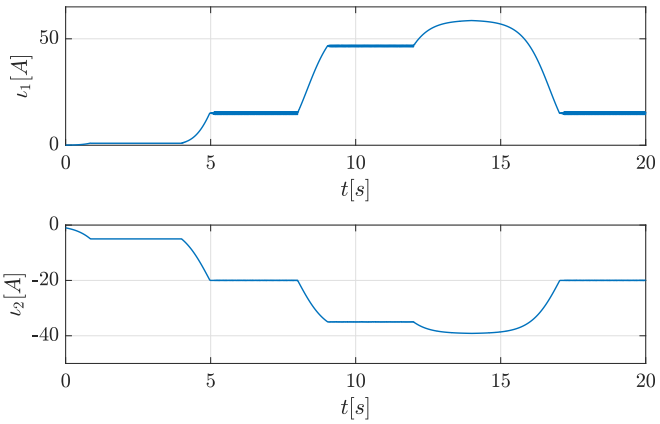

Fig. 6: From the top: time evolution of the current ι_1; time evolution of the current ι_2

current, in practice, it is often required that duty cycle u is saturated to an upper bound lower than 1. In the present example the maximum allowed duty cycle $\bar{u}$ is equal to 0.6. The duty cycle is obtained by inversion of the linear transformation in (6), where the symmetric set is designed with $U = 1$. Choosing the sliding function as in (8), with reference to equations (1) and (9), one has

$$f_1 = \frac{1}{C_2}\left[-\left(\frac{R_s}{L_2} + \frac{1}{RC_2}\right)\dot{\imath}_2 - \left(\frac{1}{L_2} - \frac{1}{R^2C_2}\right)\dot{v}_2 - \left((\tilde{u} - U)\frac{\bar{u}}{2U} + \bar{u}\right)\frac{\dot{v}_2}{L_2}\right]$$
$$f_2 = -\frac{1}{L_2C_2}\frac{\bar{u}}{2U}v_1.$$

It must be noted that the exact knowledge of f_1 and f_2 is not required for the design of the control algorithm. In fact, only estimation of the bounds K_m, K_M and C in (10) is required. The 3-SMC algorithm in (12) has been chosen to generate the discontinuous control law v with $\alpha = -1$, $\beta_1 = 100$ and $\beta_2 = 4000$, with the value of α being negative to compensate the negative sign of f_2. Furthermore, the BIC algorithm has been implemented as in (15) with parameters $k = 100$, $k_I = 1$ and $m = 2$.

Starting from $v_2(0) = 10V$, the reference output voltage is initially set to $-50V$. As it is shown in Figure 4 (bottom), the output voltage is regulated at the desired value through the action of the 3-SMC combined with the BIC algorithm. The evolution of the BIC output $\tilde{u}$ and the actual duty cycle u are shown in Figure 5, while the converter currents response are presented in Figure 6. At $t = 4s$ the output voltage reference is instantaneously decreased to $-200V$, and it is further decreased at $t = 8s$ to $-350V$. In both cases, the proposed algorithm manages to regulate the output voltage to the desired value without reaching the duty cycle saturation limit. As indicated in Figure 6, the decrease of the voltage reference causes the increase of the current flowing through the converter. From $t = 12s$ to $t = 14s$, the reference is selected as $\bar{v}_2 = -480V$, which causes the saturation of the duty cycle. In fact, as it is shown in Figure 5, the BIC saturates its output to its upper bound, which causes the duty cycle to reach its maximum allowed value $\bar{u}$. While such saturation prevents the achievement of the control objective, it allows to keep the converter current limited. Finally, after $t = 14s$, the reference is chosen again to be $-200V$, the BIC algorithm correctly desaturates, and the output voltage is regulated at the new desired value.

VI. Conclusions

This paper proposed a possible solution to the problem of controlling of a class of DC/DC converters through saturated higher order sliding mode control strategies. Such alternative approach is based on the so-called BIC algorithm, classically used to replace integral control, and here recast into the SMC framework. Specifically, the BIC is used in place of the classical integrator when designing a continuous 3-SMC, with the aim of stabilizing the output voltage of DC/DC converters while ensuring smoothness and boundedness of the duty cycle. The effectiveness of the proposed approach has been assessed in simulation with a Cúk converter model.

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