Journal of Instrumentation

PAPER • OPEN ACCESS

The SparkPix-S ASIC for the sparsified readout of 1 MHz frame-rate X-ray cameras at LCLS-II: pixel design and simulation results

To cite this article: L. Rota *et al* 2024 *JINST* **19** C01010

Jinst

Published by IOP Publishing for Sissa Medialab

Received: *July 24, 2023*
Accepted: *November 29, 2023*
Published: *January 15, 2024*

24th International Workshop on Radiation Imaging Detectors
Oslo, Norway
25–29 June 2023

The SparkPix-S ASIC for the sparsified readout of 1 MHz frame-rate X-ray cameras at LCLS-II: pixel design and simulation results

L. Rota,[a] F. Mele,[b,c,*] A. Habib,[a] H. Kim,[a] P. King,[a] B. Markovic,[a] A. Peña Perez[a] and A. Dragone[a]

[a] *SLAC National Accelerator Laboratory, Sand Hill Road, Menlo Park, California, U.S.A.*
[b] *Politecnico di Milano, Via Anzani, Como, Italy*
[c] *INFN-Milano, Via Celoria, Milan, Italy*

E-mail: filippo.mele@polimi.it

Abstract: Exploiting the "sparse" nature of the information in XPCS (X-ray Photon Correlation Spectroscopy) and XSVS (Speckle Visibility Spectroscopy) experiments, we present the SparkPix-S, a 3-sides buttable Application Specific Integrated Circuit (ASIC) based on a sparsified readout strategy for large-format hybrid detectors. The SparkPix-S architecture, based on the successful ePix family, will be composed as follows: a front-end 2-D matrix of 384×352 square pixels with 50 µm pitch is arranged to match the dimensions of a PIN Si-sensor matrix; charge readout, signal shaping and amplitude discrimination is performed at pixel-level, by means of a low-power (<18 µW) analog processor, which, in case of an event, negotiates access to an analog bus placed every other column; on the chip periphery (balcony), the information on each bus is digitized by an array of successive approximation analog-to-digital converters (SAR-ADCs) running at 10 Msps; on the digital back-end the global logic will generate the output data stream using low-voltage differential signalling (LVDS). A first prototype of the SparkPix-S, with a reduced matrix size of 96×96 pixels, is currently under production on a 130 nm CMOS technology. Simulated performance results show an equivalent noise charge <60 el. r.m.s. at 1 MHz repetition rate, with a maximum input energy of 60 keV and capability to discriminate charge signals with equivalent energy as low as 900 eV.

Keywords: Front-end electronics for detector readout; VLSI circuits; Pixelated detectors and associated VLSI electronics; X-ray detectors

*Corresponding author.

https://doi.org/10.1088/1748-0221/19/01/C01010

2024 JINST 19 C01010

Contents

2024 JINST 19 C01010

1 Introduction

With a unique capability of producing X-ray pulses at 1 MHz repetition rate, the upgrade of the Linac Coherent Light Source (LCLS-II) at the SLAC National Accelerator Laboratory will offer the potential to significantly advance several areas of X-ray science [1]. Experiments based on X-ray Photon Correlation Spectroscopy (XPCS) and Speckle Visibility Spectroscopy (XSVS) for the study of spontaneous fluctuations at the atomic scale, and stochastic fluctuations of matter on ultra-fast timescales, will require a new generation of 2D detectors with fine spatial resolution (<50 µm), single-photon discrimination capability in the soft and tender X-ray energy range, and the possibility to operate at the full 1 MHz repetition rate of LCLS-II.

However, for a 1 Mpixel camera capable of running at 1 MHz frame-rate, the expected data throughput for a full-frame readout ranges in the order of several Tb/s, rising significant concerns in terms of data processing and analysis capability. The new family of SparkPix application specific integrated circuits (ASICs), aims at tackling the 1 MHz frame-rate challenge for large-area and high-resolution detectors, realizing revolutionary experiment-specific x-ray cameras, with advanced information extraction features. For XPCS and XSVS experiments with such a small pixel dimension, the expected average frame occupancy is around 0.05%, with a shot-to-shot occupancy still largely below 1% (see figure 1). Only in some unlikely pattern conditions, a 10% frame occupancy can be recorded for a limited amount of time. Given the sparse nature of the information in these experiments, we designed the SparkPix-S, a 3-sides buttable Application Specific Integrated Circuit (ASIC) based on a sparsified readout strategy for large-format hybrid detectors, which is presented in the following sections.

2 The SparkPix-S architecture

The sparsification strategy in the SparkPix-S will allow a massive reduction of the data-rate, from several Tb/s to few tens of Gb/s. However, moving away from a full-frame readout brings several design and architectural challenges. The analog readout and trigger circuitry must be sufficiently

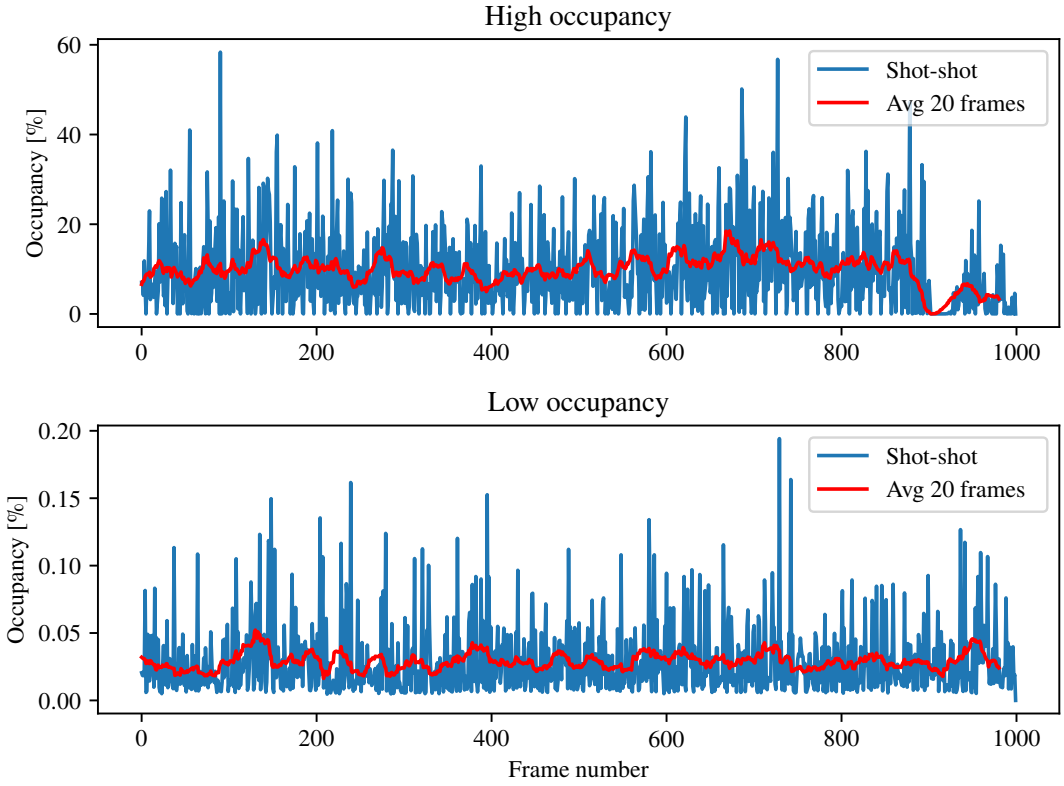

Figure 1. Representative samples of high (top) and low (bottom) frame occupancy in XPCS experiments over 1000 frames. Dataset courtesy of Y. Sun and C. Hansson.

low-noise to effectively discriminate small fractions of photons, which will be largely affected by charge sharing effects due to the small pixel size. Calibration of background noise will become more difficult, and the handling of shared resources in over-occupancy scenarios is fundamental. Moreover, even if the SparkPix-S ASIC is designed for a PIN Si-sensor matrix, compatibility with other sensors, such as low-gain avalanche diodes (LGADs) — intended to extend the low-energy range of the camera — should be planned ahead for future phases of the project. The main requirements for the current phase are summarized in table 1.

The SparkPix-S architecture, is based on the successful ePix family [2, 3], which allows an efficient reuse of interface and configuration hardware blocks, firmware and test resources. A front-end 2-D matrix of 384×352 square pixels with 50 µm pitch is arranged to match the pitch of a larger Si-sensor, realizing a 3-sides buttable layout, with the fourth side (balcony) being devoted to back-end signal processing and data transmission. The final camera size, composed tiling several sensors, is expected to have between 0.5 and 2 Mpixels. A schematic representation of the SparkPix-S architecture is shown in figure 2. The readout pixel cell is characterized by a full-analog architecture, described in the following section. On the balcony, the information is digitized by an array of column-parallel successive approximation analog-to-digital converters (SAR-ADCs), for a total of 192 ADCs per ASIC. Each ADC runs at 10 Msps with a 10-bit nominal resolution. The global logic will generate the output data stream using low-voltage differential signalling (LVDS) at 1 Gbps. Timing constraints are designed to match the 1% occupancy, which is largely sufficient for most of

Parameter	Specification
Technology	CMOS 130 nm
Maximum frame-rate	1 MHz
Maximum frame-occupancy (pixel-hit/frame)	<1%
Input photon energy range	4–12 keV
Frame occupancy	<1%
Pixel size	50×50 μm^2
Full-reticle geometry	384×352 pixels (3-sides buttable)
Maximum input signal	60 keV (5 photons pile-up)
Minimum detectable signal	1 keV (1/4 photon)
Equivalent noise charge (ENC)	<60 el. rms
Power consumption	<1 W/cm^2 (≃15μW/pixel)
Shaping filter	5τ correlated double sampling (CDS)

Table 1. Summary of main specifications of the SparkPix-S ASIC.

operative cases. In the unlikely conditions of over-occupancy (or when dealing with high-occupancy patterns), the SparkPix-S can be configured to respond in two modes. The first option is to flush the excess data, reducing the output image size. Alternatively, the system can be paralyzed until all triggered pixels are readout by the user, effectively reducing the output frame-rate to few kHz. In both cases, a flag notifies the data acquisition system (DAQ) of the specific occurrence.

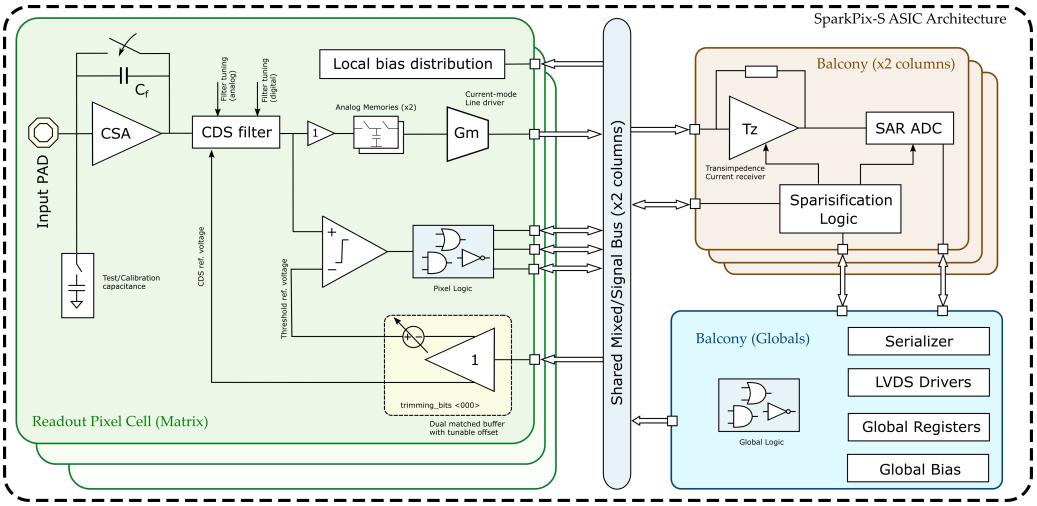

Figure 2. Simplified schematic of the SparkPix-S ASIC architecture.

3 Pixel read-out architecture

The first block of the readout pixel cell is a fixed-gain charge sensitive amplifier (CSA) working in pulsed-reset mode [4] with a test-input capacitance for calibration purposes. After the preamplifier

reset (150 ns), the following correlated double sampling filter (CDS) processes the CSA output signal, with a 5-τ sub-optimal shaping [5], to minimize gain sensitivity with respect to the filter time-constant over PVT variations. The CDS includes analog and digital controls for both fine and coarse global tuning of the shaping time. The output of the CDS filter is fed to a threshold comparator block, which, when an event is detected, triggers the analog-sampling and subsequent pixel readout procedure. The voltage references for the CDS filter and for the comparator are generated from a single global reference line, using a matched-pair of local buffers with tunable offset, minimizing the number of bits needed for threshold trimming. The presence of two analog memories allows for a ping-pong read/write process, increasing the effective throughput.

After each frame, a digital token is passed along every other column to negotiate the access a shared analog bus, which connects the pixel cells to the balcony receiving blocks. Pixels which request access to the bus retain the token for the time required for the data transmission, before forwarding the token to the following pixel. Transmission between the pixel and the back-end is performed in current mode to reduce capacitive cross-talk [6, 7], using a high-linearity transconductance driver and a transimpedance receiving stage.

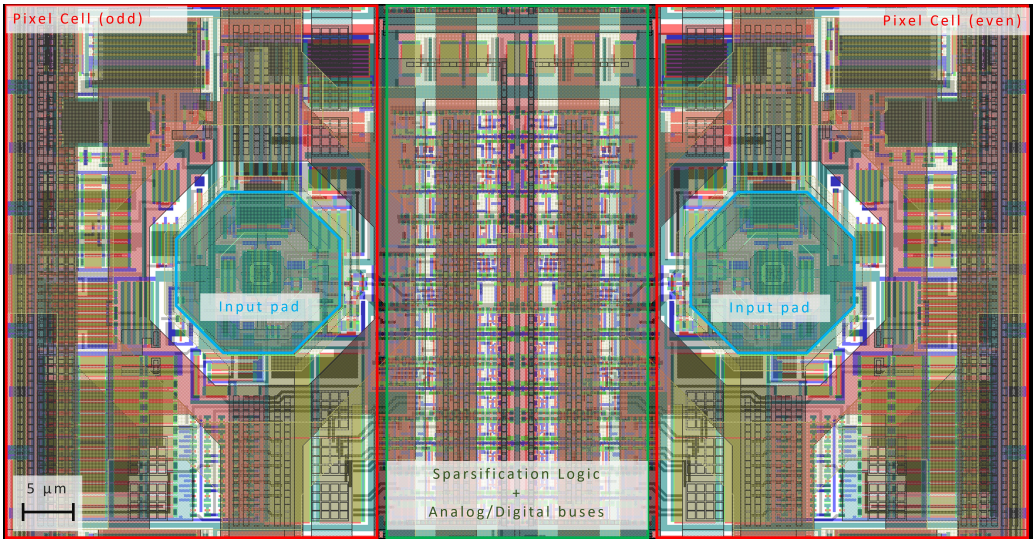

Figure 3. Detail of the layout of two readout pixels cells in the SparkPix-S matrix. Odd and even columns are characterized by symmetrical layout, which allows easier access to shared resources.

4 Prototype physical layout

A reduced 96×96 matrix prototype is currently under production on a 130 nm CMOS technology by TSMC. A detail of the layout of two adjacent pixel cells in the SparkPix-S matrix is shown in figure 3. Due to the small pixel pitch, a large fraction of the higher metal layers are occupied by the octagonal input pads, increasing the complexity of the power mesh. The design of a fully-analog readout cell helps to reduce injections from the high-frequency clock in the digitally-intensive back-end balcony, and allows to allocate more space for the physical layout of the analog core within the tight area constraints of each pixel. In addition to the analog/digital 1.2 V supplies and ground lanes,

2024 JINST 19 C01010

a dedicated 0.6 V voltage source supply (VSS), for the high-transconductance front-end devices, is distributed across the matrix, to the minimize on-chip power dissipation. Between every other column, a central trench is dedicated for the analog/digital busses, spare-logic and local clusters of bias regeneration and filtering.

5 Simulation results

Post-layout simulation of the SparkPix-S readout cell, including the back-end transimpedance amplifier and the ADC, show a nominal equivalent noise charge of less than 56 electrons rms. The expected noise level will to allow to set the noise threshold down to 900 eV, enabling coincidence analysis and charge reconstruction across neighbor pixel for charge sharing down to ¼ of photon. The effective conversion gain at the ADC input is of 165 mV/fC, while the power consumption is around 18 µW/pixel. The non-linearity error is below 1% for the maximum single-photon energy range (12 keV), which will represent the most frequent case in low-occupancy scenarios, as shown in figure 4. An acceptable compression of 10% is expected for energies up to 60 keV, resulting from the unlikely event of 5 photons pile-up.

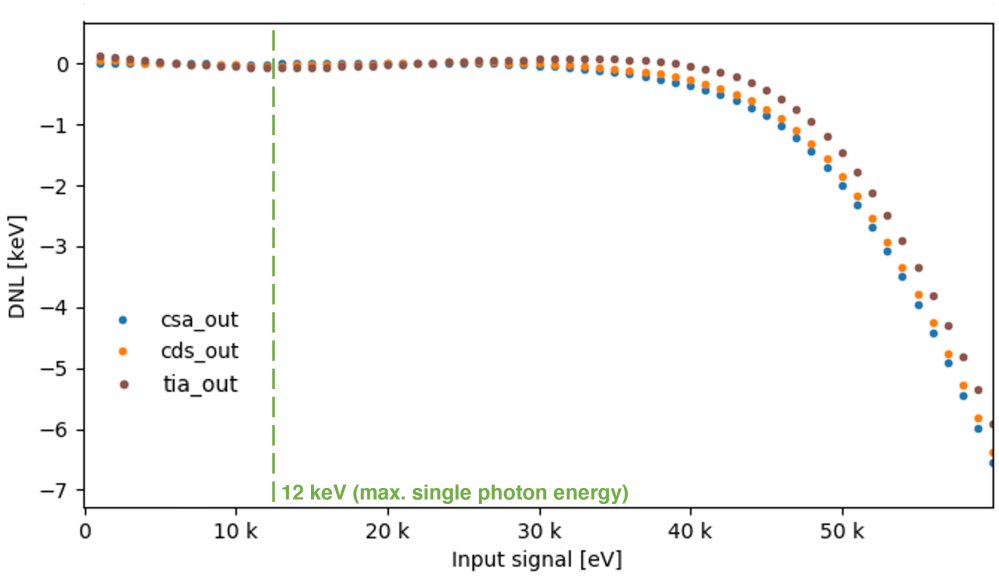

Figure 4. Differential non-linearity plot simulated at the output of the charge sensitive amplifier (csa_out), correlated double sampling filter (cds_out), and transimpedance output (tia_out) respectively.

Acknowledgments

This work was supported in part by the Italian Ministry for University and Research (MUR) and by the European Union (EU) under the project FSE REACT-EU, PON Ricerca e Innovazione 2014-2020-DM 1062/2021.

2024 JINST 19 C01010

References

[1] P. Abbamonte et al., *New science opportunities enabled by LCLS-II X-ray lasers*, Tech. Rep., SLAC National Accelerator Lab., Menlo Park, CA, U.S.A. (2015).

[2] A. Dragone et al., *ePix: a class of front-end ASICs for second generation LCLS integrating hybrid pixel detectors*, in the proceedings of the *2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC)*, Seoul, Republic of Korea (2013), p. 1–5 [DOI:10.1109/NSSMIC.2013.6829505].

[3] A. Dragone et al., *ePix: a class of architectures for second generation LCLS cameras*, *J. Phys. Conf. Ser.* **493** (2014) 012012.

[4] F. Mele, J. Quercia and G. Bertuccio, *Analytical Model of the Discharge Transient in Pulsed-Reset Charge-Sensitive Amplifiers*, *IEEE Trans. Nucl. Sci.* **68** (2021) 1511.

[5] E. Gatti, P.F. Manfredi, M. Sampietro and V. Speziali, *Suboptimal filtering of* $1/f$ *noise in detector charge measurements*, *Nucl. Instrum. Meth. A* **297** (1990) 467.

[6] F. Mele et al., *ORION, a Multichip Readout Electronics for Satellite Wide Energy Range X-/γ-Ray Imaging Spectroscopy: Design and Characterization of the Analog Section*, *IEEE Trans. Nucl. Sci.* **68** (2021) 2801.

[7] M. Gandola, F. Mele, M. Grassi, P. Malcovati and G. Bertuccio, *Multi-chip front-end electronics lyra for x and γ ray detector for hermes mission*, 2021 *JINST* **16** T12013.

2024 JINST 19 C01010