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Innovative Fault Current Evaluation Method for Active DC Grids

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Abstract: DC smart grids are a promising solution for the efficient integration of renewable energy sources and loads. Still, their widespread adoption is hindered by significant challenges related to fault response, identification, and clearance. The traditional DC fault analysis method is a useful tool for straightforwardly understanding the behaviour of fault current contributions from DC converters in LVDC networks during a fault. However, when a system with multiple converters and non-negligible fault impedance need to be considered, its accuracy is severely limited due to the assumptions included in the problem solution, thus leading to the following: (a) the dependency of the results' reliability on fault impedance values and/or other converter fault current contributions; (b) the inaccuracy of the diode current estimation; and (c) the inaccuracy of the conductor joule integral. Thus, these results' data may be unreliable for designing protection systems for one converter or for an entire network. In order to overcome these issues, this paper proposes an innovative, simple numerical approach to DC fault current evaluation, which can be adopted when the number of converters become significant, or the network is complex. This method arises from the primary interest in solving the circuit to extract the indicators (current peak value and time, joule integral, etc.) necessary for designing circuit protections. This approach proved to grant two main advantages over traditional methods: (a) it provides accurate results, with no need to introduce any specific assumption; (b) it can be structured to manage an arbitrary number of converters; and (c) it reduces the computational processing times and resources necessary to simulate an entire DC network in comparison to other circuit solution software.

Keywords: DC smart grids; LVDC distribution network; DC fault current assessment; non-zero impedance fault analysis; numerical methods

Citation: Valbuena Godoy, J.; Negri, S.; Oliva, F.; Antoniazzi, A.; Faranda, R. Innovative Fault Current Evaluation Method for Active Direct Current Grids. *Electronics* **2024**, *1*, 0. https://doi.org/

Academic Editors: Antonio Di Bartolomeo, Fortunato Pezzimenti, Alessandro Ruvio, Gianpaolo Vitale and Davide Astolfi

Received: 29 January 2024
Revised: 14 February 2024
Accepted: 20 February 2024
Published:

1. Introduction

Within the ever-evolving landscape of the electricity sector, direct current (DC) smart grids have increasingly been reincluded in the paradigm of electrical power utilization, thus coming back to the historical dilemma between alternating current (AC) and DC networks that has persisted since the first conceptions of energy transportation and distribution [1]. The distinct advantages of DC smart grids become increasingly evident as the demand for cleaner energy solutions rises, and the proximity of energy generation and consumption becomes more common [2,3]. In comparison with existing AC distribution networks, low-voltage direct current (LVDC) systems offer opportunities to enhance the efficiency, reliability, and control simplicity of power distribution. This is relevant for many applications, from renewable energy communities [4] to electrification in developing countries [5], thus playing a pivotal role in shaping the future of the electricity sector; the

comprehensive exploration of LVDC systems requires a deeper understanding of their nuances and challenges, one of which is the protection of the system in case of a fault [6,7].

Despite the advantages related to the introduction of DC smart grids, protecting these systems presents more demanding technical challenges compared to their AC counterparts. In general, for DC networks at any voltage level, electric arcs resulting from a fault can persist for very long periods because, differently from AC networks, arc extinction cannot rely on natural current zero crossings, which are absent in DC current waveforms [8]. Specifically, in LVDC networks dominated by voltage source converters (VSCs), the first system reaction to a fault is the converters' capacitor discharge, which can lead to a very high short-circuit current. Additionally, the series impedance of DC lines is typically lower than that of AC lines, thus leading to a rapid surge in fault current. As a consequence, a DC system must face the challenge of shorter fault current rise times, thereby making it difficult to avoid reaching the prospective fault current peak values using mechanical circuit breakers with longer interruption times [9,10]. Furthermore, freewheeling diodes associated with the network converters may experience uncontrollable overcurrents depending on the converter topology and network parameters. Despite the rapid opening of IGBTs in converters, in many circumstances, freewheeling diodes cannot be excluded by the fault current path such that a substantial oversizing is necessary to prevent semiconductor damage.

In this context, evaluating the response of each converter connected to the DC network in the case of a fault is essential to correctly evaluate fault currents and losses [11] and, in turn, to design a proper protection system for the network. In the literature, this issue is commonly addressed by considering an equivalent circuit, including converters, conductors, and other relevant circuit elements, if any, which is then solved by means of one or more ordinary differential equations (ODEs). A quite mature study about this is presented in [12,13], where the fault analysis of a VSC in a high-voltage DC (HVDC) network is detailed, thus distinguishing different fault stages and providing expressions for the line current and converter terminals' voltage for each stage. In this paper, we will refer to this approach as the traditional DC fault analysis method. Indeed, this approach is the most widely adopted and many slight variations to it are known depending on the specific converter under analysis, voltage level, and grounding configuration. This is the case of [14,15], where, fault analysis was presented for an LVDC network considering different grounding configurations, and fault analysis and protections for an underwater HVDC network cables are discussed. Additional variations include fault analysis of series-connected DC collection systems [16] and the design of DC breakers based on DC fault current calculations [17,18]. However, these studies are limited, similarly to the traditional DC fault analysis, to systems with just one converter, or to faults with negligible fault resistance. In addition, the literature has approached the joint analysis of the response under the fault of multiple converters, as shown in [19,20] for a multi-port DC–DC converter and in [21] for a DC network with more than three converters. However, these studies do not reach a general solution, since [19] does not provide analytical expressions for each fault current, while [21], even though considering a network with multiple converters, is still focused on the fault current contribution of a single converter. Therefore, extending this method to an arbitrary number of converters is difficult, considering that the joint response of multiple converters implies that the ODE system to solve the circuit becomes too large. As a consequence, the results could be accurate only if the analysis becomes quite cumbersome, and the problem becomes exponentially worse as the number of converters increases. Due to this limitation, this approach is applied for DC networks with multiple converters only for the case where the fault impedance is nearly zero [22].

Regarding these limitations, fault assessment is often mainly focused on the maximum fault current values that can be generated in the case of a fault to establish the protections settings. This is shown in [23], where the technologies addressing the previously mentioned issues for DC grids protection are explored. However, as demonstrated in [24], when it comes to establishing a protection coordination scheme for a DC smart grid, a more

accurate fault current evaluation is needed. Only in this case is the development of a precise protection strategy possible, thereby enabling the selective activation of protective devices. Indeed, similarly to AC networks, the protection selectivity is crucial for isolating the fault and minimizing disruption to the rest of the system. However, for DC systems, an extension of the traditional DC fault analysis method aimed at a generalized solution, not tied to the aforementioned limitations, is required.

In this context, this paper presents an innovative method based on numerical techniques for the comprehensive assessment of a DC network's response under fault. Indeed, numerical methods has been previously considered for DC grids, as discussed in [25]. However, that study focused on an HVDC network, where many elements in the equivalent circuit could be neglected due to the long distances of the conductors, and where rapid transient behaviors and stages with different dynamics were not present. In contrast, the innovative method presented in this study is tuned for LVDC networks, starting from the same characterization performed in the traditional approach and solving the entire network in a general manner, i.e., without restrictions and assumptions. The remaining part of the paper is organized as follows: in Section 2, the traditional DC fault approach is detailed, including theoretical modeling, application in a study case, and discussion on the limitations resulting from this method. Next, in Section 3, a general solution for DC faults consisting of a numerical solution approach based on solving the circuit ODEs system through the Euler approximation is presented. Thus, this Section includes the procedures to obtain the necessary equations, the methodologies to apply them to a specific case study, and the demonstration of their effectiveness and discussion of the results for a specific study case. Lastly, final conclusions are reported in Section 4.

2. Traditional DC Fault Analysis

As mentioned, following the literature, the fault analysis of DC grids has to be performed by solving an entire network, thereby evaluating the behavior of each converter at the same time. To reach this result through the traditional DC fault analysis method is very complex, and it is generally simplified by writing current and voltage expressions under the hypothesis that the fault response of each converter can be defined exclusively by the fault impedance and the circuit elements between the converter terminals and the fault. This simplification, however, produces accurate results only when the residual fault voltage is very small, or in other quite rare cases. Therefore, the results obtained by this method cannot be generalized to all the network status cases. However, it is worth recalling this method in detail, as it will serve as a starting point to propose a general solution for DC fault analysis. In particular, this Section is devoted to discussing the traditional DC fault analysis method and highlighting its limitations.

2.1. Background and Methodology

The traditional approach to DC fault analysis is based on the assumption that when a fault occurs in a DC network, the response of each power converter connected to the DC network can be described by three different stages, which are named as follows: capacitor discharge, diode freewheeling, and fault steady state; these are described in [26]. The characteristics of these stages and how current and voltage expressions can be obtained are discussed on the following subsections.

2.1.1. Capacitor Discharge Stage: Traditional Approach

Let us consider a DC system with N converters and assume that we aim to determine the fault current contribution from the ith converter. This stage begins immediately after the fault occurs at $(t = 0)$. Due to the very fast discharge dynamics in this phase, the converter control effect has to be considered negligible. This consideration allows for generalizing the behavior of power converters during this stage. Therefore, each converter can be approximated as a simple RLC circuit, and each fault current is equal to the capacitor discharge current.

With no loss of generality, let us consider the equivalent circuit corresponding to the capacitor discharge fault phase for the *i*th converter for the case of a pole-to-pole fault, as shown in Figure 1. Note that only one resistive element and one inductive element are included to represent the conductors from the converter terminals to the fault section. For this study, it must be assumed that the values of R_{DC_i} and L_{DC_i} include both the equivalent of the positive pole conductor and that of the negative pole conductor. For this kind of analysis, in order to obtain realistic results when the fault is close to the converter terminals, it is necessary to consider some parasitic elements of a real capacitor. Therefore, the capacitor model here adopted includes its equivalent series resistor (ESR) and its equivalent series inductance (ESL) only.

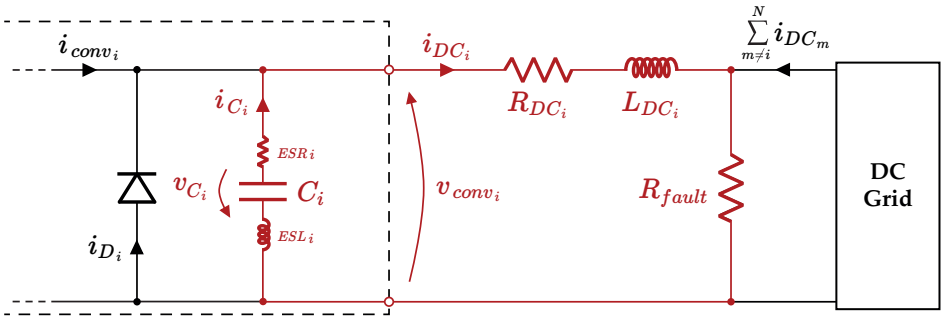


Figure 1. Equivalent circuit corresponding to the capacitor discharge fault stage for the *i*th converter.

Typically, the initial conditions for the circuit reported in Figure 1 are the values of the line inductance current and of the capacitor voltage at the instant when the fault occurs at $i_{DC_i}(0^-)$ and $v_{C_i}(0^-)$, which are both assumed to be constant. The DC converter current i_{conv_i} is assumed to be constant for the whole transient duration and equal to the initial condition $i_{DC_i}(0^-)$. Recognizing that the diode current i_{D_i} has to be null during this stage, by Kirchhoff's current law (KCL), the DC current i_{DC_i} becomes equal to sum of the converter capacitor discharge current i_{C_i} and of the constant converter current i_{conv_i}. Therefore, it is possible to write the ODEs, which provide the equivalent circuit solution considering the converter capacitor constitutive relation and the Kirchhoff's voltage law (KVL) on the only mesh in evidence shown in Figure 1, thereby resulting in the following:

$$i_{DC_i}(t) = i_{C_i}(t) + i_{conv_i} = C_i \cdot \frac{d}{dt} v_{C_i}(t) + i_{DC_i}(0^-), \tag{1}$$

$$v_{C_i}(t) + R'_{DC_i} \cdot i_{DC_i}(t) + L'_{DC_i} \cdot \frac{d}{dt} i_{DC_i}(t) = -R_{fault} \cdot \sum_{m\neq i}^{N} i_{DC_m}(t), \tag{2}$$

where R'_{DC_i} is the sum of the resistances in the circuit loop ($R'_{DC_i} = R_{DC_i} + ESR_i + R_{fault}$), and L'_{DC_i} is the sum of the inductances ($L'_{DC_i} = L_{DC_i} + ESL_i$). Note that the right term of (2) is equal to zero if only one converter is included in the DC system under analysis, while, in case more converters are present, it depends on the fault current contribution of the other $N-1$ converters connected to the DC network.

As previously discussed, in traditional fault analysis, R_{fault} is close to zero, so the right term of (2) becomes negligible (the impact of non-zero fault resistance on fault current calculation accuracy will be addressed later on in Section 2.3.1). Then, combining (1) and (2), a second-order ODE is obtained, which allows for the determination of the fault current i_{DC_i} according to the following:

$$\frac{d^2}{dt^2} i_{DC_i}(t) + 2 \cdot \alpha_i \cdot \frac{d}{dt} i_{DC_i}(t) + \omega_{0_i}^2 \cdot i_{DC_i}(t) = \omega_{0_i}^2 \cdot i_{DC_i}(0^-), \tag{3}$$

where α_i is the decay factor, which is defined as follows:

$$\alpha_i = \frac{R'_{DC_i}}{2 \cdot L'_{DC_i}} \tag{4}$$

and ω_{0_i} is the undamped resonance frequency, which is defined as follows:

$$\omega_{0_i} = \sqrt{\frac{1}{L'_{DC_i} \cdot C_i}}. \tag{5}$$

The converter fault current can be obtained from (3) as follows:

$$i_{DC_i}(t) = \frac{v_{C_i}(0^-)}{L'_{DC_i} \cdot (s_{1_i} - s_{2_i})} \cdot \left(e^{s_{1_i} \cdot t} - e^{s_{2_i} \cdot t}\right) + \frac{i_{DC_i}(0^-)}{s_{1_i} - s_{2_i}} \cdot \left(s_{1_i} \cdot e^{s_{1_i} \cdot t} - s_{2_i} \cdot e^{s_{2_i} \cdot t}\right) + i_{DC_i}(0^-), \tag{6}$$

where s_{1_i} and s_{2_i} are defined as follows:

$$s_{1,2_i} = -\alpha_i \pm \sqrt{\alpha_i^2 - \omega_{0_i}^2}, \tag{7}$$

and where $i_{DC_i}(0^-)$, equal to i_{conv_i}, and $v_{C_i}(0^-)$ are the current and voltage initial conditions, respectively. By substituting (6) in (1), the solution for the capacitor voltage is obtained, thus resulting in the following:

$$v_{C_i}(t) = -\frac{i_{DC_i}(0^-)}{C_i \cdot (s_{1_i} - s_{2_i})} \cdot \left(e^{s_{1_i} \cdot t} - e^{s_{2_i} \cdot t}\right) - \frac{v_{C_i}(0^-)}{s_{1_i} - s_{2_i}} \cdot \left(s_{2_i} \cdot e^{s_{1_i} \cdot t} - s_{1_i} \cdot e^{s_{2_i} \cdot t}\right). \tag{8}$$

Depending on the values of the RLC circuit parameters, the system may or may not exhibit oscillatory behavior. This is reflected in s_1 and s_2 as the corresponding root values appearing real or as complex conjugate pairs. Therefore, the system response will be over damped in the case where $\alpha_i > \omega_{0_i}$, critically damped in the case where $\alpha_i = \omega_{0_i}$, or under damped (oscillatory) in the case where $\alpha_i < \omega_{0_i}$.

Lastly, considering that the capacitor ESL value is usually very small, hence not affecting the voltage at the converter terminals significantly, the voltage at the ith converter terminals can be obtained as follows:

$$v_{conv_i}(t) \approx -v_{C_i}(t) - ESR_i \cdot i_{DC_i}(t). \tag{9}$$

In the traditional approach, these equations represent the circuit variables until v_{conv_i} reaches the threshold voltage of the converter diode(s) (typically around $V_d = 0.8$ V for high-power diodes [27]), thereby causing the diodes to enter conduction mode. This does not happen in all cases, but it occurs only if the transient exhibits oscillatory behavior (under damped), and the converter voltage becomes negative.

The capacitor discharge stage is particularly relevant for DC system fault analysis, inasmuch as even though this phase is usually short (a few milliseconds), it is characterized by high fault current values. The capacitor discharge phase can end in two different ways depending on the specific fault parameters:

(a) If the voltage at the ith converter terminals does not oscillate, or the oscillation is damped enough for the voltage to not reach negative values, in those cases the transient follows its natural decay, and the fault evolves directly from the capacitor discharge phase to the steady state stage; there then is no need to consider other equations to solve the system, as the two stages use the same equations;

(b) If the voltage at the ith converter terminals does oscillate, and the oscillation is large enough for the voltage to reach negative values, then the converter diode(s) connected in parallel to the capacitor enter into conduction mode. After that, a new fault stage starts, which is called the diode freewheeling stage. The instant when the voltage across the diode reaches its threshold value, named hereon t_{on}, can be evaluated by (9), thereby imposing

that the converter voltage v_{conv_i} is equal to the diode threshold voltage V_d. Therefore, the initial conditions for the next stage can be considered for $v_{C_i}(t_{\text{on}}) = V_d$ and $i_{DC_i}(t_{\text{on}})$, as evaluated by (6).

2.1.2. Diode Freewheeling Stage: Traditional Approach

As described at the end of the previous section, the diode freewheeling stage is established at the end of the capacitor discharge phase if the voltage at the ith converter terminals v_{conv_i} does oscillate, and the oscillation is large enough for the voltage to reach negative values. The diode freewheeling stage begins when the voltage across the diode reaches its threshold value, and here, that instant is named t_{on}. As discussed in the previous subsection, the value of t_{on} is obtained by (9). During this stage, the fault current flows through the converter diode(s), and it is established close the peak of the capacitor discharge current, thereby resulting in possibly high current values, which constitutes a possible risk of diode(s) damage. As a consequence, assessing this current is crucial for fault analysis and converter protection.

Using highly accurate models, such as the Shockley exponential model (non-linear), for solving the equivalent circuit with a turned-on diode can be quite complex. Therefore, as often shown in [28], a model with an ideal diode in a series with a voltage source is used to simplify calculations. Considering that the diode in this stage is in conduction mode, for this approach, the diode model will be represented only by using a voltage source (V_d) and a current-limiting resistor (r_d), as depicted in Figure 2, where the equivalent circuit for the diode freewheeling stage is reported. These values can be obtained by linearizing the exponential function of the diode at the working point or directly from the bulk voltage and bulk resistance in the diode datasheet [27].

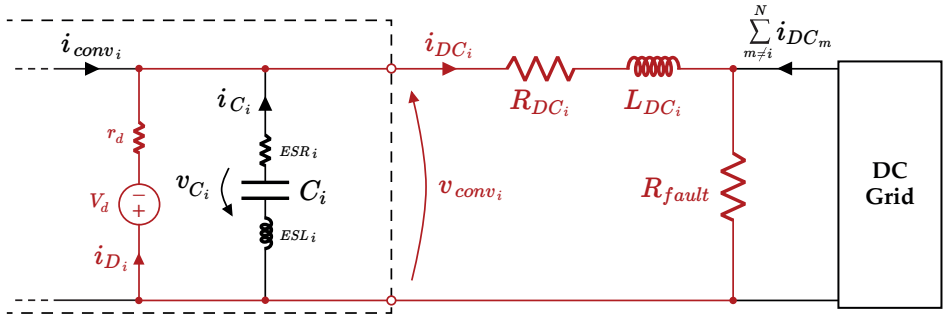


Figure 2. Equivalent circuit corresponding to the freewheeling fault stage for the ith converter.

The analysis of this circuit is different from the previous one, as in this case, there are two branches instead of just one loop sharing the same current. In order to simplify the calculations for this stage, the fault current is assumed to flow exclusively through the diode branch and not through the capacitor branch, so the capacitor current i_{C_i} is null, and $i_{DC_i}(t) = i_{D_i}(t) + i_{conv_i}$. Thus, the expression for the fault current i_{DC_i} is as follows:

$$V_d + r_d \cdot i_{D_i}(t) + (R_{DC_i} + R_{fault}) \cdot i_{DC_i}(t) + L_{DC_i} \cdot \frac{d}{dt} i_{DC_i}(t) = -R_{fault} \cdot \sum_{m \neq i}^{N} i_{DC_m}(t). \quad (10)$$

The initial conditions for this stage circuit are determined on the basis of the fault current and capacitor voltage at the instant when the diode is turned on. These values are $i_{DC_i}(t_{\text{on}})$, which are obtained from (6) and by considering $v_{C_i}(t_{\text{on}}) = V_d$. As discussed in the previous subsection, the right term of (10) is considered negligible, and the current contribution i_{conv_i} from the upstream grid remains constant.

According to all of these considerations, and similarly to the capacitor discharge phase, the ODE that provides the equivalent circuit solution is obtained considering the KVL relative to the mesh highlighted in Figure 2. The resulting ODE is as follows:

$$\frac{d}{dt}i_{DC_i}(t) + \frac{R''_{DC_i}}{L_{DC_i}} \cdot i_{DC_i}(t) = \frac{r_d \cdot i_{conv_i} - v_{C_i}(t_{\text{on}})}{L_{DC_i}}, \tag{11}$$

where R''_{DC_i} is the sum of the resistances in the circuit loop ($R''_{DC_i} = R_{DC_i} + r_d + R_{fault}$). Thus, the fault current expression for this stage is obtained by solving (11), thus resulting in the following:

$$i_{DC_i}(t) = i_{D_i}(t) = \left(\frac{v_{C_i}(t_{\text{on}})}{R''_{DC_i}} + i_{DC_i}(t_{\text{on}}) \right) \cdot e^{-\frac{R''_{DC_i}}{L_{DC_i}} \cdot (t - t_{\text{on}})} + \frac{r_d \cdot i_{conv_i} - v_{C_i}(t_{\text{on}})}{R''_{DC_i}}. \tag{12}$$

The voltage at the ith converter terminals is then obtained as follows:

$$v_{conv_i}(t) = v_{D_i}(t) = -v_{C_i}(t_{\text{on}}) - r_d \cdot i_{DC_i}(t). \tag{13}$$

Finally, this stage will end when the fault current in the diode is no longer capable of being maintained in conduction mode. This is determined by solving (13), which is when the voltage v_{conv_i} becomes smaller than the diode threshold voltage V_d. This instant (when the diode turns off and the fault steady state stage is established) is named t_{off}. In this instant, the fault current i_{DC_i} and capacitor voltage v_{C_i} are $i_{DC_i}(t_{\text{off}})$, which are evaluated by (12), and $v_{C_i}(t_{\text{off}}) = V_d$.

2.1.3. Fault Steady State Stage: Traditional Approach

After the diode freewheeling stage, one last transient stage is present, which is named fault steady state stage. In this stage, the same circuit used for the capacitor discharge stage, reported in Figure 1, can be used. As before, its solution is given by (6) for the current and (8) for the voltage, where now the initial conditions are, as described at the end of the previous section, $i_{DC_i}(t_{\text{off}})$, which is evaluated by (12), and $v_{C_i}(t_{\text{off}}) = V_d$. The resulting expressions for the fault current, capacitor voltage, and voltage at the converter terminals, respectively, are the following:

$$i_{DC_i}(t) = \frac{v_{C_i}(t_{\text{off}})}{L'_{DC_i} \cdot (s_{1_i} - s_{2_i})} \cdot \left(e^{s_{1_i} \cdot (t - t_{\text{off}})} - e^{s_{2_i} \cdot (t - t_{\text{off}})} \right) + \frac{i_{DC_i}(t_{\text{off}})}{s_{1_i} - s_{2_i}} \cdot \left(s_{1_i} \cdot e^{s_{1_i} \cdot (t - t_{\text{off}})} - s_{2_i} \cdot e^{s_{2_i} \cdot (t - t_{\text{off}})} \right) + i_{conv_i}, \tag{14}$$

$$v_{C_i}(t) = -\frac{i_{DC_i}(t_{\text{off}})}{C_i \cdot (s_{1_i} - s_{2_i})} \cdot \left(e^{s_{1_i} \cdot (t - t_{\text{off}})} - e^{s_{2_i} \cdot (t - t_{\text{off}})} \right) - \frac{v_{C_i}(t_{\text{off}})}{s_{1_i} - s_{2_i}} \cdot \left(s_{2_i} \cdot e^{s_{1_i} \cdot (t - t_{\text{off}})} - s_{1_i} \cdot e^{s_{2_i} \cdot (t - t_{\text{off}})} \right), \tag{15}$$

$$v_{conv_i}(t) \approx -v_{C_i}(t) - ESR_i \cdot i_{DC_i}(t). \tag{16}$$

It is worth recalling that, while the hypothesis of constant converter contribution to the fault current is reasonable for the first two stages of the fault response, which has a very fast dynamic, the converter fault current contribution is always considered to be slowly varying. This may not necessarily hold for this stage, especially for converters whose steady state fault current cannot be actively limited by the converter control. However, for some converters, this is not a major issue since, according to their control principles and capabilities, they can limit the current through a switching function. Consequently, they can avoid a supplying current in the case of a fault with a suitable control system or provide a limited, predefined current contribution. Nevertheless, this capability is not universal for all power converters. Considering the aim of this analysis, which is mainly focused on protection purposes, the effect of this stage is not very significant because of the following:

(a) The fault current values are usually much smaller than the ones experienced in the first two stages;

(b) Protections are usually required to trip before the fault steady state is established to avoid system damage, and the steady state fault current can be extinguished by tripping the AC side protection, which is not effective during the first two stages.

2.2. Case Study: Comparison between Traditional DC Fault Analysis Method and Numerical Simulations

In order to discuss the effectiveness and limitations of the traditional DC fault analysis approach previously discussed, an example of a LVDC network, as shown in Figure 3, which includes four converters with $V_{grid} = 800$ V of nominal voltage, is considered as a case study. The considered example of a DC network is composed of different converters, and all converters are assumed to have the capability to manage the converter contribution to the fault current when the fault steady state stage is reached. As a consequence, to simplify the calculations with no loss of generality, in this study, each converter current contribution i_{conv_i} has been considered to be null.

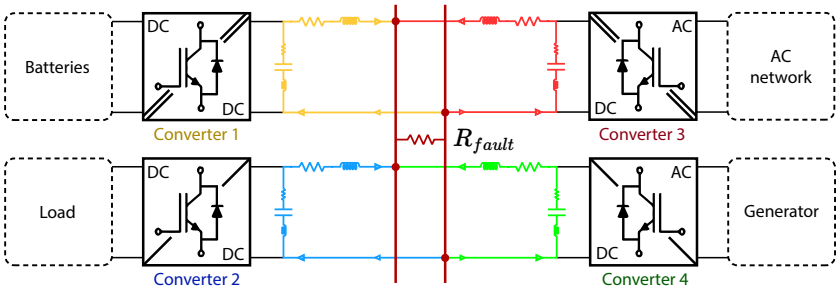


Figure 3. Considered example of DC network.

Several combinations of converter power (and, accordingly, output capacitors) and conductor length are here considered. In particular, converters 1 and 2 have capacitors and lines designed for a power that is three times less than that of converters 3 and 4.

Similarly, as far as line length is concerned, converters 1 and 3 are connected to conductors that are three times shorter than those of converters 2 and 4. The corresponding circuit parameters are shown in Table 1, including all the parameters needed for the equivalent circuits. Regarding the diode freewheeling stage, the considered diode model includes $V_d = 0.8$ V and $r_d = 0.108$ mΩ [27]. These values are used for all converter diodes.

Table 1. Circuit and physical parameters of the considered example DC grid.

Converter	Power [kW]	Capacitor Parameters			Conductor Parameters			
		C [mF]	ESR [mΩ]	ESL [nH]	Section [mm^2]	Length [m]	R_{DC} [mΩ]	L_{DC} [μH]
1	400	10.8	15.8	15	180 *	10	1.301	2.228
2	400	10.8	15.8	15	180 *	30	3.903	6.685
3	1200	30	6.6	11	500 **	4	0.188	0.942
4	1200	30	6.6	11	500 **	12	0.564	2.827

* Flexible bare multi-core copper conductor. ** Rigid bare single-core copper conductor.

Based on the parameters of each converter circuit, the equations obtained in the previous subsection are applied to calculate the decay factor, undamped resonance frequency, and roots of the characteristic polynomial. The calculations are performed for two different fault resistance values, namely $R_{fault} = 0.1$ mΩ and $R_{fault} = 10$ mΩ; the results are reported in Table 2.

Table 2. Values of decay factor, undamped resonance frequency, and roots of the characteristic polynomial obtained using the traditional DC fault approach for the considered DC grid.

Converter	R_{fault} = 0.1 mΩ				R_{fault} = 10 mΩ			
	α [rad/s]	ω_0 [rad/s]	s_1 [rad/s]	s_2 [rad/s]	α [rad/s]	ω_0 [rad/s]	s_1 [rad/s]	s_2 [rad/s]
1	3822.7	6439.7	−3823 +j5182	−3823 −j5182	6029.4	6439.7	−6029 +j2262	−6029 −j2262
2	1474.0	3726.3	−1474 +j3422	−1474 −j3422	2212.8	3726.3	−2213 +j2993	−2213 −j2993
3	3586.9	5703.5	−3589 +j4435	−3589 −j4435	8779.9	5703.5	−2105	−15,455
4	1271.1	3305.7	−1271 +j3052	−1271 −j3052	3015.6	3305.7	−3016 +j1354	−3016 −j1354

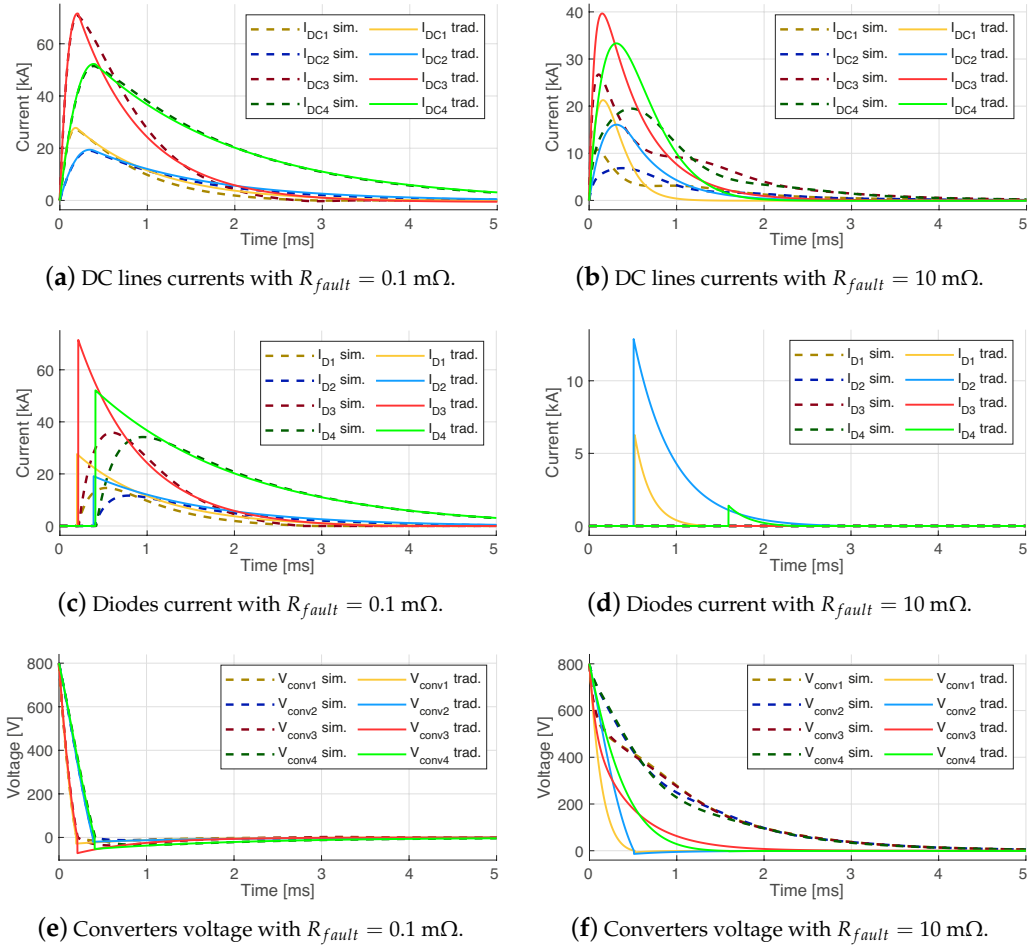
As discussed in the previous section, the value of ω_0 depends only on the converter capacitance and line inductance, while the value of α also includes the effect of resistive elements, including the fault resistance. Therefore, the fault response can be simply evaluated on the basis of parameters s_1 and s_2. In particular, when s_1 and s_2 appear in complex conjugate pairs, an oscillatory behavior is expected, as happens for all the converters in the case with $R_{fault} = 0.1$ mΩ. On the contrary, when s_1 and s_2 are real values, the fault response is expected to be over damped, which, in this analysis, occurs only in the case of converter 3 with $R_{fault} = 10$ mΩ.

Finally, initial conditions for all converters are considered as $i_{DC_i}(0) = 0$ and $v_{C_i}(0) = -V_{grid}$. Based on these values, the roots of the characteristic polynomial are calculated, and the equations detailed in the previous subsection for I_{DC_i}, I_{D_i}, and v_{conv_i} are evaluated.

Figure 4 shows the responses of each circuit according to the traditional DC fault analysis approach compared with the waveforms obtained from simulations of the whole system realized in MATLAB Simulink®, which is used as the reference framework.

Let us consider first the case of fault impedance close to zero ($R_{fault} = 0.1$ mΩ). In this case, the behavior of the fault current obtained by the traditional DC fault analysis method (Figure 4a) was quite close to that obtained from simulations, even though it exhibited slight discrepancies in the correspondence of the diode turn-on. This was evident mainly in the case of converters with higher power (1 and 2). The same behavior occurred for the voltage at the converter terminals (Figure 4e), thereby matching the responses only during the capacitor discharging stage and not during the diode freewheeling one. The biggest discrepancies were observed in the diode current (Figure 4c), as the shape of the current waveforms were different when the diode turned on, thereby showing a sharp peak instead of smoother behavior. Only after few milliseconds, when the current was decreasing in both responses, the two curves did match.

On the other hand, when the fault impedance was small but not negligible ($R_{fault} = 10$ mΩ), the behavior considerably differed between simulations and calculations from the traditional DC fault analysis. The fault current peaks (Figure 4b) calculated with the traditional method were significantly higher than those obtained from simulations, and their dynamics were very different too. Indeed, the curves obtained from the traditional method only presented one peak and were monotonously decreasing afterward, while the curves obtained from simulations showed additional oscillations after the main peak. Regarding the diode current (Figure 4d), the curves calculated using the traditional method, converters 1, 2, and 4, would have been expected to enter the diode freewheeling stage. Meanwhile, the simulations showed that there were not diodes turned on. This can be explained by analyzing the voltage behavior reported in Figure 4f. Freewheeling occurs for one converter when the voltage at that converter's terminals v_{conv_i} becomes negative and exceeds the diode voltage threshold. However, the voltage curves from simulations do not present an oscillating characteristic but rather an almost over damped one. The voltages on the terminals of all converters are similar, and they decay without passing through zero.



(**a**) DC lines currents with $R_{fault} = 0.1$ mΩ.

(**b**) DC lines currents with $R_{fault} = 10$ mΩ.

(**c**) Diodes current with $R_{fault} = 0.1$ mΩ.

(**d**) Diodes current with $R_{fault} = 10$ mΩ.

(**e**) Converters voltage with $R_{fault} = 0.1$ mΩ.

(**f**) Converters voltage with $R_{fault} = 10$ mΩ.

Figure 4. Comparison between traditional DC fault analysis and simulation results.

Considering Figure 4, it is possible to observe that, in the case where the fault impedance was small, the fault current peaks were similar to the simulations and occurred practically at the same time. However, when the joule integral was calculated to find the value of I^2t in the conductors from the converter to the grid, some significant discrepancies appeared. For the lower power converters (1 and 2), the I^2t values were higher when calculated through the traditional DC fault analysis method. Instead, for converters 3 and 4, the values of I^2t calculated by the traditional method were lower. This can be explained analyzing Figure 4a. Indeed, during the freewheeling stage, the curves of high power converters tended to be under the simulations curves, while the opposite occurred for converters 1 and 2.

Regarding the diode current, remarkable discrepancies were present in all the two cases here analyzed. Considering that, as can be seen in Figure 4c, for the traditional approach, the current peaks occur as soon as the diode is turned on, the curve shapes will be very different from the simulation ones. In particular, the most evident variation is shown in the maximum current derivative. Since, in the traditional approach, the change between stages is immediate, a virtually infinite current derivative is expected. As a consequence, these data were not taken into account. Additionally, if the evaluation is performed with discrete time steps, this current derivative value depends on the chosen time step, which makes it clearly an ill-posed indicator.

Considering the fault impedance of 10 mΩ, both the values of the fault current and of the diode current obtained from the traditional DC fault analysis differed significantly in comparison to simulations. Considering the fault current, all peak values obtained by the traditional method were significantly higher then the ones obtained by simulation, and

they occurred at very different times. For the I^2t values, a pattern was not found: as one decreased, one increased, and the others remained relatively the same, but the differences were significant. Considering now the diode current as previously mentioned, converters 1, 2, and 4 were expected to enter the diode freewheeling stage according to the traditional approach, and this behavior contradicted the simulations.

In order to quantify the difference between the current curves obtained through the traditional method and the simulations, the coefficient of determination or R^2 was evaluated with the same amount of sampling data points P for any curve. This value is calculated as shown below:

$$R^2 = 1 - \frac{\sum_{p=1}^{P}\left(I_{sim_p} - I_{trad_p}\right)^2}{\sum_{p=1}^{P}\left(I_{sim_p} - \overline{I_{sim}}\right)^2}. \tag{17}$$

On the basis of the data evaluated using (17) and presented in Table 3, it can be stated that, in this case, only a few currents are suitably described by the traditional method. Therefore, in the following, the limitations of this method will be addressed.

Table 3. Main indicators for fault current evaluation: comparison between traditional DC fault analysis and Simulink simulation.

Converter	$R_{fault} = 0.1\ \Omega$		$R_{fault} = 10\ \Omega$	
	R^2 Line Current	R^2 Diode Current	R^2 Line Current	R^2 Diode Current
1	0.980	0.468	−0.173	0.001
2	0.995	0.712	0.027	0.022
3	0.989	0.472	0.682	1
4	0.999	0.754	0.675	0.162

2.3. Limitations of the Traditional DC Fault Analysis Method

This section presents a summary of the main limitations of the traditional DC fault analysis method on the basis of the results of the case study presented in Section 2.2 and of the assumptions and simplifications discussed in Section 2.1. Three main issues emerge from the aforementioned analysis and results, namely (a) the dependency of the results' reliability on fault impedance values and/or other converter fault current contributions; (b) the inaccuracy of the diode current estimation; and (c) the inaccuracy of the conductor joule integral. Each of these issues is further discussed in the following subsections.

2.3.1. Dependency of the Results' Reliability on Fault Impedance Values and/or Other Converter Fault Current Contributions

Due to the simplifications adopted in traditional DC fault analysis, the most relevant limitation of this method is that the response of each particular converter is evaluated without taking into account the effect on the fault residual voltage due to the contribution of each converter, which is defined as follows:

$$v_{res}(t) = R_{fault} \cdot \left(i_{DC_i}(t) + \sum_{m \neq i}^{N} i_{DC_m}(t)\right). \tag{18}$$

Therefore, this assumption is not limiting only when the fault impedance is close to zero (as the fault residual voltage is zero too) or when the fault current contributions from other converters are negligible. However, as R_{fault} or other converter current contributions increase, the fault residual voltage increases too and affects the dynamics of the response of each converter. The dynamic of this voltage depends on all the converters connected to the network, including the converter under study. Therefore, this voltage cannot be obtained from the current contribution of each single converter, nor by the sum of the fault current contribution of all the converters obtained by the traditional DC fault analysis method.

With this approach, the effect is not accurately modeled, as the residual voltage due to other converters' fault current contribution is not taken into account in the calculation of the fault current contribution of a single converter. This results in significant errors, as the capacitors' discharge dynamics are obviously altered. This can be observed in Figure 4b, where the dynamics of the fault currents of converters 1, 2, and 3 presented an additional oscillation that did not follow its natural response (a curve with only one inflection point at the peak). As a consequence, the traditional DC fault analysis method can be used with no issues only in the following cases: (a) the DC system includes only one converter; and (b) the DC system includes several converters, but the fault impedance values belong to a certain range such that the residual voltage is small enough. Unfortunately, this range is strongly dependent on the specific DC network under analysis, thereby making any generalization of the presented results impossible.

2.3.2. Inaccuracy of the Diode Current Estimation

With respect to the calculation of the diode current, the traditional DC fault analysis approach is very limited due to the simplifications made to obtain the equations for the diode freewheeling stage. As previously commented, in the deduction of (11), it is assumed that the capacitor current is zero from the moment the diode turns on. While this assumption is a reasonable approximation for the evaluation of the overall fault current, it is not an accurate estimation of the diode current, as can be seen in Figure 4c. Since ESL inductance prevents an instantaneous change in the current of the capacitor branch, the dynamic of the diode current is slightly attenuated by the capacitor current. Thus, the hypothesis of $i_{D_i} = i_{DC_i}$ is correct only when the ESL is completely discharged. This inconsistency in the traditional approach implies that the values obtained by this method are not reliable for evaluating the capability of the diode to withstand the fault current.

2.3.3. Inaccuracy of the Conductor Joule Integral

This limitation is derived from the oversimplification introduced in the evaluation of the currents. When the I^2t value is calculated to check the thermal limitation of power components, the accumulated error causes a considerable discrepancy. As an example, let us consider the conductor connecting converter 1 with the DC grid bus when $R_{fault} = 0.1$ mΩ in the case under study. For this case, the joule integral maximum admissible value is 699.9×10^6 A^2s when it is used as a cable with a 180 mm^2 cross-section conductor and isolated by a cover of ethylene propylene rubber and reticular propylene (EPR-XLPE) [29]. According to the calculations obtained by the traditional analysis, the overcurrent protection should trip to avoid thermal damage, because the joule integral value would be 718.5×10^6 A^2s. Nevertheless, according to the data from simulations, the protection device is not required to trip, because the joule integral is actually around 22% less than the joule integral maximum admissible value for the cable, which is equal to 560.3×10^6 A^2s. Due to these inaccuracies, it is considered that the intrinsic uncertainty of the traditional DC fault analysis method could negatively influence the protections adjustment.

3. Innovative DC Fault Analysis

Considering the limitations that emerged from the case study as were analyzed by means of the traditional DC fault analysis approach, this section proposes an innovative approach for evaluating the DC network response under fault. In this regard, the traditional DC fault analysis approach discussed in Section 2 is used as a starting point, for which, however, a more general solution is proposed, thus overcoming the previously identified limitations. The proposed method used to obtain a general solution is a numerical method based on the so-called Euler method to solve the complete ODEs system. This approach has three main advantages: (a) it provides accurate results with no need to introduce any specific assumption; (b) it can be easily structured to manage an arbitrary number of converters; and (c) it reduces the computational processing times and resources necessary to simulate an entire DC network compared to other circuit solution software.

3.1. Euler Explicit Method in DC Fault Analysis

Considering a DC network with N converters, it is possible to highlight that a closed-form solution of such a system is very complex, as a general solution of each converter response depends on all the others. Moreover, during the capacitor discharging stage, the ODE system is of the order $2N$, while during the diode freewheeling stage (recognizing that the capacitor current should not be neglected), the ODE system is of the order $3N$, and lastly, during the fault steady state stage, the ODE system is again of the order $2N$. Therefore, an analytical solution to evaluate the fault current contribution of each converter, if possible, has at least the same number of independent linear terms as the ODE system, which makes it quite difficult to manage.

As discussed in the previous section, in the traditional approach, some assumptions are introduced to solve the ODE system in the closed-form, thus obtaining, for each converter, a simple solution. However, these assumptions also result in a very significant reduction in accuracy.

Discarding the pursuit of a closed-form solution of the ODE system, it is possible to introduce an innovative approach based on a numerical solution. To this aim, the Euler explicit approximation is a promising solution, thereby being simple to implement and highly accurate. The general expression for the Euler explicit approximation of a function $y(t) = f(t)$ is as follows:

$$\frac{d}{dt}y(t) \approx \frac{y(t+h) - y(t)}{h} \quad \xrightarrow{\triangle t = h} \quad \frac{d}{dt}y(t) \approx \frac{y[n+1] - y[n]}{h}, \tag{19}$$

where h is the time step between the discrete values of the function y. This approximation is discussed in detail in [30], along with another numerical methods. Rearranging the expression in (19), it is demonstrated that the function y can be reformulated into a series, where the next value in the series is calculated based on the present value and a function extracted from the derivative of y according to the following:

$$y[n+1] \approx y[n] + h \cdot \frac{d}{dt}y(t) = y[n] + h \cdot f(y, ..., t), \qquad 0 \leq n \leq \frac{t_{stop}}{h} \quad n \in \mathbb{N}. \tag{20}$$

By means of (20), the continuous time ODE system obtained from the traditional DC fault analysis can be transformed into discrete time plain equations, on which the innovative DC fault analysis method is based. The accuracy of the results obtained from this approximation will depend on the value of h, which needs to be small enough, according to sampling theory. Typically, for fast parameter variations in LVDC networks, a reasonable starting point for this application could be $h \leq 0.001$ ms.

In the following subsections, each stage of the fault response, as identified by the traditional DC fault analysis method, is analyzed to obtain the circuit equations through the Euler approximation for the innovative DC fault analysis method.

3.1.1. Capacitor Discharge Stage: Innovative Approach

The capacitor discharge stage was analyzed by means of the traditional DC fault analysis method in Section 2.1.1 by means of the circuit reported in Figure 1, thereby leading to Equations (1) and (2). For the reformulation in discrete time, Equations (1) and (2) are reorganized by isolating the derivative, thus resulting in the following:

$$\frac{d}{dt}v_{C_i}(t) = \frac{i_{DC_i}(t) - i_{conv_i}}{C_i}, \tag{21}$$

$$\frac{d}{dt}i_{DC_i}(t) = -\frac{1}{L_{DC_i} + ESL_i} \cdot \left(R_{DC_i} + ESR_i \cdot i_{DC_i}(t) + v_{C_i}(t) + R_{fault} \cdot \sum_{m \neq i}^{N} i_{DC_m}(t) \right). \tag{22}$$

Note that, using the Euler approximation, it is possible to also consider the current contribution of all the converters, thus removing one of the simplifications introduced in

the traditional DC fault analysis method. As a consequence, the expression of the fault current contribution of the ith converter (22) depends on the sum of the fault current contributions from all the other converters. Substituting the continuous time variables in expressions (1), (2) to discrete time ($x(t) \rightarrow x[n]$) and applying the general form of the Euler approximation (20), the following equations are obtained for the capacitor voltage and the line current, respectively:

$$v_{C_i}[n+1] = v_{C_i}[n] + \frac{h}{C_i} \cdot \left(i_{DC_i}[n] - i_{conv_i}\right), \tag{23}$$

$$i_{DC_i}[n+1] = i_{DC_i}[n] - \frac{h}{L_{DC_i} + ESL_i} \cdot \left((R_{DC_i} + ESR_i) \cdot i_{DC_i}[n] + v_{C_i}[n] + R_{fault} \cdot \sum_{m=1}^{N} i_{DC_m}[n] \right). \tag{24}$$

With the aim of facilitating the manipulation of Equations (23) and (24), the resistances and inductances were expressed individually without association as a sum between them, which is in contrast to the traditional DC fault analysis method discussed in Section 2.1.1.

This made it possible, by determining the values for the instant $n+1$, to obtain the rest of the circuit variables as functions of fault current and converter capacitor voltage by using basic circuit theory. The only missing parameters to initiate the process were the initial conditions ($v_{C_i}[0]$ and $i_{DC_i}[0]$). To obtain comparable results, the same initial values used for the traditional DC fault analysis were used, namely $v_{C_i}[0] = -V_{grid}$ and $i_{DC_i}[0] = i_{conv_i}$, even if the option of using different values as initial values was open.

On the other hand, as the calculations progress, it is crucial to assess the value of the voltage at each converter terminal v_{conv_i} (considering that the coupling between converters produces increased accuracy but requires the need to solve a more complex system) to determine when the capacitor discharge stage is finished. As in the traditional DC fault analysis, it is possible to neglect the voltage drop across the ESL, so the following expression can be used:

$$v_{conv_i}[n] \approx -v_{C_i}[n] - ESR_i \cdot i_{DC_i}[n]. \tag{25}$$

As discussed in the traditional DC fault analysis, when (and if) the value of the converter voltage exceeds the diode threshold, namely $v_{conv_i}[n] < -V_d$, the equations used to evaluate the ith converter response must be changed to those corresponding to its diode freewheeling stage, which is described in the next section.

3.1.2. Diode Freewheeling Stage: Innovative Approach

For the analysis of the diode freewheeling stage, the ODE system deduced in Section 2.1.2 from the circuit reported in Figure 2 was used. Thus, by isolating the time derivatives in (1) and (10), the following expressions are obtained:

$$\frac{d}{dt} v_{C_i}(t) = \frac{i_{C_i}(t) - i_{conv_i}}{C_i}, \tag{26}$$

$$\frac{d}{dt} i_{DC_i}(t) = -\frac{1}{L_{DC_i}} \cdot \left(V_d + r_d \cdot i_{D_i}(t) + (R_{DC_i} + R_{fault}) \cdot i_{DC_i}(t) + R_{fault} \cdot \sum_{m \neq i}^{N} i_{DC_m}(t) \right). \tag{27}$$

In this approach, it is possible to remove the hypothesis that the capacitor current is null during this whole stage, so now $i_{DC_i} = i_{D_i} + i_{C_i} + i_{conv_i}$. The relation between the diode and capacitor current, obtained by KVL on the mesh and including the diode and the capacitor only, results in the following:

$$\frac{d}{dt} i_{C_i}(t) = \frac{1}{ESL_i} \cdot \left(V_d + r_d \cdot i_{D_i}(t) - v_{C_i}(t) - ESR_i \cdot i_{C_i}(t) \right). \tag{28}$$

By substituting the continuous time variables in expressions (26)–(28) to discrete time ($x(t) \rightarrow x[n]$) and applying the general form of the Euler approximation (20), it is possible

to evaluate the converter capacitor voltage, the fault current contribution, and the capacitor current, thereby respectively resulting in the following:

$$v_{C_i}[n+1] = v_{C_i}[n] + \frac{h}{C_i} \cdot \left(i_{DC_i}[n] - i_{conv_i}\right), \tag{29}$$

$$i_{DC_i}[n+1] = i_{DC_i}[n] - \frac{h}{L_{DC_i}} \cdot \left(R_{DC_i} \cdot i_{DC_i}[n] + r_d \cdot i_{D_i}[n] + V_d + R_{fault} \cdot \sum_{m=1}^{N} i_{DC_m}[n]\right), \tag{30}$$

$$i_{C_i}[n+1] = i_{C_i}[n] - \frac{h}{ESL_i} \cdot \left(ESR_i \cdot i_{C_i}[n] + v_{C_i}[n] - r_d \cdot i_{D_i}[n] - V_d\right). \tag{31}$$

In addition to the equations deduced from the ODEs, the diode current for the instant $n+1$ is required, which can be easily deduced by KCL from the fault and capacitor currents as follows:

$$i_{D_i}[n+1] = i_{DC_i}[n+1] - i_{C_i}[n+1] - i_{conv_i}. \tag{32}$$

The voltage at the converter terminals can be evaluated as follows:

$$v_{conv_i}[n] = V_d + r_d \cdot i_{D_i}[n] \approx -v_{C_i}[n] - ESR_i \cdot i_{C_i}[n]. \tag{33}$$

These equations are valid for all converters of the diode turned on until the instant in which $v_{conv_i}[n] > -V_d$, which is when the next fault stage begins.

3.1.3. Fault Steady State Stage: Innovative Approach

At the instant when the diode turns off and the free-wheeling stage ends, the equivalent circuit returns to the same as in the capacitor discharge stage. Since it is the same circuit, the expressions in (23)–(25) are also valid for this stage, as long as suitable initial conditions are selected. These are easily identified as the last values computed during the diode freewheeling stage.

3.2. Overview of the Proposed Method

Once the equations for each stage have been deduced, as discussed in Section 3.1, the only difficulty left in the proposed method lies in addressing the change in stages and choosing the correct equations for evaluating the response of each converter, thus considering that not all converters necessarily experience stage changes at the same instant or at all. For this reason, it is recommended to use the method through an algorithm that, as a first step, evaluates the value of v_{conv_i} for each converter, and, depending on this value, selects the correct equations to use. For clarity, an overview of the proposed methodology is reported in the flowchart in Figure 5.

To compare the results to continuous time functions, it should be recalled that each iteration of n corresponds in time to $t = n/h$ in an interval of $0 \leq n \leq t_{stop}/h$ when considering $n \in \mathbb{N}$. In addition, note that, in the diagram reported in Figure 5, it is proposed that in each step of the calculation, the variables are evaluated beginning with converter 1, then for converter 2, etc., until reaching converter N (they can be evaluated without a particular order, as the order does not matter). Therefore, it is not possible to continue with the evaluation of the values for the ith converter at time $n+1$ without first having evaluated the values of all the converters at time n.

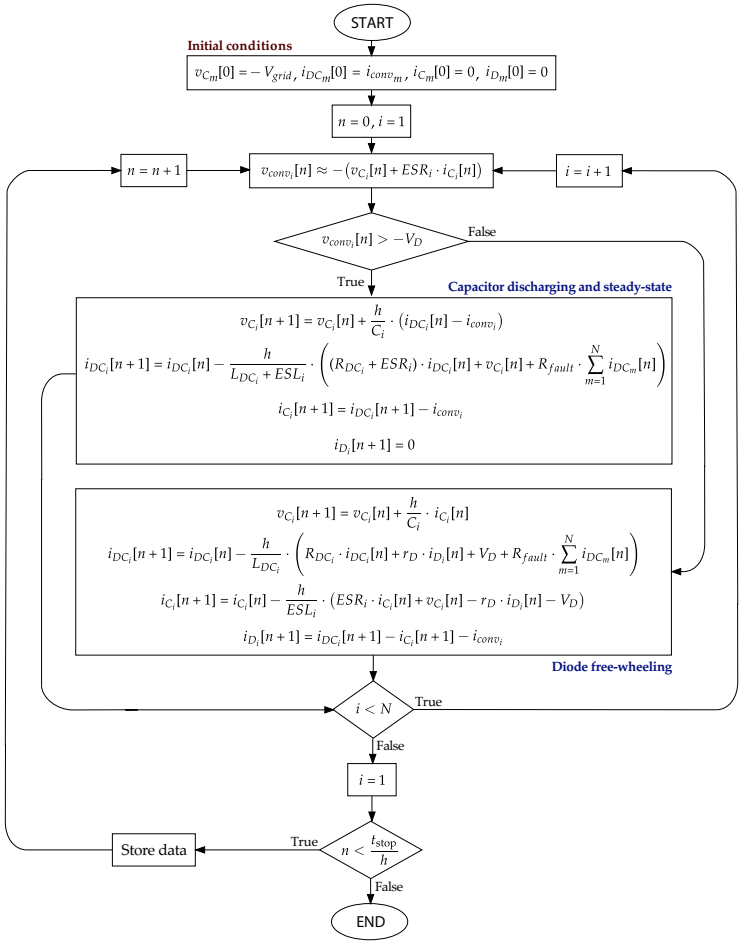


Figure 5. Complete methodology for the evaluation of the DC network fault response using the Euler approximation.

3.3. Matrix Formulation

Although the methodology outlined can be implemented in any numerical computing environment, handling the data can become problematic as the number of converters included in the DC network increases. Given that electrical networks, in general, grow over time as their lifespan advances, modifying the programming code to incorporate new converters to the network can become challenging. As a consequence, a more convenient and efficient way to input the parameters of each converter would be very useful. Furthermore, dealing with two different sets of equations is impractical for execution, while it would be simpler to evaluate one equation for each variable, with no need to distinguish among capacitor discharge, diode freewheeling, and fault steady state stages.

Taking these considerations into account and leveraging that we are dealing with linear equations only, the variables, parameters, and equations can be fruitfully organized into matrices. In this regard, the variables are firstly arranged in column vectors of size N to obtain the following:

1. The voltage across each converter capacitor $\mathbb{V}_C[n] = \left(v_{C_1}[n], ..., v_{C_N}[n]\right)'$;
2. The voltage at each converter terminal $\mathbb{V}_{conv}[n] = \left(v_{conv_1}[n], ..., v_{conv_N}[n]\right)'$;
3. The fault current contribution of each converter $\mathbb{I}_{DC}[n] = \left(i_{DC_1}[n], ..., i_{DC_N}[n]\right)'$;
4. The current in each converter capacitor $\mathbb{I}_C[n] = \left(i_{C_1}[n], ..., i_{C_N}[n]\right)'$;
5. The current in each converter diode $\mathbb{I}_D[n] = \left(i_{D_1}[n], ..., i_{D_N}[n]\right)'$;
6. The current from each converter $\mathbb{I}_{conv} = \left(i_{conv_1}, ..., i_{conv_N}\right)'$.

These vectors can be easily pre-loaded, updated, and organized in a data repository.

Successively, the parameters of each converter can be organized in diagonal matrices of size $N \times N$, thus resulting in the following:

1. The DC line resistances $\mathbb{R}_{DC} = \text{diag}\left(R_{DC_1}, ..., R_{DC_N}\right)$;
2. The converter capacitor equivalent series resistances $\mathbb{ESR} = \text{diag}(ESR_1, ..., ESR_N)$;
3. The DC line inductances $\mathbb{L}_{DC} = \text{diag}\left(L_{DC_1}, ..., L_{DC_N}\right)$;
4. The converter capacitor equivalent series inductances $\mathbb{ESL} = \text{diag}(ESL_1, ..., ESL_N)$;
5. The converter capacitor values $\mathbb{C} = \text{diag}(C_1, ..., C_N)$.

With the aim of unifying the equations for the DC fault analysis and of avoiding the distinction among capacitor discharge, diode freewheeling, and fault steady state stages, the introduction of matrices $\mathbb{D}_{\text{ON}}$ and $\mathbb{D}_{\text{OFF}}$ is proposed for the diode conduction states ON and OFF, respectively. The latter are defined, once again, as diagonal matrices of size $N \times N$, which contain information about the diode states of each converter, namely:

1. The matrix of diodes in the conduction mode $\mathbb{D}_{\text{ON}}[n] = \text{diag}(D_{\text{state}_1}[n], ..., D_{\text{state}_N}[n])$;
2. The matrix of diodes out of the conduction mode $\mathbb{D}_{\text{OFF}}[n] = \text{diag}\left(\overline{D_{\text{state}_1}[n]}, ..., \overline{D_{\text{state}_N}[n]}\right)$.

Here, D_{state_i} is 0 when the ith diode is turned off and 1 when the ith diode is turned on.

Finally, an overview of the equations of the innovative DC fault analysis method in the matrix form are included in the flowchart in Figure 6. When considering the algorithm in the matrix form, the only challenge is to update the diode state matrices at each step. As long as this is done correctly, the algorithm will be applied correctly and accurately evaluate the overall fault response of the DC network.

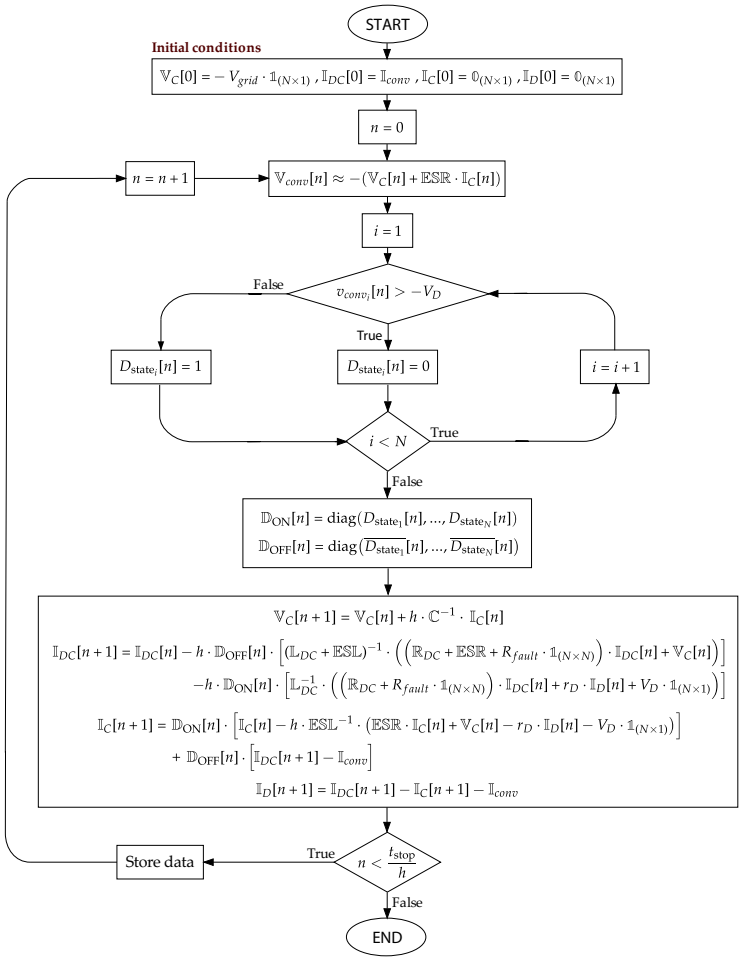
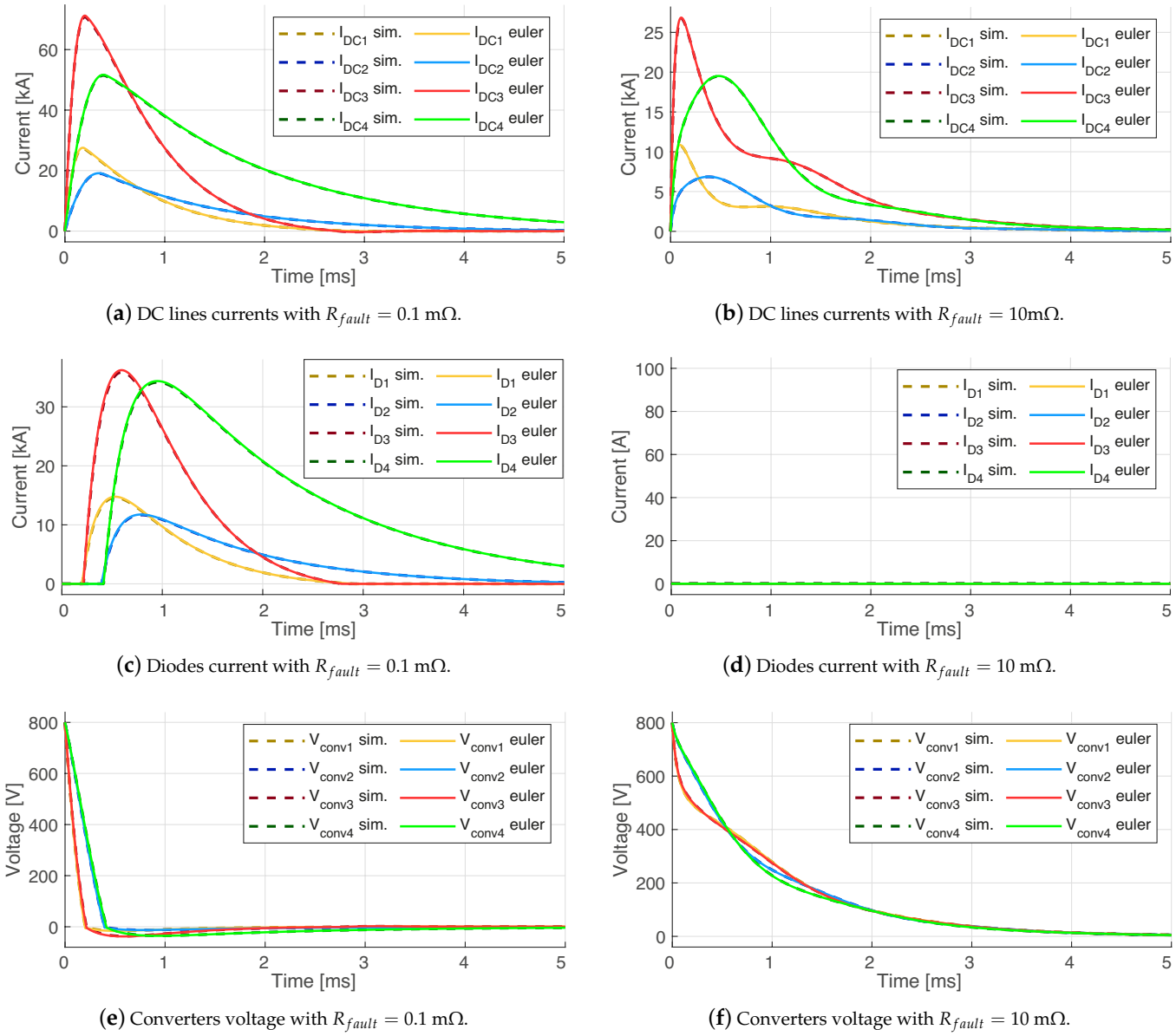


Figure 6. Complete methodology for the evaluation of the DC network fault response using the matrix formulation of the Euler approximation.

3.4. Case Study: Comparison between the Proposed Innovative DC Fault Analysis Method and Numerical Simulations

To prove the effectiveness of the proposed innovative DC fault analysis with respect to the traditional DC fault analysis method, the same DC grid example presented in Section 2 will be considered in this section. The relevant data regarding the DC network are presented in Table 1. By considering these parameters and setting the same initial conditions, we obtained $\mathbb{V}_C[0] = -V_{grid} \cdot \mathbb{1}_{(N\times 1)}$ and $\mathbb{I}_{DC}[0] = \mathbb{0}_{(N\times 1)}$; the proposed innovative DC fault analysis method was implemented with a time step equal to $h = 1$ µs.

The results obtained through the proposed method, compared with MATLAB Simulink simulation results, are shown in Figure 7. Similarly to the case study reported in Section 2.2, two different cases with different fault impedances were evaluated, with $R_{fault} = 0.1$ mΩ and $R_{fault} = 10$ mΩ, as in the previous case.



(**a**) DC lines currents with $R_{fault} = 0.1$ mΩ.

(**b**) DC lines currents with $R_{fault} = 10$mΩ.

(**c**) Diodes current with $R_{fault} = 0.1$ mΩ.

(**d**) Diodes current with $R_{fault} = 10$ mΩ.

(**e**) Converters voltage with $R_{fault} = 0.1$ mΩ.

(**f**) Converters voltage with $R_{fault} = 10$ mΩ.

Figure 7. Comparison between proposed method using the general approach and simulation results.

The curves obtained with the proposed innovative DC fault analysis method and those obtained from simulations produced superimposed curves, thereby highlighting the accuracy of this new approach. In comparison with the traditional DC fault analysis

method, it is evident that the proposed method sorted out the limitations concluded in the previous section, and it is capable of providing accurate results for DC systems with multiple converters and non-negligible fault impedance. In particular, for both of the considered cases, the fault currents shown in Figure 7a,b exhibit the same dynamics foreseen by the simulation. As expected, in the case with small fault impedance, corresponding to Figure 7a, the curves display the intrinsic natural behavior from each converter, with one single peak and no oscillations. Conversely, considering Figure 7b corresponding to the case with large fault impedance, the curves do present additional oscillations, which is an effect of the residual voltage in the fault section that is impossible to be correctly evaluated by means of the traditional DC fault analysis method, as detailed extensively in Section 2.3.1.

Therefore, it can be asserted that, regardless of the fault impedance, the proposed method is capable of satisfactorily evaluating the fault current of a converter when considering both its inherent dynamics and the dynamics of the DC network.

Regarding the assessment of the diode current, for the case with $R_{fault} = 0.1$ mΩ it is observed that the curves in Figure 7c accurately represent the diode behaviour. These curves grew rapidly but not immediately, then reached their peak value, and then decreased slowly until reaching zero at $t = t_{\text{off}}$. Meanwhile, for the case with $R_{fault} = 10$ mΩ reported in Figure 7d, the proposed method correctly evaluated that the converters did not enter into the freewheeling stage because the voltage did not decay beyond zero.

Finally, the main indicators for fault current evaluation for cases with $R_{fault} = 0.1$ mΩ and $R_{fault} = 10$ mΩ are presented in Table 4. Similarly to Section 2.2, in order to quantify the difference between the current curves obtained through the traditional method and the simulations, it was proposed to evaluate coefficient of determination or R^2, as defined in (17).

Table 4. Main indicators for fault current evaluation: comparison between the proposed general fault analysis and Simulink simulation.

Converter	$R_{fault} = 0.1$ mΩ		$R_{fault} = 10$ mΩ	
	R^2 Line Current	R^2 Diode Current	R^2 Line Current	R^2 Diode Current
1	0.998	0.997	0.987	1
2	0.998	0.989	0.994	1
3	0.989	0.996	0.988	1
4	0.999	0.997	0.991	1

It is possible to observe that, for all cases, the correlation coefficients are all very high, with a maximum error around 1%. According to Table 4, it can be observed that the diode currents in the case with $R_{fault} = 10$ mΩ all have a correlation coefficient equal to one, but this should not be considered suspicious, as the freewheeling stage in this case was absent in all the converters, and, consequently, all diode currents were identically null during the whole transient. This highlights that the proposed approach can correctly identify the freewheeling stages in the presence of non-negligible fault resistances, which was not the case for the traditional DC fault analysis method. The high level of accuracy granted by the proposed approach allows us to correctly evaluate all the most significant parameters commonly used for system protection design, such as fault current peak values and times, maximum current derivatives, and joule integrals. This approach exhibits two main advantages over traditional methods: (a) it can easily be structured to manage an arbitrary number of converters; and (b) it provides accurate results, with no need to introduce any specific assumption, thus producing results suitable for protection purposes.

4. Conclusions and Future Work

The traditional DC fault analysis method is a useful tool for straightforwardly understanding the behavior of the fault current contributions of DC converters when a fault occurs in an LVDC network. However, when a system with multiple converters and non-

negligible fault impedance is considered, its results are strongly limited in terms of accuracy due to the necessary assumptions included in the problem's solution. In particular, it is assumed that the response of each converter can be calculated without taking into account the effect of the fault current contribution of other converters in the DC network. This is fine to establish a worst case scenario, but for protection design purposes, it is reasonable only when the fault impedance is close to zero, or the fault current contribution from all other converter is null. Indeed, as R_{fault} increases, the fault residual voltage increases and this could introduce a coupling effect among the dynamic response of each converter. In addition, in the traditional DC fault analysis, it is assumed that the diode freewheeling stage is established instantaneously and that in that stage the current flowing through the capacitor is always zero. However, this assumption leads to unrealistic results, as happens for the fast rise of the diode current. As a consequence of these assumptions, three main limitations of the traditional DC fault analysis emerge for LVDC systems including multiple converters, namely (a) the reliability of the results depends on the fault impedance value and on the fault current contribution from all other converters; (b) the diode current estimation is not very accurate; and (c) the joule integral calculation for conductors is inaccurate.

In order to overcome these issues, an innovative method for DC fault analysis based on a numerical method has been presented in this paper. The proposed innovative DC fault analysis method arises from the primary interest in solving the circuit to extract the indicators (current peak value and time, joule integral, etc.) necessary for correctly designing system protections. For this purpose, it is not necessary to find a closed-form solution of the ODEs system from a circuit with several converters connected, but a time series representing the circuit variables as a function of the discrete elapsed time is enough.

This approach proved to grant several advantages over traditional methods: (a) it provides accurate results, with no need to introduce any specific assumption and regardless of the fault impedance value; (b) it can be easily structured to manage an arbitrary number of converters; (c) only minimal additional efforts are required from the user when the network configuration changes; (d) it reduces the computational processing times and resources necessary to simulate an entire DC network; and (e) it can be the starting point to develop an open-source software to perform accurate DC fault analysis. These last three advantages can also be considered in comparison to DC fault analysis through a solution software. This, being designed for multiple purposes, requires additional effort on the part of the user for the circuit layout and greater use of resources by the computational environment.

In addition, on the basis of this innovative numerical approach to DC fault analysis, future work can be addressed towards an equivalent circuit representation for the residual voltage in order to simplify the calculations in the presence of changes in the network configuration. In particular, it can be of interest to consider whether a reduced order equivalent circuit for a DC network could be found. This would simplify the calculation of the fault current for a new converter introduced into the network, since it would no longer be necessary to calculate the response of all of the N converters at the same time but only that of the converter under study and of the equivalent RLC circuit representing the complete network.

Author Contributions: Conceptualization, J.V.G. and S.N.; methodology, J.V.G.; software, J.V.G.; validation, S.N. and F.O.; formal analysis, J.V.G., S.N., and F.O.; investigation, J.V.G., S.N., F.O., A.A., and R.F.; resources, R.F.; data curation, S.N., A.A., and R.F.; writing—original draft preparation, J.V.G.; writing—review and editing, J.V.G. and S.N.; visualization, J.V.G.; supervision, A.A. and R.F.; project administration, R.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: This research did not require ethical approval.

Informed Consent Statement: This research did not involve humans.

Data Availability Statement: The data are available upon request from the authors.

Conflicts of Interest: Author Antonello Antoniazzi is employed by ABB SpA. The remaining authors declare no conflicts of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript; or in the decision to publish the results.

Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
DC	Direct Current
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
HVDC	High-Voltage Direct Current
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LVDC	Low-Voltage Direct Current
RL	Resistance Inductance
RLC	Resistance Inductance Capacitor
ODE	Ordinary Differential Equation
VSC	Voltage Source Converter

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