40-nm SPAD-Array Detection System for Ultra-Fast Raman Spectroscopy

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Abstract: Raman Spectroscopy for protein sequencing requires fast detection systems able to manage fluorescence rejection. We propose a 40-nm SPAD-Array system-on-chip with an integrated gate generation block to time-filter fluorescence photons. Preliminary characterization shows excellent performances.

1. Introduction

Raman Spectroscopy (RS) has been widely applied in medical diagnostics and one particularly promising field is proteomics, where it can unlock its full potential by discriminating 20 different amino acids enabling single-protein analysis [1].

In this framework, the ProteinID (ProID) European project focuses on the development of a novel instrumentation to perform ultra-fast RS with the specific aim of protein sequencing. The Raman response of single amino acids is obtained with optical excitation of molecules as they pass through special plasmonic nanopores, engineered to precisely control the translocation of denatured proteins [2]. The resulting secondary radiation is diffracted to spatially separate the different wavelengths, which can then be detected by an application-specific system. For this purpose, our research team developed a fast detection system based on an array of Single-Photon Avalanche Diodes (SPADs) to effectively gather information from the spatially distributed Raman photons.

One of the main requirements for such a detector is efficient rejection of fluorescence photons, which have the same wavelength of the useful signal and cannot be discarded by the simple use of an optical filter. Therefore, the different timing of the two types of radiation is exploited to discriminate between them: SPAD detectors are enabled just in user-selectable, sub-ns windows where Raman photons are expected, whereas fluorescence photons impinge on the detector when SPADs are biased below breakdown and no detection can take place [3]. Speed is another pivotal aspect of this system as the Raman spectrum acquisition should last less than 1 µs, which is the average time spent by the single amino acid in the nanopore [1], otherwise the sequenced protein would present some gaps. For this reason, the proposed detector offers an innovative jump readout solution that reduces the overall measurement time by reading a subset of the pixel outputs, selected by the user, to capture just the most significant spectral lines.

2. SPAD array architecture

The developed detection system was designed in a 40 nm planar technology by STMicroelectronics to meet the high-speed readout performances of the ProID project. It contains an array of 128 × 4 SPAD detectors, provided with individual Variable-Load Quenching Circuit (VLQC) frontends [4], 6-bit counters, column adders, a gate generation block and readout circuitry. A signal coming from the exciting laser is used to synchronize the activity of the detector with the expected occurrence of the Raman response. For this purpose, two gating signals (hard gate and soft gate) are generated to handle the time-filtering needed for fluorescence rejection. A first filtering (hard) is crucial at front-end level to actively switch off the SPADs outside the window of interest and lower the probability of afterpulsing events. A second filtering (soft) is performed at readout level to reach the desired sub-ns resolution, which cannot be achieved with hard-gating alone, due to the finite times needed to quench and reset the SPADs. The gate signals are generated on-chip with a block that comprises a Delay-Locked Loop (DLL) combined with a twin Voltage-Controlled Delay Line (VCDL) to produce 50 equally spaced pulses, insensitive to Process, Voltage and Temperature (PVT) variations. A register allows the user to externally configure the width and the position of the generated windows with a 200 ps resolution. At the output of each pixel a 6-bit counter is present to accumulate the occurred events. These data can be read either through a classical shift-register and a column adder or taking advantage of the jump readout solution, which adopts tri-state buffers to deliver the data on a common bus.

As a preliminary test of this complete structure, a smaller 16 × 4 chip was produced in the same technology, with some simplifying adjustments such as the absence of an on-chip gate generator block and of the jump readout solution. This chip allowed the testing of the SPADs fabricated in the 40 nm planar technology by

STMicroelectronics, together with the devised frontend circuit and shift-register readout performances that are presented in the following paragraph.

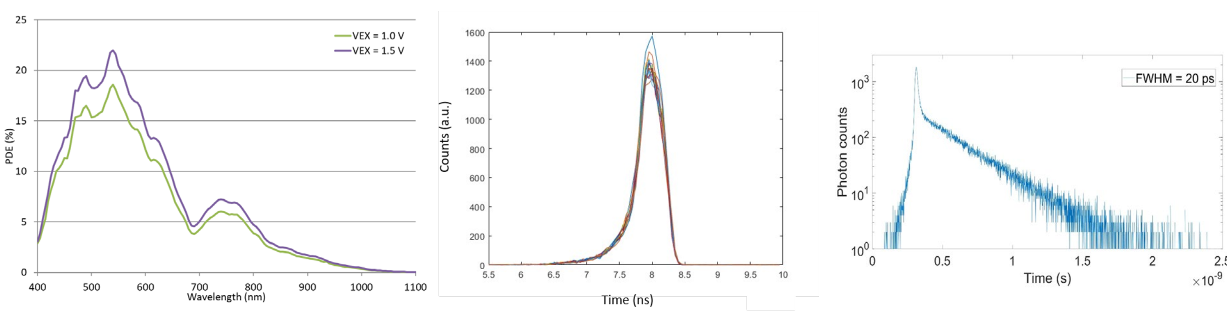
3. SPAD characterization and gating performances

One of the main figures of merit for SPADs is Dark Count Rate (DCR), which assesses the number of avalanches occurred in the detector in absence of illumination [3]. The DCR characterization of the array was carried out at 32.5°C, with the SPADs biased with both a 1 V and a 1.5 V excess voltage (15.5 V and 16 V overall SPAD reverse voltage). The array displays a median DCR of 200 cps for 1 V excess bias and of 430 cps for 1.5 V excess bias. Setting a threshold at twice the median DCR, 17.2% of the pixels are hot pixels, while this value reduces to 7.8%, when the threshold is set at 100 times the median DCR.

The Photon Detection Efficiency (PDE) of the SPAD array, that accounts for both Photon Detection Probability (PDP) and geometrical fill-factor (FF), was measured including microlenses and for multiple wavelengths. The resulting PDE spectrum is shown in Fig. 1a. It exhibited a peak at 540 nm with a value of 18.6% for V_{EX} = 1 V and of 22% for V_{EX} = 1.5 V, which is among the best values available for Raman spectroscopy [5].

Afterpulsing is another critical issue for SPAD detectors: during an avalanche current, some charge gets trapped inside the junction and released after some time, triggering another detection event that is not related to an impinging photon [5]. The afterpulsing probability of the SPAD detector was characterized on the test chip resulting in a value below 0.1%.

Being the gating signals of the test array generated outside the chip, the hard-gating duration was set by the testing board between 3 and 4.5 ns. The hard-gating window of the SPAD sensor was characterized by scanning it around a laser pulse and recording the photon counts at each step, obtaining fast rising- and falling-edge transitions of 200 ps with no variation for different excess voltages. The soft-gating duration could reach a minimum Full-Width at Half-Maximum (FWHM) of 300 ps, being only limited by the digital logic speed and thus reaching the sub-ns resolution required by ProID project. The counts recorded within the soft-gating window for all the 16 columns of the array are displayed in Fig. 1b. The SPAD timing jitter was also measured with a Time-Correlated Single-Photon Counting (TCSPC) setup. For this measurement, the SPADs were biased at 1 V excess voltage and illuminated with an 850-nm laser. The detector exhibited a jitter of 23 ps FWHM, as shown in Fig. 1c.



a) b) c)

Fig. 1. a) Photon Detection Efficiency b) Minimum soft-gating window c) SPAD timing jitter

In conclusion, our preliminary tests showed that the chosen scaled technology allows to reach an optimal combination of PDE and DCR of the SPAD sensors [5], together with a fast response of the front-end circuit that thoroughly matches RS requirements. The presence of the on-chip gate generation block in the final chip will result in gating signals with lower skew, sharper edges and better resolution, further improving fluorescence rejection [3].

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4. References

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