Electronic-photonic co-design for all-optical signal processing and computing

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***Abstract*—Analog signal processing and computing performed in the optical domain with programmable photonic chips require a dedicated electronic control layer to set and dynamically reconfigure the circuit functionality at runtime. Here, we present recent advances in electronic-photonic co-design, enabling successful operation of large-scale photonic processors.**

***Keywords*—Electronic-photonic co-design, optical computing, integrated electronics.**

I. INTRODUCTION

Photonic integrated circuits (PICs) are becoming increasingly popular in the field of analog computing, thanks to their inherent wide bandwidth and low power consumption that promise to overcome the performance wall reached by traditional digital electronics [1]. Programmable PICs, whose functionality can be defined by the user, also add flexibility to these advantages. Since their configuration needs to be dynamically adjusted at run-time, these circuits require a tailored electronic control layer. Here, we present recent advances in electronic-photonic co-design for all-optical computing and signal processing, showing different approaches that can be employed to efficiently address and control large-scale PICs.

II. MAGNITUDE-AND-PHASE CONTROL OF MZIS FOR SCALABLE OPTICAL COMPUTING

Photonic circuits based on Mach-Zehnder interferometers (MZIs) are gaining popularity in optical computing applications for their design simplicity and ability to work with complex numbers. However, current demonstrations are limited by the difficulty of properly setting the state of each MZI to configure the desired input-output transfer matrix. To this end, for each 2x2 elementary optical gate (Fig. 1a) two phase shifts ϕ and θ need to be programmed accurately. We propose to monitor, with minimally-invasive photodetectors, the optical power at both the internal and output branches of each interferometer to perform this operation without ambiguity [2]. To test this electronic control strategy, we designed a silicon PIC comprising an input vector input generator, a 2x2 optical gate for matrix-vector multiplication and an output phase detector for validation of the result (Fig. 1a). The strategy has been first employed to generate the input vector, by acting on heater ψ to control the power percentage $A_{1\%} = A_1/(A_1 + A_2)$. The measurement shown in Fig. 1b confirms the ability of the control to set any target optical power, with a measured resolution of 11 bits. We then configured the optical gate matrix by choosing $\phi = 1.8\pi$ and $\theta = 0.15\pi$, automatically set by two feedback loops, and used the input generator to perform 9 vector-matrix multiplications (Fig. 2c). All results are very accurate, showing a root mean square error in the measured power below 1% and in the measured χ_C phase of only $29\,\mathrm{mrad}$, corresponding to an equivalent resolution of 8 bits. Thanks to the local and independent feedback loops, this approach can be seamlessly extended to larger MZI processors.

III. INTEGRATED ELECTRONICS FOR ADVANCED PICS

A. ASIC controller for dynamic PIC self-configuration

When space, power, weight and multichannel operation are of concern, electronic application-specific integrated circuits (ASIC) can be an effective solution to address large-scale optical processors. As an example, Fig. 2a shows an adaptive photonic receiver, that can be used to recover a free-space beam propagating through a turbulent link. The circuit automatically computes and inverts, in the optical domain, the transfer matrix of the transmission channel [3]. Therefore, it

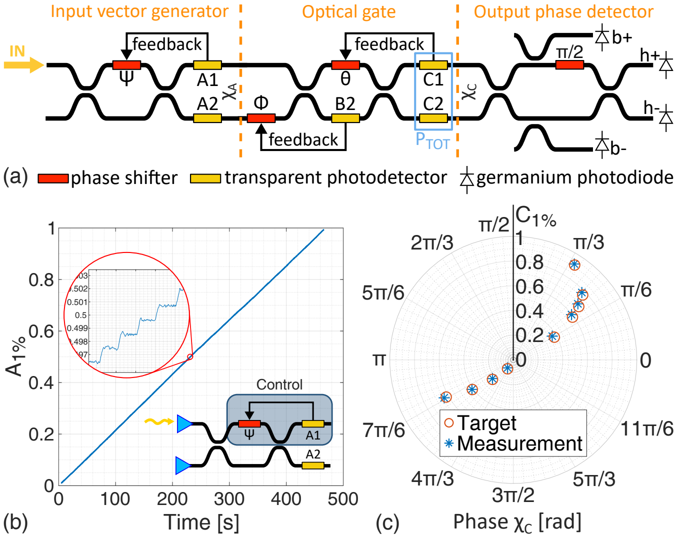

Fig. 1. a) Schematic of a 2x2 vector-matrix multiplication circuit based on MZIs, where each element is feedback-controlled electronically. b) Experimental 11-bit amplitude control of the generated input vector and c) successful vector-matrix multiplications performed by the circuit with 8-bit accuracy.

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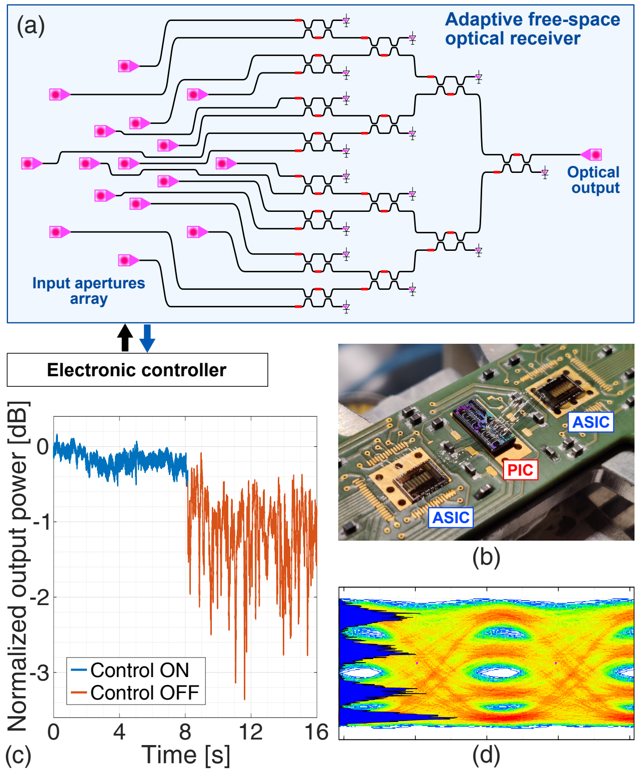

Fig. 2. a) Schematic and b) photograph of an adaptive free-space optical receiver, controlled by a pair of electronic ASICs. c) Successful reconstruction, performed optically by the PIC, of a free-space beam propagating through a turbulent channel, enabling d) high-speed PAM4 50 Gbit/s transmission.

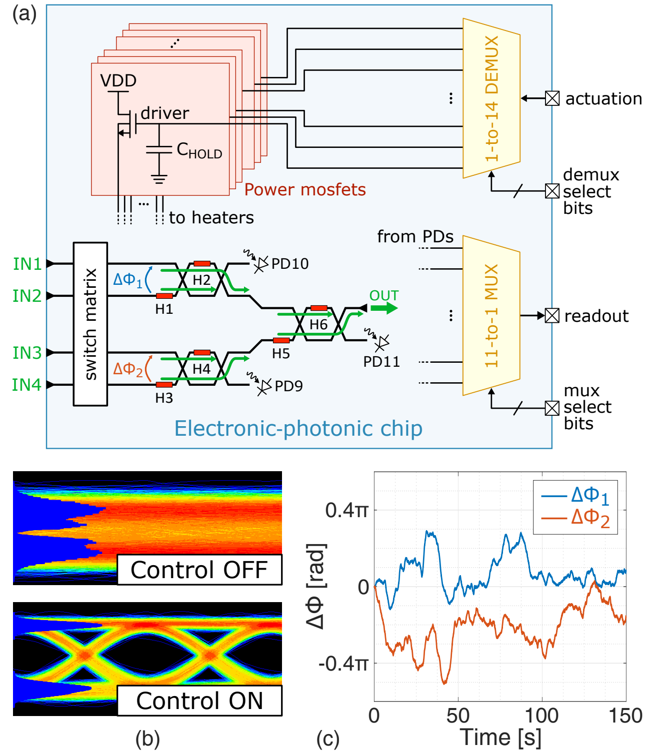

Fig. 3. a) Schematic view of a monolithic silicon chip integrating a 4-channel photonic coherent adder and the electronic circuits enabling sequential control of the optical functionality. b) Communication and c) sensing experiment, where the input phase difference is assessed while transmitting a 25 Gbit/s signal.

can be used to counteract the time-varying distortions caused by propagation through atmospheric turbulence. We designed a dedicated 8-channel control ASIC (Fig. 2b), able to address 16 heaters and 8 sensors and perform the required dynamic power minimization algorithm [4]. We used a pair of ASICs to control the PIC and recover a free-space PAM4 50 Gbit/s signal propagating through a turbulent channel. Fig 2c shows the optical power at the chip output when the electronic control is on/off. The measurement confirms that the ASIC dynamic action allows successful recovery of the impinging optical signal, by compensating the random phase fluctuations of the beam front. This results in an open eye diagram at the chip output (Fig. 2d), without the need for high-speed power-hungry digital equalization and signal processing.

B. Monolithic electronic-photonic co-integration

As a second possible solution to address large-scale PICs, we propose the monolithic co-integration of electronic circuits on photonic chips, which can be achieved even on commercial silicon photonics platforms, without modifications to the standard fabrication process, by employing non-conventional MOSFET transistors [5]. This approach can be used, for instance, to change the control paradigm of PICs from parallel to serial, thus reducing the required connections towards the control electronics. To this end, we integrated a multiplexer for sequential readout of sensors and a demultiplexer, together with a bank of high-current drivers, to serially operate the on-chip actuators (Fig. 3a). We tested this idea on a photonic circuit comprising an input switch matrix, to enable/disable the desired optical inputs, followed by a 4-channel coherent adder. The latter can be used for simultaneous communication and sensing purposes. By properly operating the on-chip actuators, the 4 input beams can be combined and extracted from a single output to recover a high-speed 25 Gbit/s modulated signal (Fig. 3b). At the same time, by analyzing the actuators command, the relative phase shift between pairs of input beams can be assessed in real-time, as shown in Fig. 3c. This can give information, for instance, on the phase-front characteristics or direction of arrival of the inputs.

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