From Multiphase to Novel Single-Phase Multichannel Shift-Clock Fast Counter Time-to-Digital Converter

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***Abstract*—With countless applications, time measurements are among industrial electronics' current most important challenges. This is not a matter of precision, which by now standard architectures have brought in the order of picoseconds and therefore at the physical limits of most common detection systems, but to the number of channels in continuous enormous growth. Just think about time-of-flight (TOF)-based applications like 3-D-imaging, time-of-arrival real-time locating systems, TOF positron emission tomography, and so on. This addresses the research on the design of new time-to-digital converters characterized by a huge number of channels and precision compliant with detectors' time resolution. In this context, field programmable gate array architectures provide fully digital and completely programmable solutions meeting the demands for flexible setups and speedy prototyping. The innovative contribution provided by the new counter architecture proposed consists of the reduction of the area required for implementation (only 110 SLICEs), with a consequent increase in the number of channels (up to hundreds in a tiny Aritx-7), much higher than the state-of-the-art multiphase solutions available today and of the new complete generation of the time estimates in real time, all while maintaining a state-of-the-art low power consumption and high resolution (up to 150 ps) and precision (up to 68.4 ps r.m.s.).**

***Index Terms*—Field-programmable gate array (FPGA), Nutt-interpolation, shift-clock fast-counter (SCFC), tapped delay-line (TDL), time-to-digital converter (TDC).**

I. Introduction

THANKS to recent developments in electronics, time interval measurements have advanced quickly, finding use in a wide range of time-of-flight (TOF)-based applications where time and space are connected by the constant speed of light. Just consider, to cite the most disruptive ones, 3-D-imaging in industry 4.0 for quality inspection and volumetric detection [1], automotive LiDAR scanners for self-driving [2], time-of-arrival real-time locating systems to automatically identify and track objects and people [3], and TOF positron emission tomography (TOF-PET) in diagnostics imaging [4]. This means that precisions of hundreds of picoseconds in time must be offered in order to guarantee the precision in space required for the majority of the applications previously stated. For this reason, time resolutions of used detectors are modest and limited to necessary for production cost restraint [5]. The time-to-digital converter (TDC), a fully digital type of time interval meter (TIM), is increasingly successful since it offers all the benefits of digital designs [6]. Complex mixed signaling is not necessary in this sense, to cite one of the most obvious advantages, principally simplifying the design in terms of engineering and production costs. The TDC can be implemented in an application-specific integrated circuit (ASIC) or, because of its fully digital structure, in a field programmable gate array (FPGA), which is currently a key resource due to its adaptability and extremely low nonrecurring engineering (NRE) costs, both in the R&D and production phases [7]. The TDC is most frequently implemented in FPGAs using delay lines or counter systems. The principal architecture of the first type is known as tapped delay-line (TDL) TDC (that is TDL-TDC), while for the other category the shift-clock fast-counter TDC (SCFC-TDC) is the most common one [8]. Of course, TDL and SCFC TDCs respond to different needs. In short, SCFC-TDCs accomplish lower resolution but require much less space for implementation than TDL-TDCs, which offer the maximum resolution at the tradeoff of a large area occupied. Therefore, TDL-TDCs are suited for applications needing very high performance in terms of resolution, while SCFC-TDCs for multichannel applications. In TDL-TDCs, the TDLs (Fig. 1) consist of chains of buffers, referred as bins or taps, each one being the unit of time quantization. As a consequence, TDL-TDCs provide resolutions, in first approximation, equal (or bigger) to the minimum propagation delay of the buffers in the technological node of the host device (e.g., $\sim$34 ps in 65-nm FPGAs, $\sim$25 ps in 40-nm FPGAs, $\sim$16 ps in 28-nm FPGAs) [9]. The TDL-TDC structure involves the use of considerable resources. First of all, the buffer chains of TDLs are intrinsically highly hardware-consuming, and the presence of

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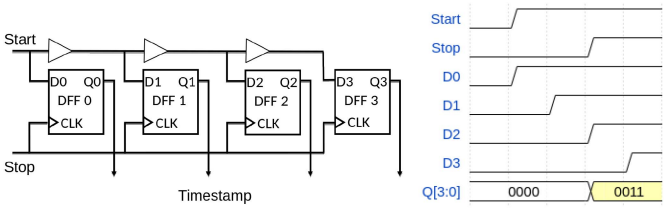

Fig. 1. Principle diagram of the TDL-TDC. (a) Architecture. (b) Waveforms.

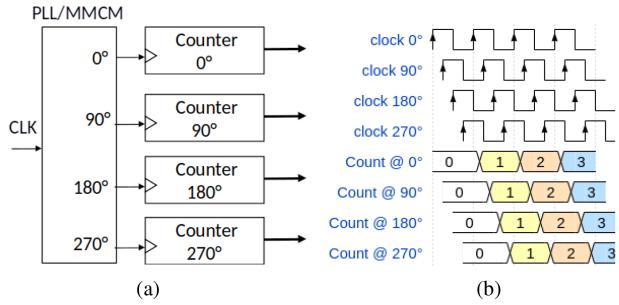

Fig. 2. Principle diagram of the SCFC-TDC. (a) Architecture. (b) Waveforms.

process and voltage-temperature fluctuations (PVT) determine mismatches among buffer delays that call for the implementation of a calibration mechanism (that consume hardware) in order to maintain high both resolution and and linearity [10]. Furthermore, in order to extend the full-scale range (FSR) and to get resolutions orders of magnitude below the minimum buffers delay value, two additional stages must be added to the basic structure, which are the Nutt-interpolator [11] to cope the former item and the subinterpolator [9], [12], [13] the latter one. Consequently, few channels can only be implemented in a single device due to the complexity of the entire resulting design, i.e., some units in small-size FPGAs (e.g., Xilinx 28-nm Artix7 family [14], [15]) up to few tens in medium-size FPGAs (e.g., Xilinx 28-nm Kintex-7 [16]). However, in high-size FPGAs (e.g., Kintex-7 [17] and Virtex-7 [18]) we can achieve hundreds of channels only if the processing, in order to save hardware and power, is done outside the FPGA. Last but not least, we must take into consideration that the purely asynchronous structure is affected by significant metastability issues on the sampling D-type flip-flops (DFFs) due to setup-and-hold time violations. Indeed, as can be seen from Fig. 1, the D inputs of the DFFs are connected directly, without any synchronization mechanism, to the Start signal and its delayed versions, which are completely asynchronous with respect to the Stop signal present at the CLK inputs. However, the structure does not present any critical issues regarding the skew between signals. In fact, the distribution structure of the clock signal (Stop in Fig. 1) within the FPGA ensures a skew lower than the minimum propagation delay of the buffers [19]. Furthermore, the topology of TDL itself prevents the output of the ith tap from being delayed compared to the output of tap $i-1$. On the other hand, the SCFC-TDC is a pure synchronous TDC built using several low hardware-consuming counters characterized by a resolution corresponding to the minimum clock period achievable in the technological node of the host device. Therefore, the counters can be driven (Fig. 2) by the same clock period but moved by an offset equivalent to the desired resolution, even though always orders of magnitude below TDL-TDC [20]. When it comes to area occupancy, SCFC-TDCs utilize a lot less space than TDL-TDCs, allowing for the implementation of more channels in a single FPGA device, even if small (e.g., Xilinx 6-Series 40-nm Spartan-6 and 28-nm 7-Series Artix-7 families). An evidence of this at different technological nodes (i.e., 65, 40, and 28 nm) and different FPGA's families (i.e., Spartan, Artix, Kintex, and Virtex) is reported in Table I. Scientific literature reports many examples of

TABLE I
OVERVIEW OF TIMING PERFORMANCE (I.E., LSB AND PRECISION) AND AREA OCCUPANCY (I.E., NUMBER OF CHANNELS IMPLEMENTED) IN TDL AND SCFC TDCS AT DIFFERENT TECHNOLOGICAL NODES AND FPGA FAMILIES (I.E., SLICE REPRESENTS THE TOTAL AVAILABLE UNITS IN THE DEVICE TO PROVIDE A COMPARATIVE METRIC)

Ref.	Type	LSB [ps]	Prec. [ps r.m.s.]	Num. Ch.	SLICE
[21]	TDL	45	18	2	N.A.
[22]	TDL	16.3	-	4	8,160
[23]	SCFC	138	-	64	11,200
[24]	SCFC	160	89.6	128	14,720
[25]	SCFC	625	255	32	11,200

(a) 65-nm 5-Series Virtex-5 FPGA family.

Ref.	Type	LSB [ps]	Prec. [ps r.m.s.]	Num. Ch.	SLICE
[26]	TDL	25.6	37	2	2,278
[27]	TDL	0.92	6	2	N.A.
[28]	TDL	7.7	8.9	8	23,038
[29]	SCFC	1000	500	17	11,662
[30]	SCFC	1000	430	4	11,662

(b) 40-nm 6-Series Spartan-6 FPGA family.

Ref.	Type	LSB [ps]	Prec. [ps r.m.s.]	Num. Ch.	SLICE
[31]	TDL	10	12.8	2	37,680
[32]	TDL	1.7	4.2	2	N.A.
[33]	SCFC	173.6	94.8	32	37,680
[34]	SCFC	312.5	184.7	32	37,680

(c) 40-nm 6-Series Virtex-6 FPGA Family.

Ref.	Type	LSB [ps]	Prec. [ps r.m.s.]	Num. Ch.	SLICE
[14]	TDL	22.3	26.04	2	33,650
[15]	TDL	2	12.5	16	33,650
[35]	SCFC	156	78	36	15,850
[36]	SCFC	138	73.6	64	28,000

(d) 28-nm 7-Series Artix-7 FPGA family.

Ref.	Type	LSB [ps]	Prec. [ps r.m.s.]	Num. Ch.	SLICE
[18]	TDL	10.54	14.59	96	108,300
[16]	TDL	10.6	8.13	64	50,950
[17]	TDL	9.4	9.5	128	50,950
[37]	SCFC	280	130	8	50,950
[38]	SCFC	89.9	56.2	256	50,950

(e) 28-nm 7-Series Kintex-7 and Virtex-7 FPGA family.

the so-called multiphase SCFC-TDCs (MP-SCFC-TDC), [20], [23], [25], [29], [30], [36], [37], [39], [40] in which the clock shifting is obtained by means of one or more phase-locked-loops (PPLs) or mixed-mode clock managers (MMCMs) [19]. So, the resolution corresponds to the clock period (e.g., bigger than 1.0 ns in Xilinx 28-nm 7-Series [37]) divided by the maximum number of clock nets that the FPGA can manage (e.g., Xilinx 28-nm 7-Series FPGAs offer 32 clocks nets with at maximum 16 clocks routed in the same clock zone). The high number of clock signals (also known as phases) with relative time skews [41] that must be controlled to maintain the resolution is the weak point of MP-SCFC-TDCs, which increases the system's complexity and portability between various configurations and FPGA types [24], [33], [34], [35], [38], [42]. A new single-phase SCFC-TDC (SP-SCFC-TDC) design is introduced to get around this restriction. The proposed SP-SCFC-TDC combine the absence of skew issues of TDL-TDC (due by the presence of the TDL and the distribution structure of the clock signal inside the FPGA) with the synchronous architecture of the MP-SCFC-TDC that, at difference with respect to the classical asynchronous TDL-TDC, minimize the metastability due to the setup-and-hold violations of the flip-flop. The rest of this article is organized as follows: In Section II, an MP-SCFC-TDC used as a reference is presented, and the novel SP-SCFC-TDC is presented in Section III. The experimental validations of the proposed architecture in 28-nm Xilinx 7-Series Artix-7 35 T (i.e., XC7A35T-1CPG236 C hosted in a Basys3 evaluation board [43]) and in Artix-7 100 T (i.e., XC7A100T-1CSG324C hosted in a Nexys4 evaluation board [44]) FPGAs are discussed in Section IV, demonstrating the possibility of implementing up to 64, 32, and 32 channels in the Artix-7 35 T (5,200 SLICE) and 128, 120, and 112 ones in the Artix-7 100 T (15,850 SLICEs) with resolutions of 625.5, 317.25, and 156.125 ps, respectively, using only 84, 108, and 110 SLICEs per channels and only one clock phase. Both MP and SP SCFC-TDC presented are organized as IP-Cores with an intuitive graphical user interface (GUI) that easily allows the user to set operating parameters, in particular the number of channels and the resolution.

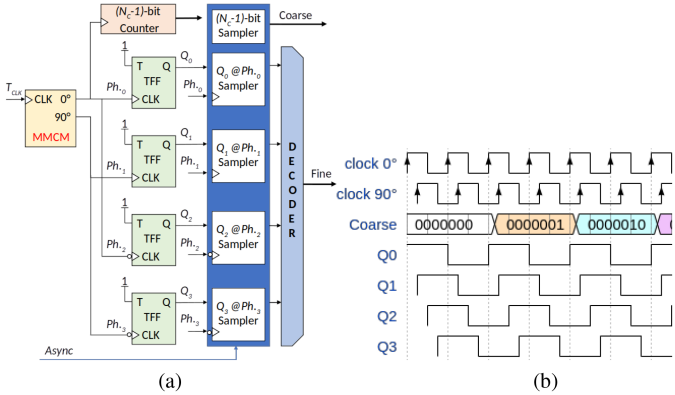

Fig. 3. MP-SCFC with one 8-bit coarse counter and 4 fine 1-bit TFF counters; $N_{PH} = 4$ and $N_C - 1 = 8 - 1$. (a) Architecture. (b) Waveforms.

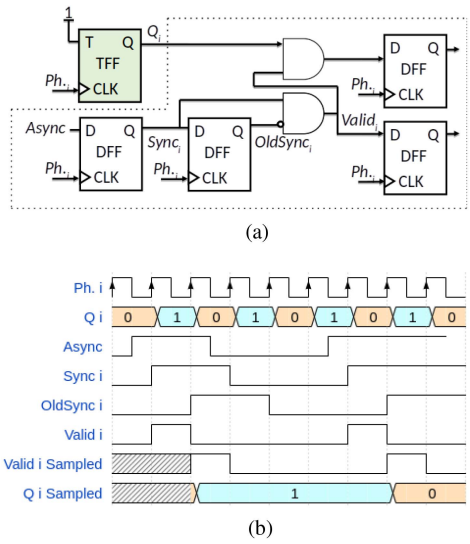

Fig. 4. Sampling of the fine part of a MP-SCFC. (a) In the box, the architecture of the generic sampler. (b) Waveforms considering only the generic phase ith.

II. Past Reference Multiphase SCFC-TDC Architecture

We have designed the MP-SCFC-TDC, taken as a reference, suitable for 28-nm Xilinx 7-Series FPGAs and organized as a tunable IP-Core [20], [23], [25], [29], [30], [36], [37], [39], [40]. Section II-A describes the design, and Section II-B reports implementation details and relative critical issues.

A. Design

According to [20], [23], [25], [29], [30], [36], [37], [39], [40], for hardware saving purpose, the MP-SCFC has not been implemented using the scheme of one N_C-bit wide counter per phase (Fig. 2) but, referring to the Nutt-interpolation, we have used only one $(N_C - 1)$-bit wide counter placed side-by-side to N_{PH} (i.e., number of phases) toggle-type flip-flops (TFFs) that are simple 1-bit wide counters. The $(N_C - 1)$-bit wide counter is the coarse counter, while the N_{PH} TFFs are the fine counters. Moreover, to maximize N_{PH} by lowering the number of the clock nets (N_{CLK}), we drive the stage of fine counters in double-data-rate (DDR) mode. In this way, we have $N_{PH} = 2 \cdot N_{\text{CLK}}$ (i.e., N_{CLK} is an even number) and the first $N_{PH}/2$ TFFs (from the 0 to the $N_{PH}/2 - 1$) work on the rising edge of the N_{CLK} clocks and the other $N_{PH}/2$ TFFs (from the $N_{PH}/2$ to the $N_{PH} - 1$) on the falling edge. Clock signals have the same period T_{CLK} and are generated using an MCMM at N_{CLK} outputs with a shift of $\Delta\varphi = 180°/N_{\text{CLK}}$ between phases. In this way, the N_{PH} TFFs explore $2 \cdot N_{PH}$ thermometric codes in $2 \cdot T_{\text{CLK}}$. Concerning the $(N_C - 1)$-bit wide counter, it is connected to a clock signal with 0° phase shift and period of $2 \cdot T_{\text{CLK}}$. Fig. 3 shows the architecture and waveforms of main signals of the MP-SCFC in case $N_C = 8$ and $N_{PH} = 4$.

In this way, in a single-channel MP-SCFC-TDC the outputs (N_{PH} outputs of the TFFs and the $N_C - 1$ bits of the coarse counter) are sampled by D-type flip-flops (DFFs), when the asynchronous physical event (Async) occurs. As shown in Fig. 4,

unlike what happens in TDL-TDCs, to avoid setup-and-hold violations in the flip-flops that constitute the sampler, the Async signal is synchronized by a DFF, one per phase, fed with the corresponding clock. By doing so, we have N_{PH} replicas (named Sync_0, $\text{Sync}_1, \ldots, \text{Sync}_{N_{PH}-1}$) synchronized to each of the N_{PH} phases. After that, each Sync_i (where $i \in [0; N_{PH}]$ and i represents the generic phase) is resampled by the same phase in order to generate OldSync_i (one per phase, i.e., OldSync_0, $\text{OldSync}_1, \ldots, \text{OldSync}_{N_{PH}-1}$). So, for each phase, the sampling process is concluded with the assertion of Valid_i (one per phase, i.e., Valid_0, $\text{Valid}_1, \ldots, \text{Valid}_{N_{PH}-1}$) when $\text{Sync}_i = 1$ and $\text{OldSync}_i = 0$ and the storage of the status of the ith TFF. After that, for avoiding to operate with multiple phases, all the sampled values are moved from the generic phase ith to phase 0 (a.k.a. master-phase) by means of a clock domain crossing (CDC). The coarse counter, synchronous with the master-phase, is sampled by $N_C - 1$ DFFs when $\text{Valid}_0 = 1$. Finally, the timestamp is constructed by combining coarse and fine measurements once data has been translated from thermometric to binary code, having FSR equal to $2^{N_C} \cdot T_{\text{CLK}}$ and resolution (LSB) equal to T_{CLK}/N_{PH}. Now, a multichannel MP-SCFC-TDC can be easily obtained by replicating the MP-SCFC and sampling circuit as many times as inputs are sharing the same MCMM. In addition, the system is set up as a configurable IP-Core enabling its simple usage.

B. Implementation Details

Having selected for implementation a 28-nm Xilinx 7-Series FPGA device, at maximum 16 clock nets can be routed in the same clock zone and 8 clocks can be managed by the MCMM [19]. In fact, MMCMs have eight outputs, which would require the use of three of them to get 16 channels, weakening the architecture efficiency due to consequent strong clock jitter. Due to this, 8 N_{CLK} is the maximum allowed (i.e., 16 for N_{PH}). Moreover, the timing analysis returns 2.5 ns as minimum clock period corresponding to 156.26 ps (i.e., 2.5 ns/16) of resolution. And here the first drawback of this architecture emerges: the technology of the selected host device, in terms of the amount of clock lines and MCMM resources, limits the achievable resolution.

In order to better focus MP-SCFC-TDC features and performance, thanks to the flexibility of the IP-Core, three different implementations have been considered (Table II), which are #1-MP with $N_{\text{CLK}} = 2$ ($N_{PH} = 4$) and 625-ps resolution, #2-MP with $N_{\text{CLK}} = 4$ ($N_{PH} = 8$) and 312.5-ps resolution, and #3-MP with $N_{\text{CLK}} = 8$ ($N_{PH} = 16$) and 156.26-ps resolution. In all implementations, the same FSR equal to 640 ns (i.e., $N_C = 8$) has been set. However, because the resolution value can only go as high as 500 ps, implementations with $N_{\text{CLK}} > 2$ are worthless. This is due to the second drawback of the MP-SCFC-TDC architecture: the time position of the asynchronous Async input with respect to the N_{CLK} clocks cannot be fixed with precision better than hundreds of picoseconds. For example, as shown in Fig. 5, if the skew of the time paths (ΔSkew) between two consecutive phases i and $i+1$ is greater than the LSB (i.e., $\Delta\text{Skew}_{i+1,i} > \text{LSB}$), the signal for that particular phase will always be sampled at the next clock edge corrupting the fine part of the measure. This second main drawback could be be effectively addressed by utilizing the "ones counter method" [45] and the "phase resort" technique [46], originally designed to resolve similar issues, such as bubble errors, in high-resolution (picoseconds) TDL-TDCs. Both solutions are also feasible for MP-SCFC-TDC; although, due to their high-resolution target, they would result in an excessively complex system for the required resolution (i.e., tens of picoseconds). The ones counter method entails analyzing data for each channel and compensating for nonidealities using an additional module, which could pose challenges when dealing with numerous channels or limited FPGA resources. On the other hand, employing the phase resort technique would necessitate intricate manual routing and/or comprehensive knowledge of implementation delays, potentially leading to a time-consuming process, particularly for multichannel implementations.

TABLE II
MP-SCFC-TDC DIFFERENT IMPLEMENTATIONS FEATURES

Figures	#1-MP	#2-MP	#3-MP
N_{CLK}	2	4	8
N_{PH}	4	8	16
T_{CLK} [ns]	2.5	2.5	2.5
Expected LSB [ps]	625	312.5	156.25
Measured LSB [ps]	625	500	500
$N_C - 1$	8-1	8-1	8-1
FSR [ns]	640	640	640
Num. LUTs/Ch	212	238	295
Num. FFs/Ch	336	431	446
Num. Ch. in Artix-7 35T	64	32	32
Num. Ch. in Artix-7 100T	128	120	112

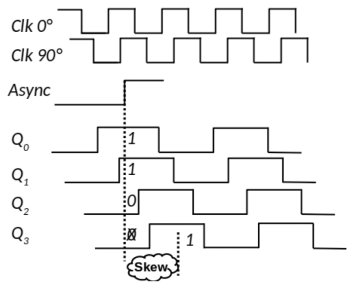

Fig. 5. Example of skew error in the MC-SCFC-TDC considering $N_{\text{CLK}} = 2$ ($N_{PH} = 4$). This results in the error of sampling "1100" instead of "1101" due to the skew of $Async$ with respect to the last phase. For simplicity, the sampler has been omitted and Async directly samples the phases.

III. Novel Single-Phase SCFC-TDC Architecture

To overcome the drawbacks of the MP-SCFC-TDC architecture (i.e., the limited number of N_{CLK} and the problem of the skew), we propose a single clock architecture using a chain of buffers that makes up a TDL, one per channel, instead of the MCMM that is common to all channels in the MP-SCFC-TDC. It is possible to observe that SP-SCFC-TDC combine the absence of skew issues of TDL-TDC (intrinsically due by the presence of the delay-line and the distribution structure of the clock signal into FPGA) with the synchronous architecture

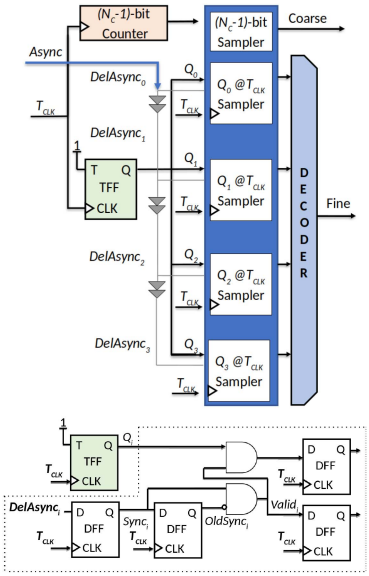

Fig. 6. Novel SP-SCFC-TDC architecture, single-channel, with $N_{PH} = 4$ (top) with highlighted the sampler (bottom).

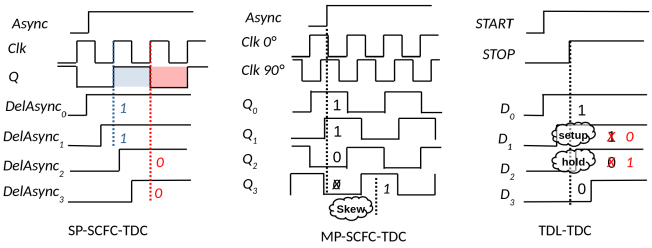

Fig. 7. Novel SP-SCFC-TDC waveforms (synchronous without skew) are compared with the MP-SCFC-TDC (synchronous with skew) and TDL-TDC (asynchronous with metastability issues but without skew).

offered by the MP-SCFC-TDC. As can be seen from Fig. 6, the output of each individual TFF (green) is sampled by the samplers (identical to those in Fig. 4), both driven by the same clock T_{CLK}. However, the asynchronous signals DelAsync_i, unlike in the TDL-TDC, are appropriately synchronized before being sampled by DFFs (white). In this way, SP-SCFC-TDC minimizes the metastability due to the setup-and-hold violations of the flip-flop. Fig. 6 depicts the developed architecture. The Async input is transmitted to the N_{PH} samplers, which are the same as in the MP-SCFC-TDC architecture, using a TDL, while the $(N_C - 1)$-bit coarse counter and only one TFF are supplied with the same clock with period T_{CLK} and phase 0° (i.e., the master-clock of the MP-SCFC-TDC solution). Fig. 7 presents the waveforms of the main nodes of the proposed architecture (SP-SCFC-TDC), which are not affected by skew, metastability, and are synchronized to the clock, comparing them with those of the MP-SCFC-TDC (synchronous but subject to skew) and the TDL-TDC (asynchronous, hence subject to metastability, setup, and hold time violations). In case of 28-nm Xilinx 7-Series FPGAs, the carry-chain resources (i.e., CARRY4) on the device are used to implement the TDL. Precisely, a proper number

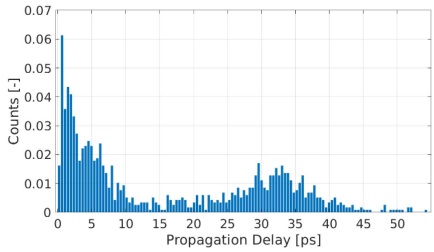

Fig. 8. Experimental measurement of the distribution of the propagation delays in a TDL ($N_{\text{TAP}} = 256$) implemented in 28-nm Xilinx 7-Series device.

of CARRY4 resources (N_{CARRY4}) are cascaded to give a TDL composed by N_{TAP} taps (i.e., $N_{\text{TAP}} = 4 \cdot N_{\text{CARRY4}}$) with total delay a bit bigger than T_{CLK}. So, considering that each tap has a propagation delay t_p comparable to the minimum one offered by the technological node (i.e., 16 ps in 28-nm devices), it is possible to choose at which step ΔN_{TAP} to extract the N_{PH} delayed Async, called DelAsync_i (one per phase: DelAsync_0, $\text{DelAsync}_1, \ldots, \text{DelAsync}_{N_{PH}-1}$) to be sent to the samplers. Thus, considering that ΔN_{TAP} taps must introduce a delay equal to the desired LSB, we have to set $\Delta N_{\text{TAP}} = \text{LSB}/t_p$ and, obviously, $N_{\text{TAP}} \geq T_{\text{CLK}}/t_p$. In this design, the choice of $N_{\text{TAP}} = 256$ (i.e., $256 > 2.5\,\text{ns}/16\,\text{ps} \simeq 157$) corresponds to $N_{\text{CARRY4}} = 64$.

However, because it was not intended to be a specific timing resource, the CARRY4 primitive displays PVT fluctuations (as predicted in Section I) in the time delay between the four taps inside the same CARRY4 and to other CARRY4 stages. The propagation delay for the 28-nm Xilinx 7-Series, shown in Fig. 8, can vary by nearly 300% from the mean value (i.e., $\sim$16 ps), corresponding to a maximum of $\sim$50 ps (i.e., ultrabin) and a minimum of $\sim$1 ps. The temporal length of ΔN_{TAP}, a consequence of the central limit theorem, remains almost constant and numerically tends to $\Delta N_{\text{TAP}} \cdot t_p$, even in the presence of considerable dispersion in propagation delays, provided that ΔN_{TAP} is sufficiently large. In Section IV, this claim will be experimentally confirmed. We would like to highlight that the proposed SP-SCFC-TDC employs a merging method for the taps. Similar but more hardware-intensive methods, designed for achieving high-resolution (picoseconds) in TDL-TDCs, are proposed in [47] and [48]. However, our proposed solution offers a simpler and more resource-efficient implementation, making it suitable for multichannel applications on smaller FPGAs with resolutions in the tens of picoseconds. In analogy with the MP-SCFC-TDC IP-Core introduced in Section II, the ΔN_{TAP} and not the N_{CLK} fixes the resolution, the FSR is equal to $N_C \cdot T_{\text{CLK}}$ and the LSB is equal $\Delta N_{\text{TAP}} \cdot t_p$. In this way, the resolution of the proposed SP-SCFC-TDC is no more constrained by the clock resources (i.e., $\text{LSB}_{MP} = T_{\text{CLK}}/N_{PH}$) but only depends on the taps propagation delay (i.e., $\text{LSB}_{SP} = \Delta N_{\text{TAP}} \cdot t_p$). Second, the problem of the skew is also eliminated, since the sampling is performed along the sequence of buffers and the skew between two samplers is negligible thanks to the structure of the CARRY4 stage.

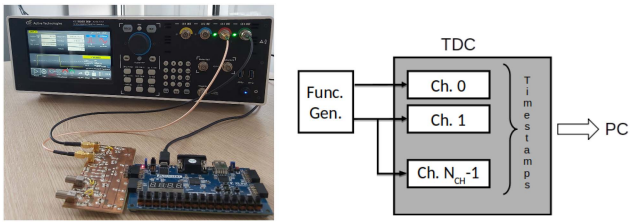

Fig. 9. Block diagram (rigth) of the experimental setup photo with Basys3 (left). To minimize the number of connectors, the channel 0 is directly connected to the function generator and all the other $N_{CH}-1$ channels to a delayed replica.

IV. Measurements

Experimental comparisons are made between the proposed SP-SCFC-TDC and systems that are currently available in literature, and with the reference MP-SCFC-TDC. In particular, Section IV-B compares the three implementations of MP-SCFC-TDC, i.e., #1-MP, #2-MP, and, #3-MP (Section II-B and Table II) with the correspondent SP-SCFC-TDC implementations named #1-SP, #2-SP, and #3-SP. All the TDCs have the same T_{CLK} equal to 2.5 ns and FSR equal to 640 ns (i.e., $N_C - 1 = 8 - 1$). Finally, Section IV-C compares MP-SCFC-TDC and SP-SCFC-TDC architectures with systems available in literature at the state of the art. While Section IV-A reports the measurement setup and the methods used to calculate the figure of merits.

A. Measurement Setup

A host computer processes the timestamps from the MP-SCFC-TDC and SPSCFC-TDC multichannel (N_{CH}) implementations in order to determine the resolutions, precisions, and respective differential and integral nonlinearity (DNL/INL). The clock signals necessary to the TDCs are provided by the oscillator available on the Basys3 and Nexys4 boards used as support hardware, while the Async signals are created by an external function generator. The setup layout is graphically represented in Fig. 9. The standard deviation (σ_{i0}) of the distribution of the differences between timestamps of the ith channel and of channel 0 is referred as channel-to-channel precision, i.e., $\sigma_{i0} = \sqrt{\sigma_i^2+\sigma_0^2}$; it mathematically correspond to the contribution of the single-shot precision of channel ith (σ_i) and channel 0 (σ_0); i.e., $\sigma_{i0} = \sqrt{\sigma_i^2+\sigma_0^2}$. To determine the DNL and INL of the generic ith channel, a code-density-test (CDT), i.e., the histogram of the occurrence, over the fine part of timestamps is performed [49]. In this manner, an estimation of the propagation delay of the N_{PH} phases is performed normalizing the histogram by the dynamic-range of 2.5 ns offered by the fine part (i.e., T_{CLK}). The average of the time duration of bins of the CDT is assumed as index of resolution. While bin-by-bin relative DNL and INL curves are derived by differentiation of the CDT, for the DNL, and successive integration, for the INL. Furthermore, according to measure theory, the generic ith channel precision is $\text{LSB}_i/\sqrt{12}$ if jitters and linearity errors are negligible (i.e., the ENOB of the system coincides with the LSB), which means that $\sigma_{i0} = \sqrt{\text{LSB}_i^2/12+\text{LSB}_0^2/12}$, where LSB_0 and LSB_i represent the resolutions of channels 0 and ith.

TABLE III
MP-SCFC-TDC versus SP-SCFC-TDC Hardware Occupancy

Figures	#1 MP	#2 MP	#3 MP	#1 SP	#2 SP	#3 SP
N_{PH}(MP only)	4	8	16	-	-	-
ΔN_{TAP} (SP only)	-	-	-	39	20	10
$N_C - 1$	8-1	8-1	8-1	8-1	8-1	8-1
Num. LUTs/Ch	212	238	295	212	238	295
Num. FFs/Ch	336	431	446	333	424	431
Num. MCMM (MP only)	1 for all Channels			0	0	0
Num. CARRY4/Ch (SP only)	0	0	0	64	64	64
Num. SLICE/Ch	84	108	110	84	108	110
Ch. % in Artix-7 35T	1.61	2.07	2.11	1.61	2.07	2.11
Ch. % in Artix-7 100T	0.53	0.68	0.69	0.53	0.68	0.69
Num. Ch. in Artix-7 35T	64	32	32	64	32	32
Num. Ch. in Artix-7 100T	128	120	112	128	120	112

TABLE IV
SP-SCFC-TDCs Nonlinearity Errors

	#1 SP	#2 SP	#3 SP
ΔN_{TAP}	39	20	10
Exp.LSB [ps]	624	320	160
Meas.LSB [ps]	625.5	317.25	156.125
DNL/INL [% LSB]	4.5/4.5	26.4/20.3	23.3/26.4

In light of the fact that all channels, roughly speaking, have the same resolution LSB (i.e., $\text{LSB}_i \simeq \text{LSB}_0$), we can assume $\sigma_{i0} = \sqrt{\text{LSB}^2/6}$ as channel-to-channel precision.

B. MP-SCFC-TDC versus SP-SCFC-TDC

We must set the ΔN_{TAP} value of the SP-SCFC-TDC to have nearly identical LSB values in order to compare MP- and SP-SCFC-TDCs fairly. By setting $\Delta N_{\text{TAP}} = 39$, the LSB value for #1-SP is in theory $39 \cdot 16$ ps $= 624$ ps and 625.5 ps measured, which is compatible with the #1-MP LSB equal to 625 ps. Similarly, $\Delta N_{\text{TAP}} = 20$ in #2-SP corresponds to theoretical LSB equal to $20 \cdot 16$ ps $= 320$ ps and 317.25-ps measured as compared to 312.5 ps of #2-MP LSB. Finally, $\Delta N_{\text{TAP}} = 10$ in #3-SP determines theoretical LSB equal to$10 \cdot 16$ ps $= 160$ ps and 156.125 ps measured as compared to 156.25 ps of #3-MP LSB.

1) Hardware Occupancy: First of all, we have investigated the hardware occupancy of MP-SCFC-TDCs and SP-SCFC-TDCs, which differ, as Figs. 4 and 6 show, by $N_{PH} - 1$ TFFs per channel and for the presence of one MCMM in MP-SCFC-TDCs replaced by 64 CARRYs per channel in SP-SCFC-TDCs. Table III displays the resources used by the two architectures in the selected target device and in some others belonging to different families.

2) Linearity and Resolution: Linearity and resolution of #1-SP, #2-SP, and #3-SP have been investigated through the CDTb etween the N_{PH} phases composed by ΔN_{TAP} taps. Measured CDTs and bin-by-bin relative DNL and INL curves are shown in Fig. 10. Table IV summarize the measured resolution or LSB (Meas. LSB), the expected one (Exp. LSB) and, the DNL/INL errors (i.e., the maximum magnitude of the bin-by-bin curves). The conclusion in Section III, which states that if the

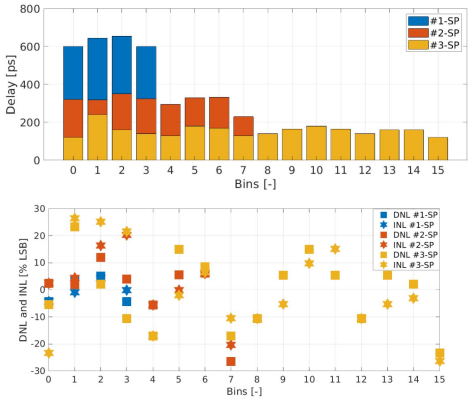

Fig. 10. CDT (top) and bin-by-bin DNL and INL curves (bottom) over #1-SP (blue), #2-SP (red), and #3-SP (orange).

TABLE V
MP-SCFC-TDC VERSUS SP-SCFC-TDC PRECISIONS

Ch-Ch Prec. [ps r.m.s.]	#1 MP	#2 MP	#3 MP	#1 SP	#2 SP	#3 SP
σ	180	144	144	180	92.3	68.4
σ_{i0}	255	204	198	255.5	130.5	96.8
$(\text{Exp. LSB})/\sqrt{6}$	255.5	127.6	63.8	254.7	130.6	65.3
$(\text{Meas. LSB})/\sqrt{6}$	255.5	204	204	255.4	129.5	63.7

dispersion of propagation delays is high and ΔN_{TAP} is sufficiently great, ΔN_{TAP}, as a consequence of the central limit theorem, the time duration of ΔN_{TAP} (i.e., the Meas. LSB) remains almost constant approximating the Exp. LSB to $\Delta N_{\text{TAP}} \cdot t_p$, is supported by the data in Fig. 10. Because the propagation delay demonstrates a maximum dispersion (ultra-bin) that is negligible compared to the LSB, it is feasible to operate in a hardware-saving mode without calibration while maintaining low relative DNL and INL.

3) Precision: Considering both expected and measured LSBs, i.e., Exp. LSB and Meas. LSB, respectively, (with $\text{LSB}_{MP} = T_{\text{CLK}}/N_{PH}$ and $\text{LSB}_{SP} = \Delta N_{\text{TAP}} \cdot t_p$), Table V displays the average values of the singe-shot (σ) and channel-to-channel precisions (σ_{i0}) measured in the various implementations and the related LSBs. The proposed SP-SCFC-TDC's advantage to the MP-SCFC-TDC is thus made clear. In fact, the observed LSB value of 500 ps corresponds to the measured accuracy limit of 204 ps r.m.s. in MP-SCFC-TDC implementations (see Section II-B).

4) Temperature Fluctuation: Unlike the MP-SCFC-TDC, where the MCMM/PLL generating the phases incorporates analog temperature compensation mechanisms, the delay-line of the SP-SCFC-TDC is uncalibrated and uncompensated. As a result, the various taps are subject to fluctuations induced by temperature variations, leading to an LSB dispersion. Consequently, the percentage dispersion of the LSB for #1-SP, #2-SP, and #3-SP was characterized by varying the FPGA temperature between 20 °C and 80 °C with 5 °C steps using a climatic chamber. The results, depicted in Fig. 11, reveal that #1-SP and #2-SP exhibit a dispersion lower than 6% (i.e., 37.5 and 19 ps in absolute value over an Meas. LSB of 625.5 and 317.25 ps respectively), while

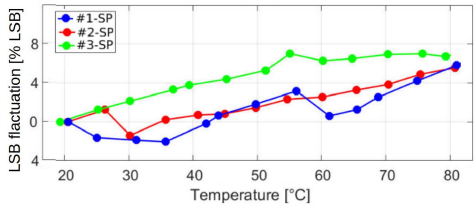

Fig. 11. LSB flactuation as function of temperature over #1-SP (blue), #2-SP (red), and #3-SP (orange).

TABLE VI
COMPARISON BETWEEN STATE-OF-THE-ART MP-SCFC-TDC ARCHITECTURES IN LITERATURE AND THE #1-MP IMPLEMENTATION

Ref.	$\frac{T_{\text{CLK}}}{N_{PH}}$ [ns]	LSB [ps]	DNL/INL [%]	Prec [ps]	Num. Ch.	FPGA (SLICEs)
[23]	2.22/16	138	28.9/-	-	-	Virtex-5 (11,200)
[20]	5.04/4	1400	40/-	700	-	N.A.
[25]	2.5/4	625	7/7	255	32	Virtex-5 (11,200)
[29]	4.0/4	1000	52/39	500	17	Spartan-6 (11,662)
[39]	3.13/4	780	40/5	280	24	Kintex-7 (N.A.)
[30]	4.0/4	1000	N.A.	430	4	Spartan-6 (11,662)
[40]	3.13/4	780	N.A.	250	24	M2GL010T (12,084)
[36]	3.33/24	138	N.A.	73.6	64	Artix-7 (28,000)
[37]	1.13/4	780	53/280	280	8	Kintex-7 (50,950)
#1-MP	2.5/4	625	N.A.	255	103	Artix-7 (15,850)

SLICE represents the total available units in the device to provide a comparative metric.

#3-SP shows a dispersion lower than 8% (i.e., 12.5 ps in absolute value over an Meas. LSB of 156.125 ps). These values can be considered negligible concerning the resolution, the precision, and DNL/INL errors.

C. State of the Art

Table VI compares available MP-SCFC-TDC implementations at state of the art and the #1-MP in Artix-7 100 T, which represents the best compromise between timing performance (i.e., LSB, DNL/INL, and precision) and area occupancy (i.e., number of channels and number of slices available in the FPGA). Table VII compares the proposed SP-SCFC-TDC with available SCFC-based TDC architectures, in which the drawbacks of the SCFC are solved using custom routing [34], [38] (first block of elements in the table), constraints [24], [33] (second block), and use of SERDES [35], [42] (third block). Moreover, hardware-consuming but high-resolution (picoseconds) subinterpolating architectures, e.g., PLL delay-matrix TDC [50] (997 SLICEs, LSB of 17.73 ps in a medium-size Virtex-6 FPGA), can be adopted in order to increase the resolution of the SCFC-based TDC up to few picoseconds. However, these subinterpolating techniques make it possible to implement hundreds of channels only in medium/high-size FPGAs.

TABLE VII
COMPARISON BETWEEN STATE-OF-THE-ART SCFC-BASED TDC ARCHITECTURES IN LITERATURE AND THE #1-SP, #2-SP, AND #3-SP IMPLEMENTATIONS OF THE PROPOSED SOLUTION

Ref.	$\frac{T_{CLK}}{N_{PH}}$ [ns]	LSB [ps]	DNL/INL [%]	Prec [ps]	Num. Ch.	FPGA (SLICEs)
[38]	1.43/16	89.9	87/82	56.2	256	Kintex-7 (50,950)
[34]	5.00/16	312.5	4.5/4.5	184.7	32	Virtex-6 (37,680)
[24]	2.57/16	160	20/-	89.6	128	Virtex-5 (14,720)
[33]	2.78/16	173.6	3.5/3.5	94.8	32	Virtex-6 (37,680)
[35]	1.25/8	156	32/100	78	2	Artix-7 (15,850)
[42]	4.76/4	1190	N.A.	500	32	Cyclone III (N.A.)
#1-SP	-	625	4.5/4.5	255.5	103	Artix-7 (15,850)
#2-SP	-	317	26/20	130.5	93	Artix-7 (15,850)
#3-SP	-	156	23/26	96.8	64	Artix-7 (15,850)

SLICE represents the total available units in the device to provide a comparative metric.

V. CONCLUSION

The performance requirements for time interval meters are continuously increasing, both in terms of precision and the ability to integrate numerous channels (up to hundreds) on a single device. The MP-SCFC-TDC architecture excellently meets these requests, but having structural issues (i.e., the limited phases N_{PH} and the problem of the skew) that limit the resolution at 500 ps if no hardware-consuming architectures (e.g., the ones counter method, the phase resort, and the PLL delay-matrix, just to cite the most effective) are introduced. This was the motivation that led to develop and propose the novel architecture SP-SCFC-TDC, which overcomes all drawbacks of the MP-SCFC-TDC by granting both high performance and low area occupancy. The proposed SP-SCFC-TDC, similar to TDL-TDCs, utilizes a delay-line and a single clock distributed through the clock resources of the FPGA to quantize the temporal events for digitization, thereby limiting the effects of skews. However, unlike the purely asynchronous nature of TDL-TDCs, it adopts the sampling techniques of MP-SCFC-TDC, which is a synchronous structure. This design choice minimizes metastability issues that may arise from violations of setup-and-hold times. For validation purpose, three implementations (i.e., #1-SP, #2-SP, and #3-SP) in 28-nm Xilinx 7-Series Artix-7 FPGAs (i.e., Artix-7 35 T and Artix-7 100 T) have been performed, having, respectively, resolutions of 625.5, 317.25, 156.125 ps and single-shot precision of 180, 92.3, and 68.3 ps r.m.s. In addition, the suggested architecture's relatively low resource usage (84 SLICEs for #1-SP, 108 SLICEs for #2-SP, and 110 SLICEs for #3-SP) enables the implementation of up to 32/64 channels in Artix-7 35 T (5 k SLICEs) and 112/128 channels in Artix-7 100 T (15 k SLICEs). Last but not least, DNL and INL are always lower than the 26.4% of the LSB. The suggested TDC is also designed as an IP-Core, making it simple for the user to modify each operating parameter separately.‘

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