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Note: Differential configurations for the mitigation of slow fluctuations limiting the resolution of digital lock-in amplifiers

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The resolution of digital lock-in amplifiers working with a narrow bandwidth (<100 Hz) is limited by slow fluctuations, which can be two orders of magnitude larger (μV range) than the noise of the input amplifier (tens of nV). In order to tackle this issue, affecting state-of-the-art laboratory instrumentation and here systematically quantified, three differential sensing configurations are presented. They adapt to different setup conditions and are based on manual and automatic tuning of dummy references, allowing a 25-fold resolution improvement for enhanced long-term tracking of impedance sensors. © *2016 AIP Publishing LLC.* [http://dx.doi.org/10.1063/1.4941721]

Lock-in amplifiers (LIAs) are extensively used for signal recovery and phase-sensitive detection in a wide range of scientific fields, from optics,[1] Raman spectroscopy,[2] atomic force microscopy[3] to gas sensing,[4] just to name a few. The multiplication operation, that is the core of the LIA,[5] can be made in several ways[6] including analog mixers, in both integrated-[4] and discrete-component implementations (with sinusoidal or square-wave references), as well as in embedded digital processors[7] and PC-based software.[8]

In the last decades, digital implementations have outperformed analog instruments, allowing reaching superior performance in terms of wider bandwidth, wider range of adjustable parameters, better accuracy, and, of course, versatility. The standard architecture of a digital LIA is shown in Fig. 1. A digital processing platform (typically a Field-Programmable Gate Array (FPGA)) takes care of the generation of the reference sinusoid and of the demodulation of the input signal. The sinusoidal signal is often digitally generated by means of a Direct Digital Synthesizer (DDS)[9] and converted into an analog signal by a Digital-to-Analog Converter (DAC). This can be followed by a filtering and amplification stage with variable gain G_{OUT} to allow the generation of a wide amplitude range of sinusoids. Similarly, the input signal V_{IN} is amplified by a variable-gain stage (G_{IN}), sampled by an Analog-to-Digital Converter (ADC) and digitally multiplied by the internal references in phase and in quadrature and finally low-pass filtered with adjustable bandwidth BW.

When narrowing the BW in the Hz range, the experimental evidence is that the output of a digital LIA shows slow fluctuations, several orders of magnitude larger than the noise expected from the output and input analog stages of the instrument. In this study, we experimentally characterize this effect and propose simple correction techniques, based on differential configurations, which allow a significant mitigation of this detrimental effect that is severely limiting the minimum detectable signal in measurements with a BW below 100 Hz.

The systematic investigation of the instrument noise in different conditions (see input configurations in Fig. 2) has been performed on two commercial digital lock-in instruments (SRS830 by Stanford Research Systems and HF2LI by Zurich Instruments) and on a custom-made digital prototype.[9] For the sake of simplicity, we report, in Fig. 3, the results obtained with the HF2LI instrument (operated at f_{AC} = 1 MHz and BW = 1 Hz), as similar behavior has been observed in the other instruments. With no input signal (grounded input) the noise is only due to the input front-end and has the expected values reported in the datasheet, scaling correctly with the input range, i.e., with G_{IN} (Figs. 3(a)-3(d)). The lowest achievable noise is 5 nV with maximum gain (input range of 1 mV, case a), while it is 76 nV with 2 V input range (case d). Thus, the best expected resolution of the LIA should be 0.03 ppm. However, when the reference sinusoid V_{OUT} is connected directly to the input (bridged as shown in Fig. 2(a)), the noise surprisingly increases: by ranging the signal amplitude from 1 mV up to 1 V (cases e, g, h, i, and j), the noise scales up proportionally, reaching a rms value of 27 μV at 1 V (case e). This value is 355 times worse than the grounded input case and corresponds to a resolution of 27 ppm. Note that the resolution results to be approximately constant at 25 ppm in all cases (except for 1 mV, 40 ppm), showing the practical impossibility to reach sub-ppm resolution. A change of a factor of 20 (from 0.1 V to 2 V) of the input range does not influence the resolution (cases g and h, V_{OUT} = 100 mV). Neither the use of an external reference signal (Agilent 33250A arbitrary waveform generator) is beneficial (case k, noise of 36 μV even worse than the 27 μV of case e), demonstrating that the noise worsening is an intrinsic limitation of the lock-in architecture. To confirm that the noise turns to be proportional to the signal, a V_{OUT} of 1 V has been directly bridged to both differential inputs of the instrument (Fig. 2(b)) so to process a signal that is ideally equal to zero, obtaining a noise of 156 nV (case f), a value similar to the grounded input case d. Based on this evidence, i.e., the instrument resolution in terms of ppm does not change with the signal amplitude, we present three differential configurations allowing a resolution enhancement without any modification of the lock-in instrument.

We focus, in particular, on impedance detection in which the LIA is used to track, in real-time, the variations of impedance ΔZ_s (measured between two electrodes) due to variations of physical transducers.[10–12] The proposed differential configurations aim at achieving an input signal proportional to the desired ΔZ_s, so to attribute the resolution limit of 25 ppm to ΔZ_s and not to the full impedance Z_s. To

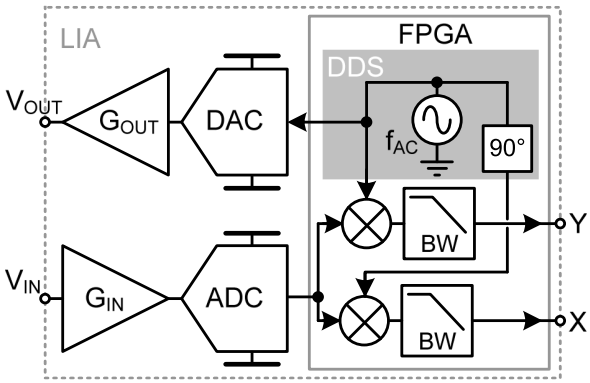

FIG. 1. Architecture of a digital lock-in amplifier based on FPGA signal processing and virtual direct digital synthesizer (DDS).

perform impedance measurements, as illustrated in Fig. 2(c), one electrode of the unknown impedance Z_s is connected directly to V_{OUT}, while an external transimpedance amplifier (TIA) is commonly used to convert the current collected at the companion electrode into a voltage sampled at the instrument input V_{IN}. Note that proper adoption of advanced TIA topologies[13–15] can reduce the front-end noise to a negligible value with respect to the LIA slow fluctuations. For example, in the case of a capacitive sensor with a capacitance C_S larger than the capacitance of the amplifier, the signal-to-noise ratio (SNR) of a capacitance variation of ΔC_S and a noise limited by the equivalent input voltage noise $\left(\overline{e_{OA}^2}\right)$ of the TIA is

$$SNR = \left(\frac{\Delta C_S}{C_S}\right)^2 \frac{V_{out}^2}{2 \cdot \overline{e_{OA}^2} \cdot BW}. \quad (1)$$

By using common values as $V_{out} = 1$ V, $\overline{e_{OA}^2} = \left(5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}\right)^2$, and BW = 1 Hz, a resolution better than 0.01 ppm could be reached, well below the limitations given by the LIA.

In high-resolution sensing applications, the absolute value of the impedance Z_s is usually not relevant while its tiny variations ΔZ_s (down in ppm range) must be tracked. The adoption of a differential sensing configuration indeed allows canceling the injected signal in the initial conditions (baseline) by means of an additional compensation circuit matched to Z_s so that only the variations with respect to the symmetric balanced condition are amplified and recorded. The subtraction can be achieved in current mode (i.e., at the virtual ground of the TIA before amplification) or in voltage mode (i.e., by means of a differential amplifier connected to the output of the TIA). Both approaches have the additional

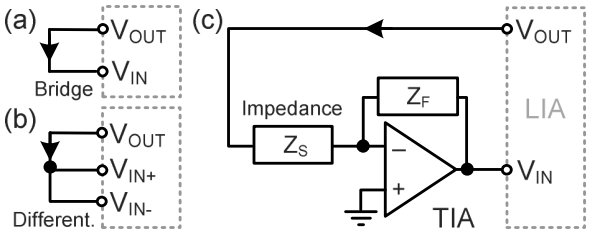

FIG. 2. Test configurations considered here: direct bridging of (a) single-ended and (b) differential inputs with the output and (c) use of an external transimpedance amplifier (TIA) with a feedback impedance Z_F for measuring the unknown impedance Z_S.

Condition	$Range_{IN}$ [V]	V_{OUT} [V]
Grounded In	0.001	-
Grounded In	0.1	-
Grounded In	1	-
Grounded In	2	-
Bridge In-Out	2	1
Differential	2	1
Bridge In-Out	2	0.1
Bridge In-Out	0.1	0.1
Bridge In-Out	0.1	0.01
Bridge In-Out	0.1	0.001
External Gen.	2	1

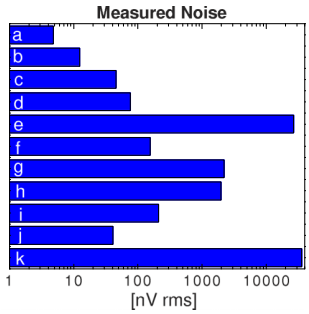

FIG. 3. Noise characterization of the HF2LI for various input configurations and signal amplitudes (recording time of 1 minute).

advantage of reducing the useful signal at the input of the LIA thus relaxing the requirement on its dynamic range.

Current subtraction can be implemented in two ways. In solution A (Fig. 4(A)), the sensor C1 is coupled with an identical replica C2, with the common terminal connected to the virtual ground and the other terminal driven by an inverting buffer in counter-phase with V_{OUT}. If the two impedances are perfectly matched and the inverting buffer is ideal, all the current flowing in C1 flows in C2 and no current is amplified by the TIA, leading to a zero voltage at V_{IN}. Any imbalance between the two arms of the sensor (behaving as a half bridge with differential driving) produces a nonzero current signal that is amplified and demodulated by the LIA. Given that the slow fluctuations added by the instrument are proportional to the small imbalanced signal, an overall improvement of resolution with respect to the measurement of the full signal is achieved.

When the technology does not allow the fabrication of a differential sensor, a separate compensation impedance (such as the dummy capacitor C_C in Fig. 4(B)) could be added which has a value close to the expected sensor impedance (C_S in Fig. 4(B)). In this solution B, a variable-gain inverting

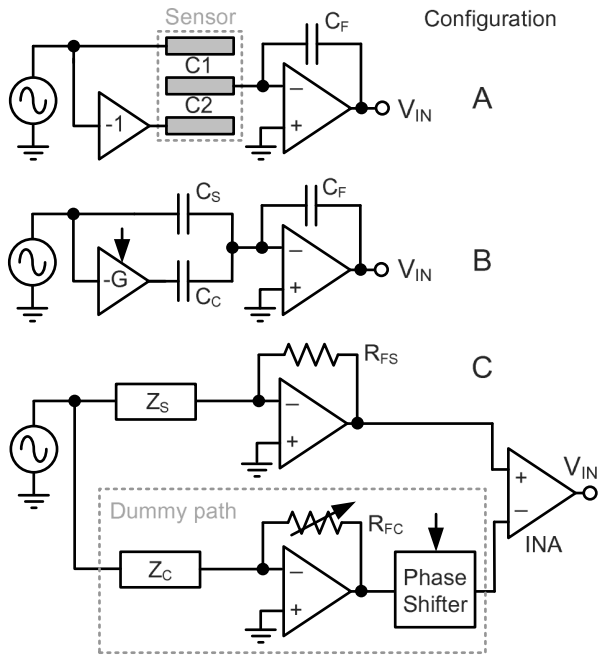

FIG. 4. Differential configurations with a subtraction in current mode: (a) for matched sensors C1-C2 and (b) with tunable gain G to match C_C with C_S. (c) Differential subtraction in voltage mode of a compensation signal coming from a parallel dummy path with tunable gain (R_{FC}) and phase.

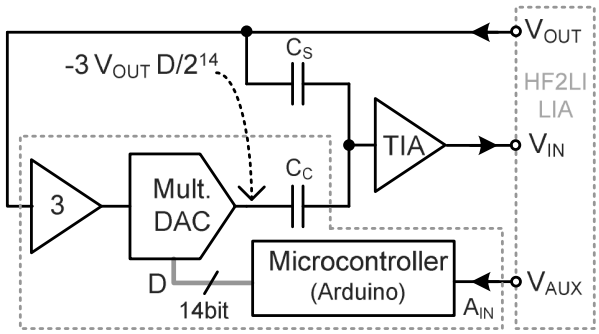

FIG. 5. Implementation of the automatic compensation circuit of solution B for cancelling C_S with current subtraction at the virtual ground by automatically tuning the voltage applied to C_C.

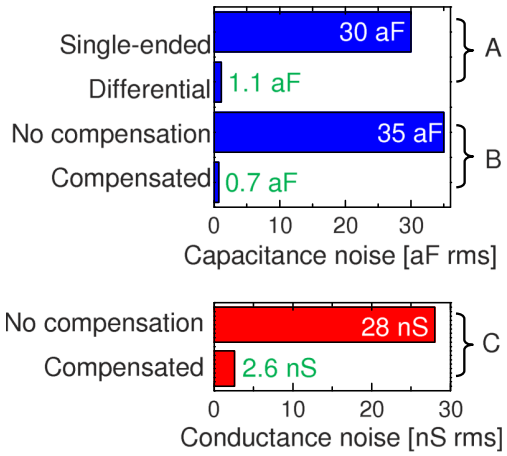

FIG. 6. Experimental examples of the effectiveness of noise reduction of the three proposed techniques: (a) and (b) for capacitance sensing and (c) for conductance.

amplifier (G) allows precise tuning of the counter-injected current to obtain perfect cancellation, i.e., accurate matching between the currents in C_C and in C_S.

Similarly, solution C, in Fig. 4, consists of the addition of a full signal chain in parallel to the sensor impedance Z_S, including a dummy impedance Z_C, a second TIA, and, if necessary, a phase shifter to be tuned, together with R_{FC}, to adjust the magnitude and phase of this auxiliary signal path. The output voltage of the dummy path is subtracted from the signal path by a differential amplifier, leading to only the residual small signal to be processed by the LIA.

The details of the hardware implementation of solutions A and C are reported in specific works, focusing on capacitive sensing of dust microparticles in air[11] and on detection of magnetic beads guided by nano-magnetic rails in liquid,[16] respectively. A major limit of solution B (and C) is the need for manual tuning of the variable-gain amplifier. In order to address this inconvenience, we realized an automatic canceling system whose simplified scheme is illustrated in Fig. 5. A high resolution and wide bandwidth digitally controlled variable-gain amplifier has been designed using a 14-bit multiplying DAC (AD5446) featuring a bandwidth of 12 MHz and a large output swing (±10 V). During the calibration of the compensation path, the microcontroller (Arduino Uno) automatically adjusts the digital input of the DAC in order to minimize the signal at the input of the LIA, i.e., to balance the differential structure. The amplitude of the signal measured by the LIA is made available on its auxiliary analog output and read using the ADC of the microcontroller. A compensation capacitance of $C_C = 1$ pF and a low-noise amplifier with a fixed gain of 3 complete the compensation path. The values have been chosen in order to compensate C_S up to 3 pF with a resolution of 14 bit (capacitance steps of about 180 aF) and a negligible effect on the noise of the TIA. The compensation path works up to a few MHz. For higher frequencies, the phase delay added by the DAC prevents an effective cancellation of the current injected by C_S.

The experimental results, all obtained with the HF2LI and summarizing the effectiveness of the proposed solutions, are reported in Fig. 6. For solution A, employing a TIA with capacitive feedback ($C_F = 1$ pF) and a triplet of matched band electrodes,[11] the switch from a single couple of electrodes to a differential configuration allows a reduction of the noise from 30 aF down to 1.1 aF ($V_{OUT} = 1$ V, $f_{AC} = 1$ MHz, BW = 1 Hz). The resolution is improved by a factor of 27 reaching ≈2 ppm. The performance is still limited by the slow fluctuations of the lock-in amplifier because of the imperfect matching between C1 and C2 (mismatch of 5% limited by lithography of the microelectrodes). For solution B, implemented with the system of Fig. 5 with a $C_S = 1.5$ pF ($V_{OUT} = 1$ V, $f_{AC} = 1$ MHz, BW = 1 Hz), the noise drops from 35 aF down to 0.7 aF when the automatic compensation is activated, demonstrating a sub-ppm resolution (0.5 ppm) thanks to the digital fine-tuning of the compensation path. Finally, for solution C, the activation of the dummy impedance path and the subtraction at the lock-in input ($V_{OUT} = 50$ mV due to the liquid environment,[16] $f_{AC} = 2$ MHz, BW = 1 Hz) reduces the conductance noise from 28 nS down to 2.6 nS.

In all these examples, the reduction of the signal at the input of the LIA given by the differential approach has allowed an improvement of the resolution better than an order of magnitude.

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