Eight-Channel Fully Adjustable Pulse Generator

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I. Introduction

ELECTRICAL pulse generators are commonly used in a variety of scientific fields, from mechanical automated acquisition chains [1] to material characterization [2], [3], and medical applications [4]. In most of these applications, commercial pulse generators [5]–[8] are employed because they provide good to excellent time resolution, accurate delay timing, and adjustable output amplitude. However, specific applications, like microchannel plate [9], radar [10], and telecommunications [11], have special requirements, such as high voltage output and ultrashort pulses. Thus, dedicated pulse generators [12], [13] have been developed to overcome the limitations of the commercial options.

In this range of applications, we can also find time-of-flight analysis [14] and time-correlated single-photon counting (TCSPC) measurements [15], [16], where a pulse generator is mainly used as a testing device for the electrical circuits downstream from the detector. These applications exploit repetition rates of tens of megahertz, and therefore a first requirement for the generator is to meet this frequency range. Moreover, the time resolution of the testing instrument is an important parameter, and becomes critical in emerging multichannel setups, where the best timing must be achieved not only on a single channel but also among all of them. Pulse generators available on the market have either good timing performance or multiple channels, but no existing instrument merges both features.

In this paper, we present a new modular pulse generator featuring eight fast differential, high time resolution channels, each one independently adjustable in terms of output amplitude, offset, frequency, duty cycle, and delay. Furthermore, each channel can be triggered by an external reference signal, allowing synchronization with external devices such as lasers, and can be used in burst mode. In this mode, the output turns off after sending out a specific number of pulses. More specifically, the desired target specifications are as follows:

1) a time resolution in the order of 10 ps;
2) a maximum delay greater than 1 μs (with a resolution of tens of picoseconds);
3) an adjustable output voltage between -2 and 6 V;
4) adjustable frequency from tens of kilohertz to tens of megahertz;
5) rising and falling edges in the order of nanoseconds.

To achieve all these characteristics, we exploited modularity by designing a board that completely manages two channels and by connecting four of these modules on a mainboard. Each 2-channel module (2CM) includes a field programmable gate array (FPGA), which manages all the settings, and two output chains, comprised of a frequency synthesizer, a feedback delayer block, and a fast output differential stage. The four 2CMs share an I^2C bus used by a microcontroller (placed on an additional board) to send the settings chosen through a dedicated PC software (designed in LabVIEW) to the programmable devices.

This paper is organized as follows. Section II will describe the 2CM, Section III will present the mainboard and the parameter settings, Section IV will show the experimental measurements, and finally the conclusion is drawn in Section V.

II. 2-Channel Module

The choice of parallelizing four 2CMs instead of building directly an eight-channel pulse generator has been made to maximize flexibility. A more compact board is easier to

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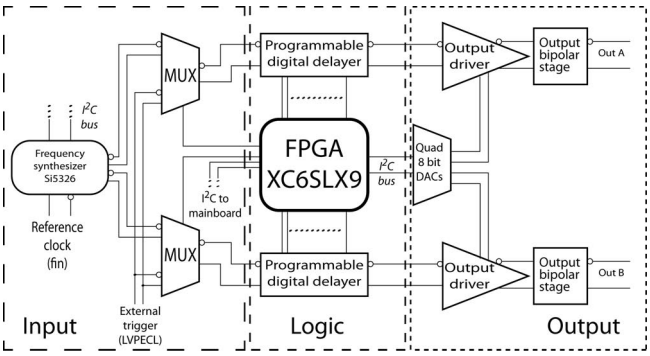

Fig. 1. Schematic of each 2CM. The input section allows the selection of the reference signal between an external trigger and an on-board generated signal. The logic section exploits an FPGA to control two digital delayers that independently set the delays and the duty cycles of the output signals. Finally, the output section provides a fast output differential signal whose amplitude and offset are set by a quad DAC.

be debugged; it allows a smarter use of the space in the case, and it opens the possibility to future expansion in terms of number of channels by juxtaposing more 2CMs. This printed circuit board has been designed by exploiting four layers and can be logically divided in three parts, all shown in Fig. 1.

The input signal can be chosen between an external trigger and the output of an on-board frequency synthesizer, the latter able to provide a low jitter signal ranging from 2 kHz to 945 MHz. In the logic section, the FPGA controls a programmable digital delayer that delays the input signal by a specific time ranging from 0 ns to 30 μs and sets the duty cycle of the output signal. The FPGA also manages amplitude and offset voltage for both channels by making use of a quad 8-bit digital-to-analog converter (DAC) device that biases the output drivers. Finally, the last differential bipolar stage is designed to provide a fast slew rate output signal when coupled with a 50-Ω output impedance.

A. Input Stage

The input signal can be chosen between an external reference and an on-board synthesized signal. As already said, this allows the flexibility to synchronize the pulse generator with a trigger coming from an external device or to choose a signal with the desired frequency. The external reference is analog processed by the mainboard and will be explained in Section III. In the 2CM, it is routed directly to a multiplexer, controlled by the FPGA, whose output is fed to the delayer loop. The other input of the multiplexer comes from the frequency synthesizer, the Si5326 from Silicon Labs [17]. This integrated circuit is able to provide two synchronous outputs frequencies (from 2 kHz to 945 MHz), each one independently adjustable by programming its internal registers ($N1$–$N3$). The relation between input and output frequencies is expressed by the following:

$$f_{\text{out}} = \frac{f_{\text{in}}}{N3} \cdot \frac{N2}{N1} \tag{1}$$

where $N3$ and $N2$ are shared between the channels, whereas $N1$ can be chosen differently for the first output frequency and the second one. To align the phase of all the channels on different 2CMs, the input clock (f_{in}) must be the same for all frequency synthesizers. Therefore, another Si5326 chip has been placed on the mainboard to provide the reference signal for the 2CM synthesizers.

B. Logic Stage

The delayer is a critical part of the system because the test of TCSPC instruments requires signals with the lowest possible jitter (in the order of 10 ps), while keeping a wide range of possible delays in both length (greater than 1 μs) and resolution (less than 100 ps). An integrated circuit with these characteristics is not commercially available. Some solutions have been presented in the literature, based on ring oscillators [18] or delay locked loops [19], but still they do not achieve the required performance in terms of timing jitter since they feature a time resolution greater than 100 ps. A third solution implemented in a complex programmable logic device (CPLD) [20] meets all of the timing specifications and is based on a high accuracy programmable desktop signal generator. The FPGA can substitute the CPLD, whereas the Si5326 chip can replace the signal generator, to create this same structure. However, the accurate and automatic adjustment of the synthesizer frequency cannot be done in the instrument (as will be explained in Section III-B). Therefore, we implemented the new architecture shown in Fig. 2(a). Its main node waveforms are shown in Fig. 2(b): after passing through a fine delayer (that adds a T_f contribution that will be explained later), the input clock (*CK*) enables a ring oscillator (*Ring1 block*) whose rising edges are counted until they reach the desired n_d value, setting in this way, the output (Q_2). A second ring oscillator (*Ring2 block*) starts together with the output rising edge, and the count of its periods determines the high time of the pulse (T_h). In particular, the *FF1* flip-flop and an AND gate enable the ring oscillator *Ring1 block* designed with a 3-ns passive delay line (CDKD3005 from ELMEC). This solution keeps the added jitter as low as possible since no digital circuits are used to implement the delay line.

The *ring_p–ring_n* differential signal is read by the FPGA and used to clock a counter (*Counter1*) that sets the data (*D2*) of the *FF2* flip-flop one cycle before the desired delay value ($n_d - 1$). When the counter reaches the n_d value, *FF2* is set, generating the rising edge of Q_2 which is the input signal of the output stage. Therefore, a T_d delay equal to $n_d \cdot T_{\text{osc1}}$ is generated (not considering the fine delayer contribution). A dedicated signal *rst1* (generated when *Counter1* reaches the value n_d) is used to reset *FF1*. It does not impact on the output signal timing performance because its only request is to be asserted before the subsequent *CK* rising edge.

Q_2 is replicated inside the FPGA by the *FF3* flip-flop and used to enable the second ring oscillator (*Ring2 block*), comprising one NAND and two inverters. Its oscillation period has been set to 2.2 ns and its rising edges are monitored by a second counter (*Counter2*). There is a small delay of about 10 ns before the oscillation actually starts, and this is due to the internal delays of the FPGA: this set time (T_{set}) is the shortest T_h of the output pulses, and therefore limits the maximum frequency of the pulse generator (50 MHz).

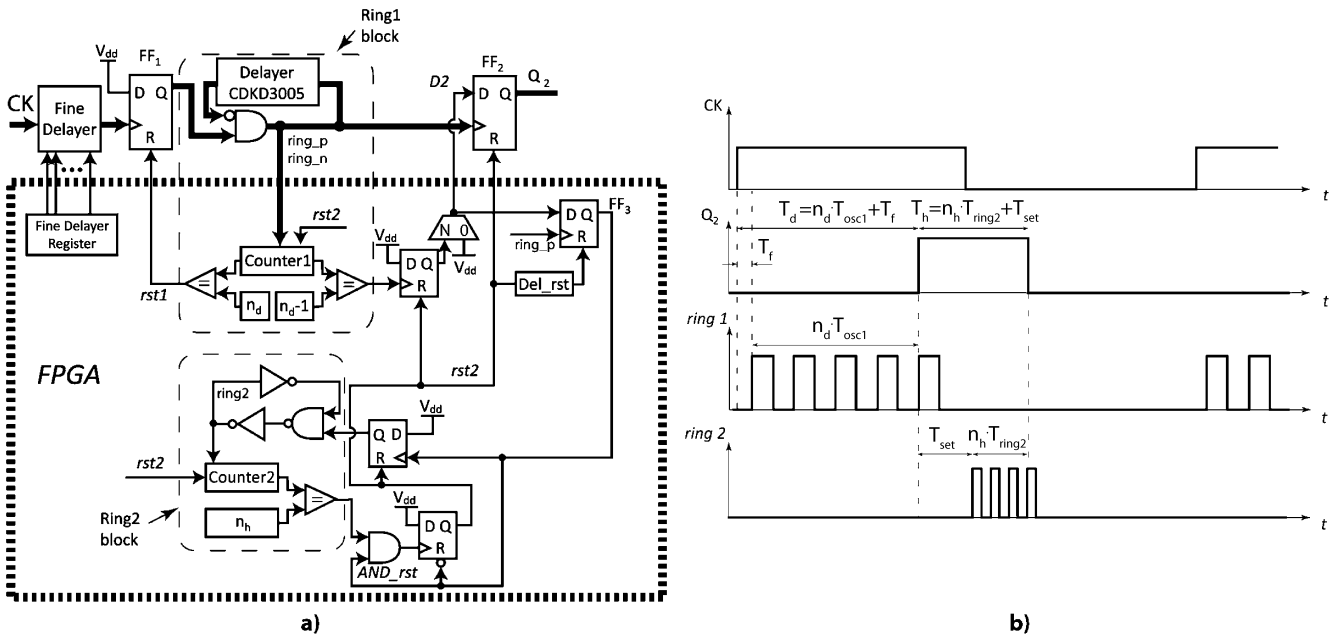

Fig. 2. (a) Physical implementation of the digital delayer. Using an external low jitter device, it is possible to reach a much higher time resolution compared with a circuit fully developed with FPGA logic. To reduce electromagnetic coupling, we exploited differential traces, shown in thick lines. (b) Waveforms of the implemented schematic block. To generate the Q_2 rising edge after n_d cycles of *ring_p*, *D2* must be set one cycle before n_d. The fine delayer adds, instead, a T_f contribution, for a total added delay of $T_d = n_d \cdot T_{\text{osc1}} + T_f$. Finally, T_h is regulated by n_h and is actually $(n_h \cdot T_{\text{ring2}}) + T_{\text{set}}$.

The *Ring2 block* eventually generates a reset signal (*rst2*) once the desired n_h value is achieved, resetting all the components, notably *FF2* that resets Q_2. Eventually, *FF3* is reset after waiting a delay *Del_rst*, to avoid glitches on *rst2*.

Fig. 2(a) shows also ancillary circuitry that implements specific cases such as 0-ns delay (done by setting the second input of the *D2* multiplexer to the high logic level) and minimum pulsewidth (generated using the AND_rst gate).

The choice of implementing the delayer loop externally from the FPGA has been made to keep the added jitter on the rising edge of the input signal as low as possible using specific low jitter components. We have chosen integrated circuits designed by Micrel: in particular, the SY10EP51 device has been used for *FF1* and *FF2*, whereas the SY10EP05 chip implements the AND gate. The falling edge instead can bear more jitter since it is not the edge of interest and this is the reason why we exploit FPGA logic to design the structure that implements the *Ring2 block* and to generate the *rst2* signal.

The minimum obtainable step is as fine as the loop time, which cannot be lower than twice the delay of the loop made by the CDKD chip and the flip-flops. This has been measured to have the accurate time of the ring oscillator period which is 7.6 ns. This step is far greater than the minimum one required to test a TCSPC instrument: indeed, the finer the delayer resolution, the better the characterization of the instruments being tested. For this reason, a fine digitally programmable delayer (SY100EP195 from Micrel) has been added upstream to the ring oscillator in the pulse generator. It adds the T_f contribution and it is programmed through the FPGA using a 10-bit parallel bus. It has a delay resolution of 10 ps and adds a jitter contribution less than 1 ps_{RMS}. With the presented architecture, the coarse delay can be generated with the loop structure and the finer regulation with the digital delayer. In this way, it is possible to generate an arbitrarily long delay, limited just by the number of bits used for n_d. Considering the maximum full-scale range of our TCSPC devices (100 ns), we set the T_d limit to 30 μs ($n_d = 12$ bits), keeping a wide margin for possible future developments. In addition, the T_h parameter, set inside the FPGA (to maximize the flexibility), has been limited to 30 μs.

C. Output Stage

The Q_2 signal is fed to the output stage. Differential stages presented in the literature achieve a slew rate lower than what is required [21], even though they exploit slew rate enhancement techniques [22], [23]. The ones that reach the required performance are single ended stages [24], hence a new stage has been designed. A first p-n-p bipolar junction transistor (BJT) differential stage $T_7 - T_8$ (BFT92 from NXP Semiconductors, acronym for Next Experience) adapts the dynamics of the *FF2* (LVPECL standard, acronym for Low Voltage Positive Emitter Coupled Logic) to the one of the output n-p-n BJT differential stage. This circuit is sketched in Fig. 3(a) and its design is crucial to obtain the desired waveform at the output. Indeed, we tuned its tail resistors to dampen ringing effects on the output signal and to adjust voltage levels to be compliant to the input dynamics of $T_1 - T_2$ transistors.

Fig. 3(b) shows the output stage $T_1 - T_2$: it has been designed to be coupled with a 50-Ω transmission line (R_L) and to work completely unbalanced. Its working principle is sketched by the red arrows. The $T_3 - T_4$ biasing transistors are independent from the input voltage V_d: they halve the $2I_{\text{OFF}}$ current, thus

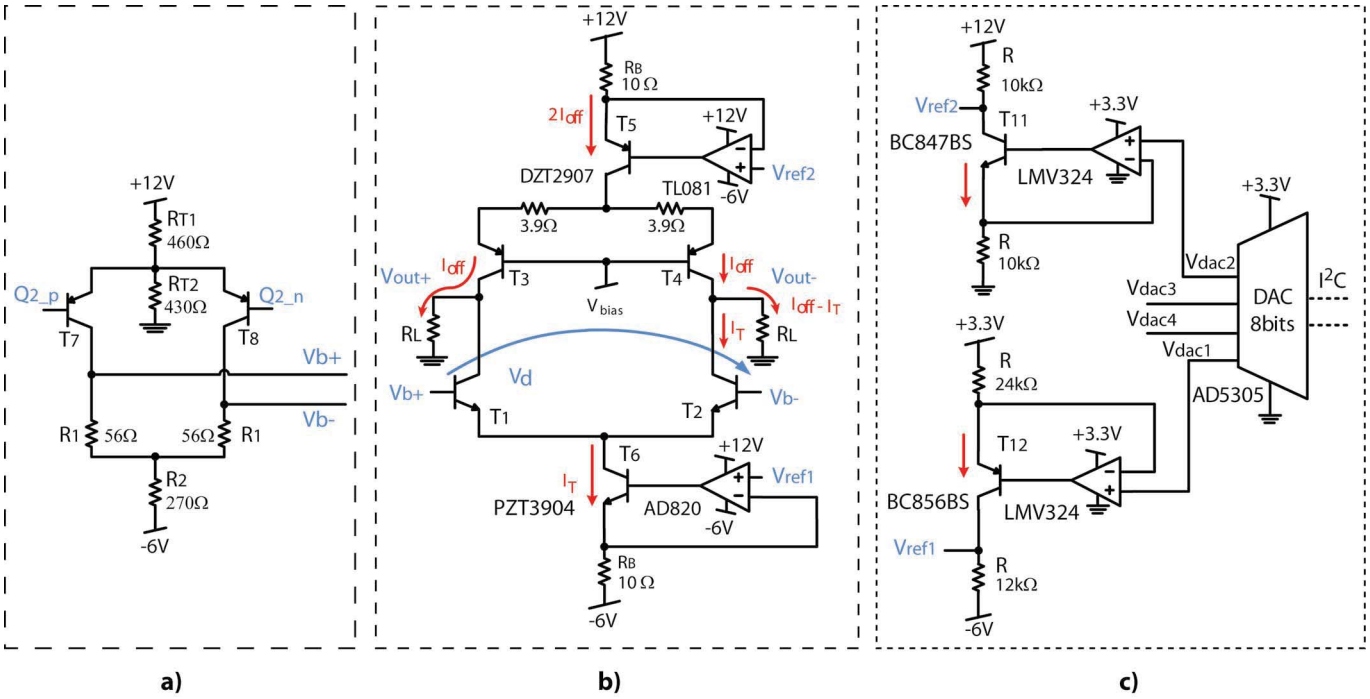

Fig. 3. Schematics of the output stage of one channel. (a) Circuit that adjusts the dynamics of the signal coming from the delay stage (LVPECL) to the one of the output differential stage. (b) Output stage with tail current generators. (c) Buffers that adapt the DAC output voltages to the dynamics of the tail generators.

pouring I_{OFF} into each branch. The $T_1 - T_2$ transistors, instead, work alternatively depending on the input voltage; a positive V_d switches T_1 OFF, and the I_{OFF} current goes into the left-hand side output node, increasing its voltage by

$$V_{\mathrm{out}+} = I_{\mathrm{OFF}} \cdot R_L. \tag{2}$$

On the contrary, the same V_d switches T_2 ON, and the right-hand side branch carries a current equal to I_T, sinking it from the output node, yielding

$$V_{\mathrm{out}-} = (I_{\mathrm{OFF}} - I_T) \cdot R_L. \tag{3}$$

Therefore, the high level of the output signal is set when I_{OFF} is completely poured into R_L, whereas the difference $I_{\mathrm{OFF}} - I_T$ defines its low level. Basically, we can say that I_{OFF} defines the offset whereas I_T sets the voltage swing.

To have an output amplitude variable from 0 to 6 V on the 50 Ω, $2I_{\mathrm{OFF}}$ has to vary from 0 A to 240 mA, so that I_{OFF} is 0 A–120 mA per branch, while I_T has to be from 0 A to 120 mA, since it flows alternatively in one of the two branches. This way, it is possible to also get a negative voltage, which is useful, for example, to generate a NIM (Nuclear Instrumentation Module) standard signal (−0.7–0 V, $2I_{\mathrm{OFF}} = 0$ A, and $I_T = 14$ mA). To achieve the best timing performance, the $T_1 - T_2$ transistors must switch as quickly as possible: a 1000 V/μs edge is chosen as the target specification, and among all the transistors we choose the BFQ591 from NXP Semiconductors, also taking into account its wide V_{CE} dynamics. For the $T_3 - T_4$ stage, we choose the p-n-p complementary type (BFQ149 from NXP Semiconductors).

Fig. 3(b) shows that the I_T and $2I_{\mathrm{OFF}}$ current generators exploit an operational amplifier and a BJT to sink or source the desired tail currents. Transistors T_5 and T_6 are not

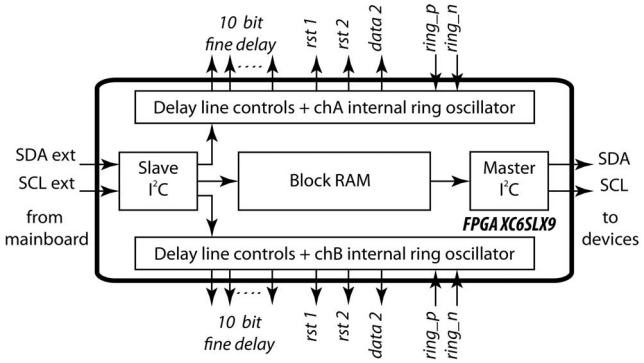

Fig. 4. Schematic block of the FPGA firmware. From the external I^2C, the FPGA receives new parameters that are saved into the block RAM or stored into registers for the delay line blocks. The last ones set the fine delays upstream the loop, and implement the schematic described in Fig. 2(a). Master I^2C reads the block RAM and programs the frequency synthesizer and the DAC described in the previous paragraph.

complementary since the former one must carry a double current compared with the latter one, and we choose, respectively, DZT2907 from diodes incorporated and PZT3904 from ON Semiconductors. Operational amplifiers are also different because different output dynamic ranges are required: indeed, AD820 (from analog devices) rails down to its negative supply, whereas TL081 (from STMicroelectronics) rails up to its positive supply. The R_B resistor value has been chosen as a tradeoff between its dissipated power and voltage resolution and is equal to 10 Ω for both generators. To be able to set the desired tail currents, the voltages V_{ref1} and V_{ref2} must be

$$0\ \mathrm{mA} \le I_T \le 120\ \mathrm{mA} \rightarrow -6\ \mathrm{V} \le V_{\mathrm{ref1}} \le -4.8\ \mathrm{V} \tag{4}$$

$$0\ \mathrm{mA} \le 2I_{\mathrm{OFF}} \le 240\ \mathrm{mA} \rightarrow +9.6\ \mathrm{V} \le V_{\mathrm{ref2}} \le +12\ \mathrm{V}. \tag{5}$$

It is possible to manage all these reference voltages using a single quad DAC followed by amplifiers. The schematics of this solution (for one channel) are shown in Fig. 3(c). The chosen DAC is the AD5305 (from analog devices): the FPGA provides four digital codes through the I^2C bus, and the DAC converts them into the four voltages $V_{\mathrm{dac}1-4}$. The subsequent operational amplifiers (LMV324 from Texas Instruments) adapt these voltages to those required by the tail current generators.

D. FPGA Management Firmware

The FPGA is the logic core of the 2CM; it must be able to receive and send commands, and to manage the two delayer loops. We choose the XC6SLX9 from Xilinx in a TQFP (Thin Quad Flat Pack) package as tradeoff between available logic resources and layout considerations. The schematic block of its firmware is depicted in Fig. 4.

Two I^2C buses are implemented on each 2CM. The first bus comes from the mainboard, is shared among all the 2CMs, is mastered by the microcontroller, and is used to send commands to the FPGAs. Each FPGA stores the data received from this bus into its internal block RAM or into dedicated registers used to manage the delay lines. The second I^2C bus instead runs on every single 2CM and is mastered by each FPGA to program the frequency synthesizer and the DAC.

As explained before, the FPGA also includes one internal ring oscillator per channel and all the logic that controls the external ring oscillator of the delayer loop (Fig. 2). Ultimately, all the additional features are handled by the FPGA, so its code must include the management of the burst mode, and the choice of the input signal.

III. Mainboard, Microcontroller, and Software

To assemble the complete eight-channel instrument, a mainboard has been designed: it mechanically supports four 2CMs, it processes the shared external trigger and the reference clock, and it allows the exchange of information between the microcontroller and the 2CMs by exploiting an I^2C bus. On an additional board, the parameters of the pulse generator are converted by the microcontroller, which in turn receives the desired settings from a remote PC through a USB connection. A LabVIEW graphical user interface (GUI) has been designed to set and control all of the adjustable parameters.

A. Mainboard

The mainboard includes eight connectors, two for each 2CM, to provide mechanical stability to the 2CMs, as well as to route all of the shared electrical signals. Among these, two differential lines carry the external trigger and the reference clock. The latter is given by another Si5326 frequency synthesizer whose output is split by a 1:4 LVPECL fanout buffer (SY89831 from Micrel). The external trigger (*trig in*), instead, is processed by the circuit shown in Fig. 5. This structure allows the pulse generator to receive both NIM-like signals (negative amplitude, sensitive on the falling edge) and TTL-like signals (positive amplitude, sensitive on the rising edge). The input resistor network is necessary to adapt the external trigger to the comparator input dynamic range. Through the use of a digital potentiometer (controlled via the I^2C bus), the threshold value of both comparators can be set by the microcontroller. Eventually, a multiplexer is used to choose which of these signals passes to a second 1:4 LVPECL SY89831 buffer and then to the 2CMs.

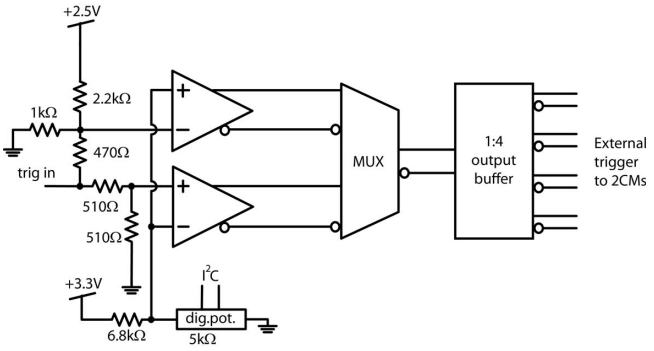

Fig. 5. Schematic block of the external trigger conditioning circuits. After the 50-Ω terminator resistor, the trigger is split and processed in parallel by two comparators. One is sensitive to the falling edge of the signal *trig in* (compliant with a NIM-like signal), whereas the other one is sensitive to the rising edge (TTL-like). A subsequent differential multiplexer routes the chosen signal to the four boards through a 1:4 differential buffer.

In addition to the signal processing and transfer, the mainboard also routes the power supply for all the boards. The instrument has a single supply input, powered by any electrical socket, which is reduced to 13.2 and 5 V by two ac/dc converters and has a maximum power consumption of 50 W.

B. Microcontroller and Firmware

The microcontroller is the core that translates the data coming from the PC into the correct values to be sent to the programmable device registers. A PIC24FJ64GA006 from microchip has been chosen due to its internal I^2C and SPI (Serial Peripheral Interface) blocks. As mentioned above, to communicate with the four FPGAs, the digital potentiometer and the frequency synthesizer on the mainboard the I^2C is used. Instead, the SPI bus carries the data coming from a FT232 device, which is a USB-to-UART (Universal Asynchronous Receiver-Transmitter) integrated circuit from FTDI (Future Technology Devices International).

The microcontroller firmware works strictly together with the GUI and the FPGA code. When a single or more parameters are set in the PC software, all of them are transferred to the microcontroller. Then, the microcontroller finds out which of the settings have been modified, converts them into the right codes required by the target device (FPGA, Si5326, DAC, ...), and saves them in its RAM. Finally, it sends a specific memory block to each device to configure it into the new state.

Most of the parameters require just a conversion from the physical quantity shown in the GUI to the digital number necessary to the programmable devices, but the frequency synthesis is worth of a more in-depth discussion. Silicon Labs provides a free software (DSPLLsim) that generates

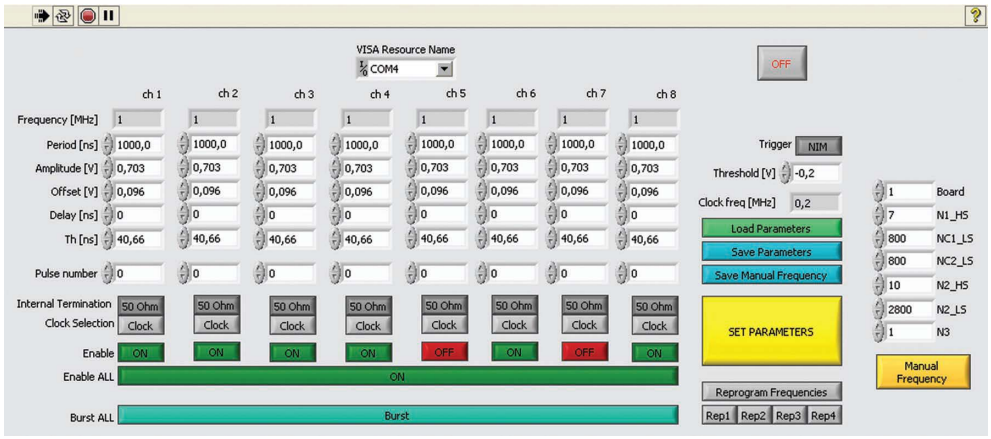

Fig. 6. Pulse generator GUI designed in LabVIEW. It shows the current settings and allows the independent modification of each parameter without affecting the others. Current settings can also be saved in a file and reloaded. On the right-hand side, a section called manual frequency allows the manual selection of the parameters of each synthesizer giving more flexibility to the system. This section must be used together with the DSPLLsim from Silicon Labs.

TABLE I
MAXIMUM RATINGS OF THE PULSE GENERATOR.

Parameter	Minimum	Maximum	Step
Period	20 ns	500000 ns	2.5 ns
Amplitude	-2 V	6 V	16 mV
Offset	0 V	6 V	32 mV
Delay	0 ps	30 µs	10 ps
T_h	10 ns	30 µs ($T_h + Delay < Period$)	2.2 ns
Burst #	0 (continuous)	2^{48}	1
Ext. trigger Threshold	0 V	1.2 V	5.5 mV

the best combination of parameters $N1$–$N3$ in terms of output jitter and frequency accuracy based on the input frequency and the desired output ones. Unfortunately, it is not possible to use this code inside the microcontroller, thus a simplification has been made. By fixing the main synthesizer frequency to 200 kHz and the oscillation frequency of the 2CM synthesizers to 5.6 GHz, we have been able to get all of the desired periods with a step of 2.5 ns. This sets a limitation on the available synthesizable frequencies, but this range can be further extended using a section of the GUI dedicated to the manual data entry of the parameters $N1$–obtained from the DSPLLsim. When using this section, the parameter conversion in the microcontroller is skipped, whereas a specific function that sends the GUI numbers directly into the registers of the Si5326 is started. All five phase-locked loops (four on the 2CMs and one on the mainboard) can be programmed this way, leading to the largest possibility of adjustment in terms of frequencies.

C. Graphical User Interface

The GUI has been programmed in LabVIEW, and the front panel is shown in Fig. 6.

With this GUI, all of the previously explained parameters can be independently modified. The software provides a user-friendly interface that shows the system actual settings and sends the new desired values to the microcontroller. The ranges the pulse generator can reach are summarized in Table I as well as their quantization steps. In particular, the period step has been limited to 2.5 ns to decrease the calculation complexity and improve the accuracy of the output frequency. The amplitude and offset circuits instead, employ the same DAC but have different conversion stages so the same LSB results in a different voltage resolution. The limitation on the delay line is due to the fine delayer SY100EP195, whereas T_h step depends on the period of the *Ring2 block*. Finally, the limitation to the external trigger threshold is due to the LSB of the digital potentiometer (refer to Fig. 5 to convert the latter one to actual thresholds of NIM- and TTL-like signals).

In addition to the settings already discussed, it is possible to choose the standard of the expected external reference and its threshold voltage, the clock selection between the trigger and the internal clock generated on the 2CMs, and the selection of internal 50-Ω termination. Moreover, it is possible to disable the channels that are not used in the measurement and also to save current data in a text file and to reload it when necessary.

IV. EXPERIMENTAL RESULTS

The experimental measurements have been carried out to test the effective performance of the pulse generator, particularly in terms of output voltage waveforms, time resolution, and delay linearity of the different channels.

A. Output Waveforms

The output voltage waveforms are shown in Fig. 7. The steepness of the edge affects the settling time of the output: the steeper the edge, the larger the output overshoot and the more asymmetric the differential voltages. Actual reasons for this effect have not been found yet, since many factors are concurrent. The main hypothesis is related to a nonperfectly symmetric behavior of the two BJTs of the adapting

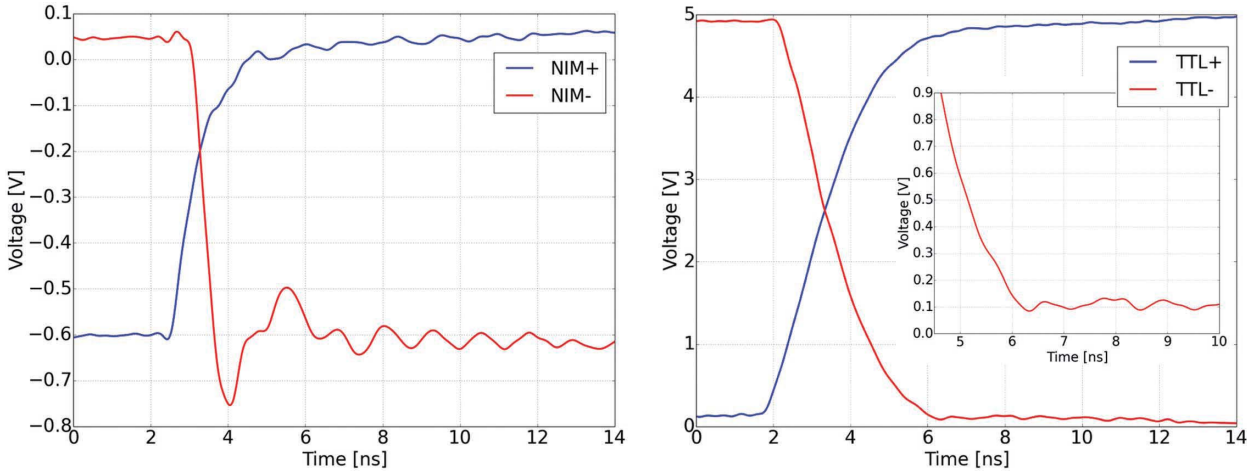

Fig. 7. Output waveforms of the differential pulse. (a) NIM standard. (b) TTL standard. Left: small (20%) overshoot, but the very steep edge improves time resolution. Right: instead, has a 10%–90% rising time of about 2.5 ns and shows no overshoot, as illustrated in the magnified subplot (same scale as the left-hand side figure).

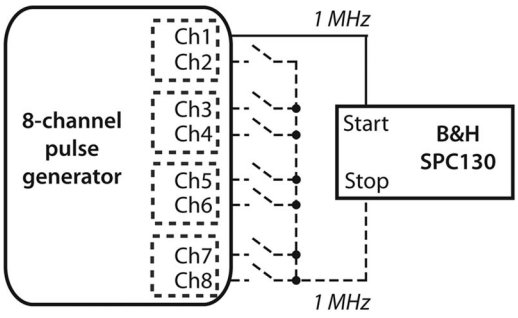

Fig. 8. Measurement setup for the time resolution. Channel 1 has been used as the *start* reference (at 1 MHz) for every measurement, whereas for *stop* we selectively used one of the other channels (at 1 MHz). Since the range of the SPC-130 is 50 ns, for longer delays both *start* and *stop* signals have been delayed, in particular, the *stop* one has been kept 20 ns after the *start* one.

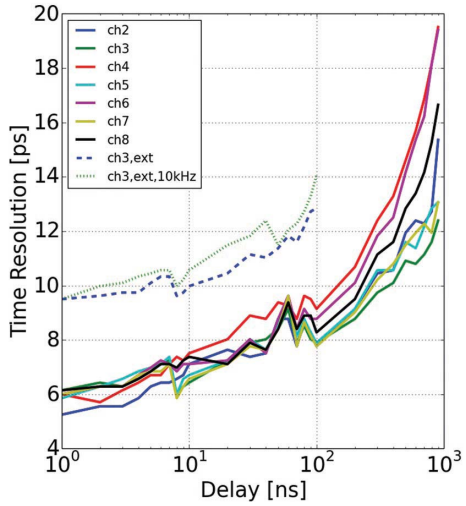

Fig. 9. Time resolution of the pulse generator that increases (i.e., worsens) with the delay. Note that the SPC-130 contribution of 6.3 ps has been deconvolved on this plot. The last two plots require a different setup so measurements have been taken over the range of possible setting in the setup.

stage $T_7 - T_8$, in Fig. 3(a). Indeed, parasitic capacitance may have different impacts when the base current is sourced or sunk by the transistor, leading to the small overshoot in fast-edges signal. Anyhow, even if this effect is as wide as the 20% of the swing, it is not enough to fail a TCSPC measurement, so in our case, it is possible to deal with it. On the other hand, the steep edge (less than 1 ns and 1600 V/μs) improves the timing performance since it reduces the timing jitter, which is a great advantage for testing TCSPC instruments.

B. Time Resolution

To use the pulse generator to evaluate the performance of a TCSPC instrument, it is mandatory to have a low jitter between the channels. This has been evaluated through a state-of-the-art TCSPC system (SPC-130 from Becker and Hickl, used in single acquisition mode [20]) by sending two outputs of the pulse generator to its *start* and *stop* inputs, and using them to measure the time resolution between different channels of the pulse generator. Fig. 8 shows the setup used for this measurement.

Channel 1 has been chosen to be always the *start* signal whereas the others have alternatively been the *stop* one. These measurements have been repeated several times for each channel, changing the delay of the *stop* signal, from the minimum (0 ns with zero loops of the ring oscillator delayer) to 1 μs (limited by the chosen frequency of 1 MHz) to evaluate the jitter introduced by the loop.

Since an increasing curve has been obtained for every channel (Fig. 9, ch2–ch8 curves), we can assert that the feedback delayer introduces a timing jitter dependent on the number of loops of the ring oscillator. On the other hand, time resolutions between different channels are quite similar, starting around 6 ps and increasing to a worst case of only 20 ps for a 900-ns delay. This is a great achievement especially considering that the channels are on different boards, where the reference signal are generated by different synthesizers.

The dashed curve in Fig. 9 shows the time resolution between an external pulse generator (Philips PM5786B) and Channel 3. This measurement requires a different setup, shown in Fig. 10, and this limits the maximum delay to 100 ns.

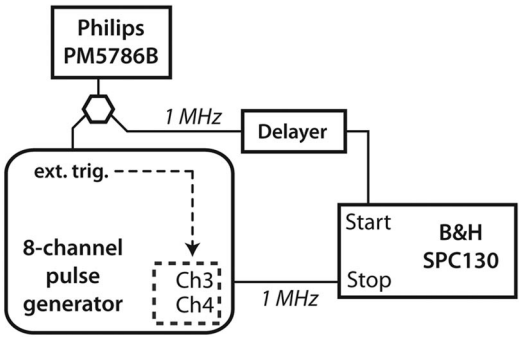

Fig. 10. Setup involving the external pulse generator. The external delayer has a maximum delay of 64 ns, thus the two measurements performed with this setup stop at 100 ns.

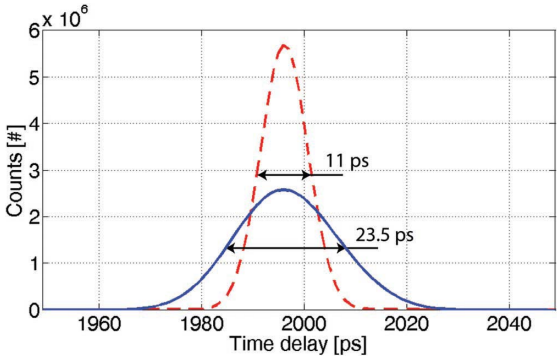

Fig. 11. Histogram of a resolution measurement that exploits time-tagging mode (the SPC-130 resolution has not been deconvolved here). Even at 1 MHz, this key parameter worsens from 11 ps when the delay is 0 ns (red dashed line) to 23.5 ps when the delay is 500 ns (blue solid line).

The worsening of this time resolution compared with the previous one in Fig. 9 is due to the contribution of the external trigger acquisition chain (Fig. 5). Even if slightly worse, the time resolution remains remarkable in this case as in the other ones, worsening by just 3 ps.

The last measurement (green dotted line) in the plot still exploits the last setup, but the frequency of the external trigger is 10 kHz. The time resolution is marginally worse, thus it may be mistakenly ascribed to the poorer stability of the pulse generator at low frequencies, but a deep investigation shows a different reason. We ran two longer (a few minutes) measurements at 1 MHz exploiting the time-tagging feature [26] of the Becker and Hickl SPC-130 (*start* is Channel 1 and *stop* is Channel 2), one with 0-ns delay and one with 500 ns on both *start* and *stop* signals, and we report the result in Fig. 11.

The first measurement (red dashed line) is coherent with the time resolution measured in single acquisition mode whereas the second one (blue solid line) shows a worsening of the figure of merit. This clarifies that the poorer performance is not related to the lower frequency, but to other issues. Temperature sensitivity is the most probable cause, most likely in one of the components of the delayer loop. To better investigate this problem, longer measurements have been run. The employed setup is the one depicted in Fig. 8, but using a 10-kHz frequency. This choice is a tradeoff between the length of the measurement (80 min) and the amount of generated data (almost 1 GB). In addition, for this measurement, the time-tagging feature of the SPC-130 board has been exploited and

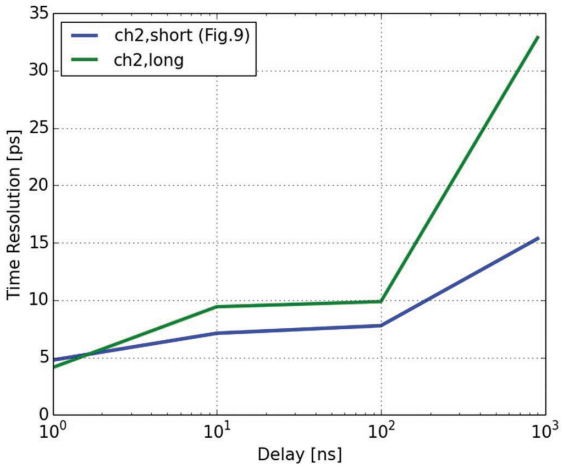

Fig. 12. Comparison between the time resolutions obtained for short (a few seconds) and long measurement times (80 min). The reported results have been acquired with Channel 1 as the *start* and Channel 2 as the *stop*. Results for the other channels are similar.

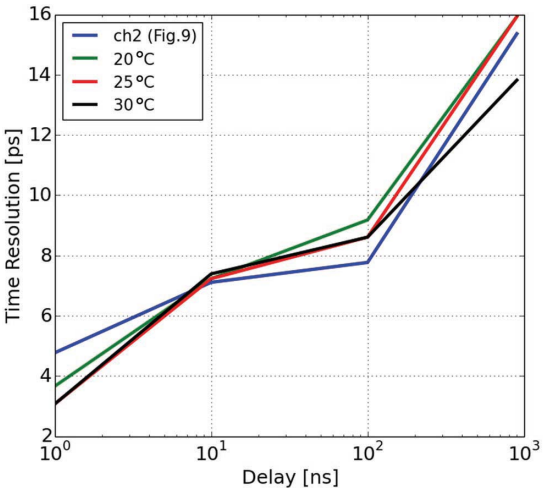

Fig. 13. Comparison among the time resolutions obtained at different room temperatures. The blue curve is used as a reference with the previous measurement.

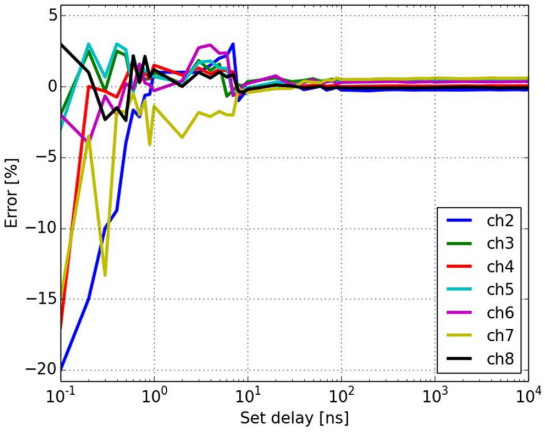

Fig. 14. Percentage of the error introduced by the delayer loop.

Fig. 12 shows the obtained results. The blue line reports the data already shown in Fig. 9 (acquired for a few seconds), whereas the green one represents the long measurement. As can be noticed for short time delays, the differences in the

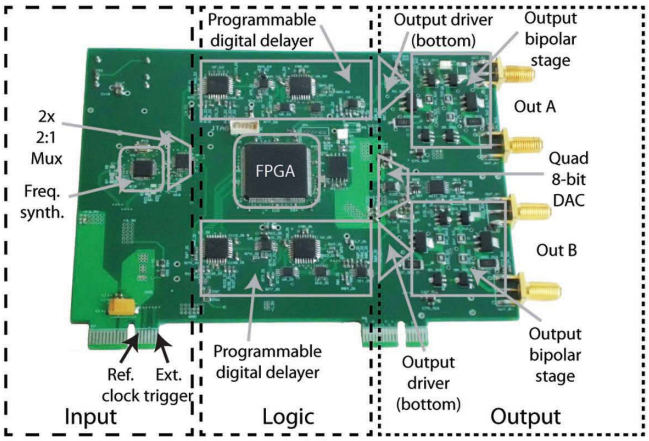

Fig. 15. (a) 2CM board with localization of the different blocks. The output drivers are placed on the bottom side of the board and are not visible in this picture. (b) Picture of the pulse generator described in this paper. It shows 17 SMA (Sub-Miniature A) connectors, one for the external trigger and eight pairs for the outputs.

time resolutions are limited because variations in the period of the external ring oscillators are negligible. Indeed, these delays are obtained with a small number of loops of the delayer *Ring1 block*. For long delays instead, temperature drift affects the oscillation period thus worsening the performance.

Anyhow, the main problem does not concern the absolute temperature of the environment, but its variations. Indeed, constant temperature measurements have been carried out, and the outcome is reported in Fig. 13. The pulse generator has been placed in a temperature-controlled atmosphere room and the time resolution has been measured at 20 °C, 25 °C, and 30 °C (which is the expected temperature range in a laboratory room) for a short measurement time. The differences among the time resolutions at different temperatures are lower than 2 ps and this proves that the absolute temperature does not affect the obtainable time resolution.

For the three different temperatures, the peak positions have also been saved. They have no drift for 0-ns delay, whereas for 900 ns their shift is equal to 80 ps moving from 20 °C to 30 °C. This agrees with the previous hypothesis, and this further proves that a temperature variation during a measurement influences the time resolution of the instrument.

All measurements have been carried out with a 5-W fan placed into the case of the pulse generator. This helps in decreasing the temperature impact on the performance, although differences in temperatures remains among different boards and in different places on each board.

C. Linearity

The linearity of the designed pulse generator has also been evaluated, in particular, the accuracy of the delay introduced by the delayer loop. Fig. 14 shows the percentage of the error between the set delay and the measured one. It has been evaluated using Channel 1 as the reference for all the other channels. As can be noticed, the error is limited to 1%–20% for delays less than 10 ns, whereas it decreases to 0.3% for longer ones. This effect is due to the implemented architecture: the small delays (less than 7.6 ns) are generated using only the SY100EP195 delayer chip. The delay introduced by this device is directly affected by the chip temperature, thus fluctuations among the boards lead to differences among the channels. However, for very small delays, the error on the selected value is comparable with the jitter of the instrument.

V. Conclusion

In this paper, we presented a pulse generator with eight independent and fully adjustable differential channels. We exploited modularity by developing a 2CM, four of which have been installed on a mainboard. Each 2CM includes an FPGA that manages all of the circuit parameters, each one adjustable via a PC software. A microcontroller placed on a dedicated board is the core that converts the physical quantities set on the software to the codes needed by the programmable devices. In Fig. 15(a), a picture of the 2CM is presented, with highlights on the main blocks (refer to Fig. 1 and Section II). The instrument is completely encased in a $324 \times 268 \times 147$ mm^3 box, as shown in Fig. 15(b), and the required power (50 W) is supplied by a single 110–220 V plug.

The performance of the pulse generator is remarkable in terms of time resolution (6 ps), whereas it presents a small overshoot on falling edges of fast-edge pulses (20% on a 1-ns edge). Since its main focus is the test of new multichannel TCSPC systems, this issue can be overcome by placing an input threshold lower than the ringing amplitude. The timing performance has been studied with care and the lowest possible jitter has been achieved by using specific low jitter devices, differential lines, and fast output transistors.

References

[1] T. Ohmae, T. Matsuda, K. Kamiyama, and M. Tachikawa, "A microprocessor-controlled high-accuracy wide-range speed regulator for motor drives," *IEEE Trans. Ind. Electron.*, vol. IE-29, no. 3, pp. 207–211, Aug. 1982.

[2] T. Korn, F. Müller, D. Grundler, and C. Schüller, "Characterization of Permalloy films on high-bandwidth striplines," *J. Magn. Magn. Mater.*, vols. 272–276, no. 6, pp. E1341–E1342, May 2004.

[3] A. Dichiara, "*In situ* diagnostics for the study of carbon nanotubegrowth mechanism by oating catalyst chemical vapor deposition for advanced composite applications," Ph.D. dissertation, Dept. Eng. Mater. Sci., École Centrale Paris, Paris, France, Nov. 2012.

[4] K. T. Moesta *et al.*, "Protoporphyrin IX occurs naturally in colorectal cancers and their metastases," *Cancer Res.*, vol. 61, no. 3, pp. 991–999, Feb. 2001.

[5] Berkley Nucleonics. *Electro Optic Benchtop Pulse Generator*. [Online]. Available: http://www.berkeleynucleonics.com/resources/6040_datasheet.pdf, accessed 2014.

[6] Quantum Composers. (2012). *9520 Series Digital Delay Pulse Generator*. [Online]. Available: http://quantumcomposers.com/support/support-down/item/9520-datasheet

[7] Stanford Research System. *DG535 Digital Delay/Pulse Generator*. [Online]. Available: http://www.thinksrs.com/downloads/PDFs/Catalog/DG535c.pdf, accessed 2014.

[8] Agilent Technology. (2013). *81180B Arbitrary Waveform Generator*. [Online]. Available: http://cp.literature.agilent.com/litweb/pdf/5991-0364EN.pdf

[9] D. J. Bradley, J. F. Higgins, and M. H. Key, "Nanosecond gating of AN image intensifier capable of triggered picosecond photography," *Appl. Phys. Lett.*, vol. 16, no. 2, pp. 53–55, Jan. 1970.

[10] D. J. Daniels, "Surface penetrating radar," *Electron. Commun. Eng.*, vol. 8, no. 4, pp. 165–182, Aug. 1996.

[11] M. Z. Win and R. A. Scholtz, "Impulse radio: How it works," *IEEE Commun. Lett.*, vol. 2, no. 2, pp. 36–38, Feb. 1998.

[12] T. Xia, A. S. Venkatachalam, and D. Huston, "A high-performance low-ringing ultrawideband monocycle pulse generator," *IEEE Trans. Instrum. Meas.*, vol. 61, no. 1, pp. 261–266, Jan. 2012.

[13] V. N. Rai and M. Shukla, "A high-voltage pulser circuit with sub-nanosecond rise time," *Rev. Sci. Instrum.*, vol. 65, no. 6, pp. 2134–2136, Jun. 1994.

[14] A. Kilpelä and J. Kostamovaara, "Laser pulser for a time-of-flight laser radar," *Rev. Sci. Instrum.*, vol. 68, no. 6, pp. 2253–2258, Jun. 1997.

[15] F. Villa *et al.*, "SPAD smart pixel for time-of-flight and time-correlated single-photon counting measurements," *IEEE Photon. J.*, vol. 4, no. 3, pp. 795–804, Jun. 2012.

[16] S. Antonioli, M. Crotti, A. Cuccato, I. Rech, and M. Ghioni, "Time-correlated single-photon counting system based on a monolithic time-to-amplitude converter," *J. Modern Opt.*, vol. 59, no. 17, pp. 1512–1524, Oct. 2012.

[17] Silicon Labs. (2010). *Any Frequency Precision Clock Multiplier Jitter Attenuator*. [Online]. Available: https://www.silabs.com/Support%20Documents/TechnicalDocs/Si5326.pdf

[18] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1273–1282, Dec. 1993.

[19] J. Christiansen, "An integrated high resolution CMOS timing generator based on an array of delay locked loops," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 952–957, Jul. 1996.

[20] J. Kalisz, A. Poniecki, and K. Różyc, "A simple, precise, and low jitter delay/gate generator," *Rev. Sci. Instrum.*, vol. 74, no. 7, pp. 3507–3509, Jul. 2003.

[21] J. Ramirez-Angulo, R. G. Carvajal, and A. Lopez-Martin, "High slew rate two stage A/AB and AB/AB op-amps with phase lead compensation at output node and local common mode feedback," in *Proc. IEEE ISCAS*, May 2008, pp. 288–291.

[22] I. Grech, J. Micallef, and T. Vladimirova, "Low voltage, high speed fully differential CMOS op amp," in *Proc. 7th IEEE ICECS*, vol. 1. Dec. 2000, pp. 7–10.

[23] B. H. Kassiri and M. J. Deen, "Slew-rate enhancement for a single-ended low-power two-stage amplifier," in *Proc. IEEE ISCAS*, May 2013, pp. 1829–1832.

[24] N. Charalampidis, K. Hayatleh, B. L. Hart, and F. J. Lidgey, "A wide bandwidth voltage-follower with low distortion and high slew rate," in *Proc. 13th IEEE ICECS*, Dec. 2006, pp. 256–259.

[25] Becker & Hickl Gmbh. (2010). *SPC 130 Time Correlated Single Photon Counting Module*. [Online]. Available: http://www.becker-hickl.de/pdf/dbspc130-2.pdf

[26] W. Becker. (2008). *The bh TCSPC Handbook (3rd ed.)*. [Online]. Available: http://www.boselec.com/products/documents/BHTCSPCHandbook8-21-07LTR2.pdf