A 2-GHz Bandwidth, Integrated Transimpedance Amplifier for Single-Photon Timing Applications

Matteo Crotti, Ivan Rech, *Member, IEEE*, Giulia Acconcia, Angelo Gulinatti, *Member, IEEE*, and Massimo Ghioni, *Senior Member, IEEE*

I. Introduction

NOWADAYS, the applications exploiting photon timing techniques, such as time-correlated single-photon counting (TCSPC) [1] and time-of-flight measurements [2], require the development of systems characterized by several parallel single-photon detectors, followed by multichannel acquisition chains. Because of the simultaneous acquisition of different light signals, these innovative multidimensional systems enable higher maximum count rates and shorter measurement times, thus providing a better performing instrumentation that will, in turn, widen the spectrum of potential applications.

However, the development of multipixel detectors and of multichannel electronics for TCSPC systems is still underway. Currently, systems having a large number of channels exhibit a poor performance compared with single channel ones, highlighting a clear tradeoff between the performance and channel counts. Concerning the detector, different solutions were proposed in the past, being based on multianode photo multiplier tubes [3], which exhibit some intrinsic drawbacks [bulky and fragile structure, high power dissipation, low photon detection efficiency (PDE), and sensibility to electromagnetic disturbances] and on single-photon avalanche diode (SPAD) arrays fabricated using standard CMOS technologies [4], [5]. Deep submicrometer (DSM) CMOS technologies are mandatory for the fabrication of dense SPAD arrays with large numbers of pixels, adequate fill factor (i.e., the active-to-total area ratio of a single pixel), and smart pixels, which include the integrated counting/timing electronics. However, a challenging basic issue must be faced: the inherent features of DSM CMOS technologies, namely, the relentless trend toward higher doping levels, lower thermal budget, and thinner p- and n-well layers, conflict with SPAD detector performance. The smaller depth of carrier-collection layers limits the PDE, and the high electric fields arising from higher doping result in strongly enhanced dark count rate (DCR) due to band-to-band and trap-assisted tunneling effects.

As an alternative, SPAD arrays fabricated with custom silicon technologies were introduced in the past few years [6]. These arrays provide a better PDE and a lower DCR compared with CMOS ones, although their maximum pixel number is limited to less than 100. Due to the electrical crosstalk between the adjacent pixels, the incorporation of high-performance photon timing capabilities into custom SPAD arrays is a challenging task even with small numbers of pixels. Fast and large voltage transients ($\approx$1 V/ns) generated by the active quenching circuits (AQCs) cause electrical disturbances on nearby pixels, which preclude low avalanche-sensing thresholds, resulting in poor timing performance [7].

The AC coupled pick-up circuit [7] that has been successfully used in single-detector systems to obtain a low timing jitter cannot be exploited in multi-SPAD arrays. The switching noise of adjacent pixels would be coupled to the current pick-up circuits through both on-chip and on-board paths, thus preventing the detection threshold to be lowered
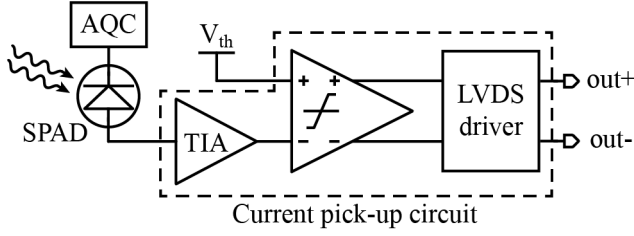
Fig. 1. Block diagram of the complete SPAD pixel, including the designed avalanche current pick-up circuit. AQC: active quenching circuit. TIA: transimpedance amplifier. LVDS: low-voltage differential signaling.

below 100 mV. On the other hand, the integrated MOS structure [8], [9] used in multidetector systems leads to worse time resolution, higher power dissipation, and lower fill factor of the detectors.

Hence, there is the necessity to develop a new avalanche detection circuit, to fully exploit the features of custom SPADs and their advantages over CMOS detectors and to open the way to the development of larger arrays.

We have successfully demonstrated [10] the possibility to obtain a good performance, in terms of time resolution and crosstalk, using a transimpedance amplifier (TIA) based on a single n-p-n bipolar junction transistor to detect the SPAD avalanche current. From the measurement results, it has been noticed the possibility to obtain a state-of-the-art time resolution [34-ps full-width at half-maximum (FWHM)] designing a transimpedance stage characterized by a bandwidth larger than the avalanche current one (about 1 GHz), so that the anode-substrate SPAD capacitance is not charged, no current flows through the detector parasitic capacitance and the entire current is read by the pick-up circuit. Moreover, the introduction of a simple *RC* low-pass filter, with a 600-MHz pole, after the current pick-up circuit, has made the crosstalk between different pixels negligible.

The good results achieved with the discrete component structure have sketched the guidelines for the design of a fully integrated TIA for multipixel photon timing applications. To fit the specifics of these applications, the circuit should present a bandwidth larger than 1 GHz to obtain a good temporal resolution, low crosstalk between the channels and as small as possible silicon area and dissipated power, to be able to implement a large array of read-out circuits.

This paper is organized as follows. In Section II, the SPAD current read-out circuit is described and its main features are presented. In Section III, the results obtained with the designed pick-up circuit are shown. Finally, the conclusion is drawn in Section IV.

II. READ-OUT CIRCUIT STRUCTURE

A block diagram of a complete pixel for photon timing applications, including a simplified schematic of the designed read-out circuit, is shown in Fig. 1. The avalanche current pick-up circuit is based on a TIA connected to the SPAD anode terminal, whereas the AQC [11] is connected to the SPAD cathode side. The pick-up circuit output voltage is compared with a threshold voltage (V_{th}) by the subsequent comparator, to detect the avalanche current and keep the
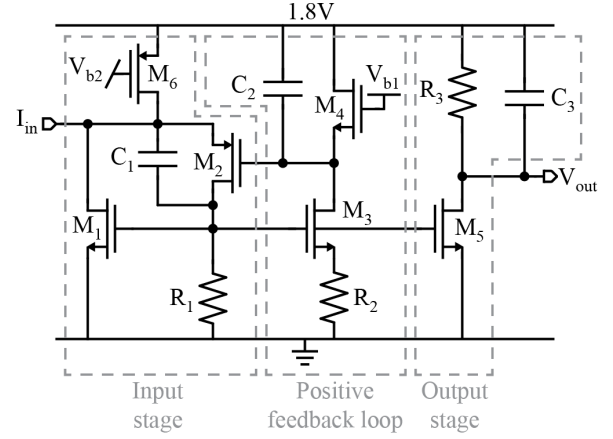

Fig. 2. Schematic of the designed TIA.

TABLE I
DIMENSIONS OF THE TIA DEVICES

M_1	$40\mu m/0.18\mu m$	R_1	9.7kΩ
M_2	$20\mu m/0.18\mu m$	R_2	5kΩ
M_3	$20\mu m/0.18\mu m$	R_3	2.04 kΩ
M_4	$40\mu m/0.18\mu m$	C_1	70fF
M_5	$5.5\mu m/0.18\mu m$	C_2	1.5pF
M_6	$95\mu m/0.18\mu m$	C_3	135fF

photon arrival time information. To deeply characterize the circuit, the threshold voltage can be externally adjusted, whereas in future implementations, it will be internally generated, to reduce the overall number of pads and hence the circuit area. Finally, a low-voltage differential signaling (LVDS) driver routes the photon detection information out of the integrated circuit to the following electronics, typically a time-to-amplitude converter or a time-to-digital converter, which measures the photon arrival time.

As shown, the single pixel includes also the AQC. To include all the electronics in a single chip, the pick-up circuit has been developed in a 0.18-μm high voltage (HV) CMOS technology, suitable to implement also the quenching circuit. The technology, more than the possibility to use HV transistors, necessary only for the AQC implementation, offers also low-voltage isolated transistors, because of a triple well process. This feature allows the implementation on a single die both of the AQC and the pick-up circuit, even if the two circuits operates on the two different SPAD sides, separated by several tens of volts.

A. Transimpedance Amplifier

The complete schematic of the designed transimpedance stage and the device dimensions is shown in Fig. 2 and Table I, respectively. The circuit can be divided into three main blocks: an input stage, a positive feedback loop, and a final output stage.

The input stage consists of transistors M_1 and M_2 and of the resistance R_1 (a MOSFET working in the triode region) and implements a current amplifier with an active shunt feedback [12]. If only this part of the circuit were considered, the bandwidth would be limited to less than 1 GHz by the p-MOS transistor M_2; to overcome this problem, the capacitance C_1 has been added to the circuit. The capacitance implements a feedforward compensation [13] and enlarges the stage bandwidth to more than 2 GHz. At high frequencies, above the singularities introduced by C_1, the feedback loop is closed by the capacitance; M_1 works in transdiode configuration and the TIA functionality is preserved.

This structure, because of its ease and to the low number of parasitic capacitances, may achieve the required bandwidth, but the input impedance would be too high to keep the anode voltage constant when a photon triggers the SPAD avalanche.

Considering only this part of the circuit, the input impedance, at low and medium frequencies, when the feedback-loop gain is much larger than 1, would be equal to

$$R_{\text{in}} = \frac{1/g_{m,2}}{1 + g_{m,1} \cdot R_1} \cong \frac{1}{g_{m,2} \cdot g_{m,1} \cdot R_1} \tag{1}$$

where $g_{m,1}$ and $g_{m,2}$ are the transconductances of M_1 and M_2, respectively. To obtain low input impedance, the resistance R_1 should be maximized, but in this way, the bandwidth of the stage would decrease, because the parasitic pole connected to the gate node of MOSFET M_1 would be moved to lower frequencies. Moreover, the biasing current of the stage has to be minimized to keep the dissipated power low, and the transconductances of the MOSFETs cannot be increased without increasing the MOSFET dimensions and influencing the stage bandwidth.

The circuit biasing current has been chosen to keep low power dissipation and to keep all the MOSFETs in the strong inversion regime, to maximize the transistor cutoff frequencies. To this aim, the biasing current of the first stage has been chosen to 250 μA, and the other two circuit branches are biased with a 50-μA current each, so that the total current flowing in the TIA is equal to 350 μA, corresponding to a dissipated power of 630 μW.

To reduce the input impedance, a second feedback loop, consisting of M_3, M_4, and R_2, has been added. The second loop has a positive feedback, with a loop gain lower than one to ensure stability. Without this part of the circuit, if the gate voltage of M_2 were fixed, the input voltage would rise when the input current rises; the second feedback loop lowers the gate voltage of M_2 when the input current rises, keeping the input voltage constant.

Hence, the employment of the second feedback loop allows overcoming the tradeoff between the input impedance and the bandwidth. With the chosen structure, the low-frequency input impedance is equal to

$$R_{\text{in}} = \frac{1/g_{m,2}}{1 + g_{m,1} \cdot R_1} \cdot \left(1 - \frac{g_{m,3} \cdot 1/g_{m,4}}{1 + g_{m,3} \cdot R_2} \cdot g_{m,2} \cdot R_1\right). \tag{2}$$

The impedance, compared with the input impedance reported in (1), is reduced by the factor between brackets,
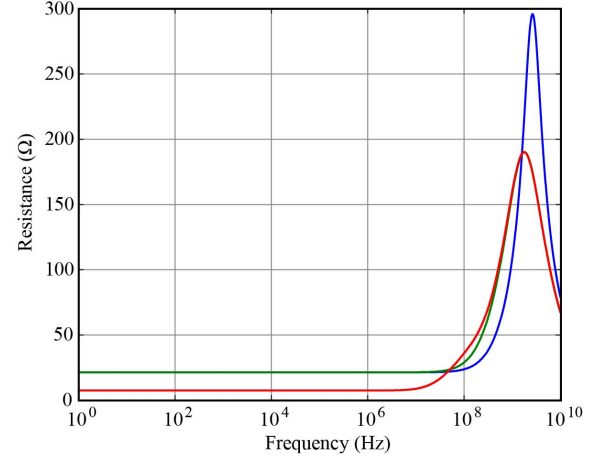

Fig. 3. Input impedance of the designed TIA. Blue curve—input impedance without the feedforward compensation and without the positive feedback loop. Green curve—input impedance when adding the capacitance C_1. Red curve—complete circuit.

equal to 1 minus, the second loop gain. Therefore, it is possible to reduce the low and medium frequency impedances having a loop gain as close as possible to 1. The maximum loop gain is limited by the necessity of having a stable operation in all possible conditions. Due to the mismatches and the process parameter variations, the low-frequency gain should be quite lower than 1. The function of the resistance R_2 is the reduction of the low-frequency gain of the second feedback loop.

The simulated input resistance of the TIA is reported in Fig. 3. The blue curve represents the impedance without C_1 and without the positive loop; the addition of C_1 (green curve) leads to a reduction of the high-frequency impedance and the employment of the second feedback loop (red curve) has allowed obtaining an extremely low impedance at low and medium frequencies: for frequencies up to 100 MHz, the input resistance is lower than 40 Ω. The input impedance starts to increase at a few tens of megahertz, where the dominant pole of the feedback loop is located. To introduce this pole, the C_2 capacitance has been added to the circuit. Considering the capacitance, (2) results in

$$R_{\text{in}}(s) = \frac{1/g_{m,2}}{1 + g_{m,1} \cdot R_1}$$
$$\cdot \left(1 - \frac{g_{m,3}}{1 + g_{m,3} \cdot R_2} \frac{1/g_{m,4}}{1 + sC_2 \cdot 1/g_{m,4}} \cdot g_{m,2} \cdot R_1\right). \tag{3}$$

At a first-order approximation, the dominant pole frequency is $g_{m,4}/2\pi C_2$, equal to 50 MHz. Because of the parasitic capacitances of the transistors and of the layout, the input impedance reach a maximum of 190 Ω at a 1.5-GHz frequency and then starts to decrease.

The capacitance C_2 introduces the dominant pole also in the loop gain of the circuit. To evaluate this gain, neglecting all the parasitics, it is possible to cut the feedback loop before the gate of MOSFET M_1, stimulate the circuit with a signal v and calculate the voltage v' before the cut, as shown in Fig. 4, where R_0 is the parallel between the early resistances of MOSFETs M_1 and M_6, and Z_L represents the parallel
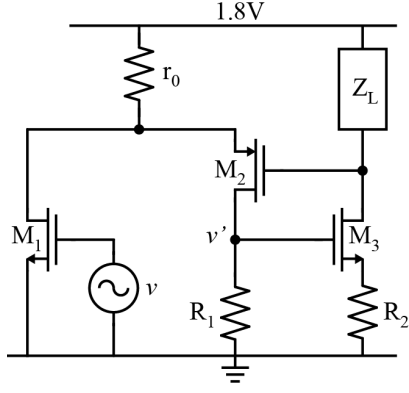
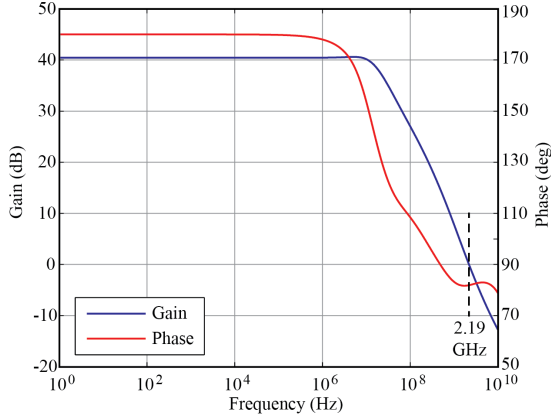Fig. 4.   Schematic for the evaluation of the TIA loop gain.

Fig. 5.   Loop gain and phase of the designed TIA.

of C_2 and M_4. The resulting loop gain is

$$G_{\text{loop}} = \frac{v'}{v}$$

$$= -g_{m,1} \frac{r_0}{r_0 + 1/g_{m,2}\left(1 - g_{m,2} \cdot \frac{g_{m,3}}{1 + g_{m,3} \cdot R_2} \cdot R_1 \cdot Z_L\right)} R_1. \tag{4}$$

The positive loop effect is visible in the current partition between R_0 and M_2: the higher is the second loop gain, the larger is the current flowing through the transistor, and the larger is the loop gain. By rearranging the expression and substituting Z_L

$$G_{\text{loop}} = -g_{m,1}R_1$$

$$\times \left(1 - \frac{1}{g_{m,2} \cdot r_0} + \frac{R_1}{r_0} \frac{g_{m,3}}{1 + g_{m,3} \cdot R_2} \frac{1/g_{m,4}}{1 + sC_2 \cdot 1/g_{m,4}}\right) \tag{5}$$

where the dominant pole introduced by C_2 is clearly visible.

The loop gain and phase of the designed TIA are shown in Fig. 5. The circuit has been dimensioned to maximize the gain while keeping a large phase margin: as said, the dominant pole is located at a few tens of megahertz, the gain at 1 GHz is equal to 8 dB, the achieved gain-bandwidth product is 2.19 GHz, and the phase margin is equal to 81°.
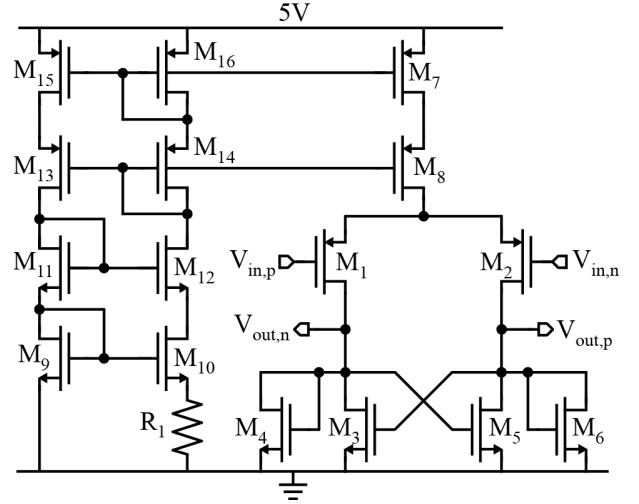

Fig. 6.   Schematic of the designed comparator.

The phase margin has to be as large as possible to avoid the pile-up effect and not introduce correlations between the two consecutive photons: after the detection of an avalanche, when the SPAD current returns to zero, the transimpedance stage has to return as fast as possible to the steady-state conditions to increase the maximum avalanche detection rate and not introduce distortions in the measurement. To the same aim, the MOSFET dimensions shown in Table I have been chosen to have a large input current dynamic range: during the detection of the avalanche current, all the transistors remain in the saturation working region and the settling time after the detection is minimized.

As said before, it is necessary to introduce in the pick-up circuit a low-pass filter, to minimize the crosstalk among the pixels. The chosen structure is suitable to this aim, since it allows decoupling the low-pass filter and the effect of the following electronic input impedance from the transimpedance stage. As shown, the low-pass filter has been implemented simply by means of the resistance R_3 and of the capacitance C_3.

To estimate the time jitter introduced by the circuit, the noise must be considered. Starting from the TIA output voltage noise, the time jitter can be calculated, as reported in [14], as

$$\sigma_t = \frac{\sigma_n}{\text{SR}} \tag{6}$$

where SR is the output voltage slope when an avalanche is detected and is equal to 4.3 kV/μs, σ_n is the *rms* output voltage noise, calculated integrating the output spectral noise density over the entire circuit bandwidth, equal to 290.9 μV, and σ_t is the TIA *rms* timing jitter. The calculated timing jitter is 68 fs, corresponding to an FWHM jitter of 0.16 ps.

Finally, the circuit biasing voltages are obtained from a self-biasing current mirror structure [15], to obtain an operation as more independent as possible from the supply voltage.

B. Comparator

The schematic of the comparator is shown in Fig. 6. The comparator has a fully differential structure so that the

sensitivity of the circuit to the external disturbances is minimized. The constant current operation avoids peak current absorption during commutations and reduces the generated power supply noise and the interference among the pixels.

To minimize the occupied area and the dissipated power, an extremely simple structure, based on a differential input pair with an active load, has been chosen [16].

To decrease the introduced noise and improve the timing performance of the pick-up circuit, a p-MOS input has been chosen: since the transistor flicker noise is the main contribution to the overall noise, this structure has been preferred to an n-MOS input one.

The circuit load consists of four transistors: the two positively feedback MOSFETs (M_3 and M_5) implement a semilatch structure, useful to completely unbalance the output voltage in the presence of very small input signals. The two transdiode connected transistors (M_4 and M_6) have two main functions: they fix the output low (0 V) and HVs (0.6 V) and they reduce the positive feedback gain of the semilatch, which otherwise would be too large and would lead to a fixed output voltage.

To estimate the obtainable time resolution, the comparator timing jitter must be calculated. The comparator has an output voltage noise of 8.95 mV *rms* and the differential output slope, during a commutation, is equal to 4.22 kV/μs. Starting from (6), the calculated *rms* timing jitter is 2.12 ps, corresponding to an FWHM jitter of 4.98 ps. Although the timing jitter introduced by the comparator is 30 times larger than the TIA one, the pixel time resolution, which will be described in the following section, will not be affected by the circuit noise.

The 5 V supply voltage has been chosen to have a comparator compatible also with the integrated pick-up circuit described in [8].

Finally, a self-biasing current mirror, to achieve independence from the supply voltage, has been used, and the biasing current has been set to 100 μA.

This way the entire pick-up circuit, including also the biasing stage and excluding only the differential output driver, requires a 500-μA current, corresponding to a dissipated power of 1.1-mW per pixel.

The comparator output signal is routed out of the integrated circuit by a standard LVDS driver based on a constant current differential stage [17] biased with a 3.5-mA current, with an internal common-mode feedback network.

C. Layout

A microphotograph of the pick-up circuit is shown in Fig. 7. The overall circuit occupies a small silicon area: the entire active area, not including the external pads, is equal to 135 μm × 115 μm; the TIA, including also the biasing circuit, has a total area of 60 μm × 70 μm and the comparator occupies a silicon area of 50 μm × 30 μm.

III. MEASUREMENT RESULTS

The main pick-up circuit performance in single-photon timing applications is the time resolution and the crosstalk
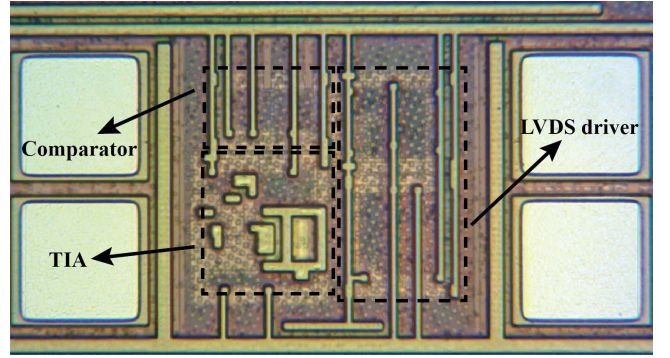

Fig. 7. Microphotograph of the integrated current pick-up circuit.

between different pixels. Both performances have been evaluated connecting to the pick-up circuit a 50-μm diameter SPAD array developed in custom technology [18], characterized by a breakdown voltage of 32.8 V and biased at a 5.7 V overvoltage. To develop the tools to simulate the circuit time resolution and to be able to improve the pick-up circuit performance, the measurement and analysis of the SPAD avalanche current growth have been performed too.

A. Time Resolution

The time resolution obtainable with the designed circuit has been measured turning on a SPAD of the array and keeping all the other detectors below the breakdown voltage, to avoid any possible crosstalk among different detectors.

The setup used to perform the resolution measurement includes a femtosecond laser (featuring an 80-MHz repetition rate and a 780-nm wavelength) that directly illuminates the SPAD and a Becker and Hickl SPC-130 module, to measure the time delay between the laser synchronism pulse and the photon detection pulse exploiting the TCSPC technique. The SPAD anode-substrate voltage has been set to −15 V and the comparator threshold voltage to 1.25 V, corresponding to an equivalent current threshold of 1.65 mA.

The measurement has been carried out in different conditions, to deeply characterize the designed circuit. Fig. 8 and Table II report the results obtained varying the average SPAD detection rate from several kilohertz per second to a few megahertz per second. The designed circuit does not introduce distortions at any frequency and the SPAD timing response is accurately acquired. The obtained FWHM resolution is lower than 50 ps for low count rates and increases to 62 ps when the SPAD detection rate increases.

Fig. 8(b) shows more in detail the peaks of the acquired waveforms: a shift of the peak position, reported also in the table and referred to the peak position at 50 kc/s, can be noticed. The peak position variation is lower than 10 ps, and therefore it is negligible if compared with the 50-ps resolution. Hence, also in an actual measurement, where the detection rate may have large variations, the pick-up circuit presents the shown time resolution and no distortions are introduced in the collected waveform.

The time resolution has been measured also as a function of the SPAD anode-substrate voltage and the results are
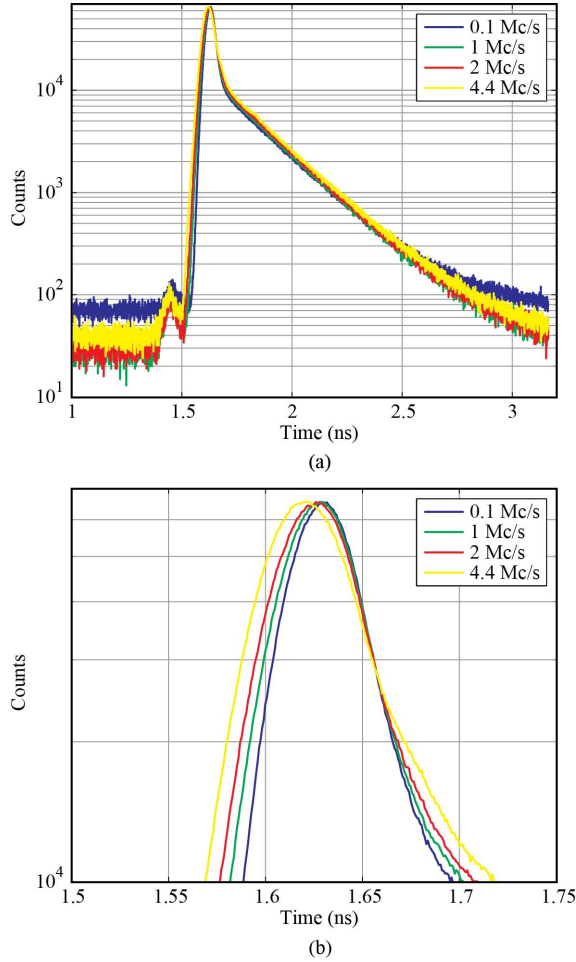
(a)

(b)

Fig. 8. (a) Time response of the designed transimpedance stage connected to a custom technology SPAD as a function of the photon detection rate. (b) Zoomed-in view of the waveform peaks.

TABLE II
TIME RESOLUTION AND PEAK POSITION SHIFT AS A
FUNCTION OF THE SPAD COUNTING RATE

Count rate	FWHM time resolution (ps)	Peak shift (ps)
50 kc/s	48.1	0
100 kc/s	48.3	0.8
200 kc/s	49	0.6
500 kc/s	50.6	-0.1
1 Mc/s	52.8	-1.4
1.5 Mc/s	54.8	-3
2 Mc/s	56.6	-3.5
4.4 Mc/s	62.3	-7.6

shown in Table III. The measurements have been carried out keeping constant the comparator threshold voltage, the detection rate (300 kc/s), and the SPAD overvoltage: this way the avalanche current growth remains unchanged, whereas the anode-substrate parasitic capacitance varies. The time resolution improves when the absolute value of the anode-substrate voltage is increased. The parasitic capacitance has a relevant influence on the obtainable performance: when the

TABLE III
TIME RESOLUTION AND PEAK POSITION VARIATION AS A FUNCTION
OF THE SPAD ANODE-SUBSTRATE VOLTAGE

Anode-substrate voltage (V)	FWHM time resolution (ps)	Peak shift (ps)
-6	56.3	0
-9	52.8	-10.5
-12	51	-17.9
-15	50.1	-23.3
-18	48.7	-27
-21	48.4	-29
-24	47.9	-29.9

TABLE IV
TIME RESOLUTION AS A FUNCTION OF THE
COMPARATOR THRESHOLD VOLTAGE

Threshold voltage (V)	Equivalent current threshold (mA)	FWHM time resolution (ps)
1.7	0.035	41.5
1.6	0.4	49
1.5	0.75	50.4
1.4	1.1	50.7
1.3	1.45	50.3
1.2	1.82	49.3
1.1	2.18	50.3
1	2.54	52

applied voltage decreases, the thickness of the SPAD space charge region increases and the capacitance value decreases; therefore, the high-frequency parasitic impedance becomes more relevant and a larger percentage of current flows in the pick-up circuit. This behavior is confirmed by the peak position variation: the smaller is the parasitic capacitance, the earlier the pick-up circuit reveals the avalanche, meaning that the actual current threshold is reduced. Hence, to improve the time resolution obtainable with the pick-up circuit, it is necessary to further reduce the high-frequency input impedance, and to make it much lower than the parasitic anode-substrate capacitance.

Finally, the time resolution has been evaluated as a function of the comparator threshold voltage. As reported in Table IV, the obtained performance shows an independence from the equivalent current threshold, if the first, extremely low value is excluded. This behavior makes possible the use of the current pick-up circuit with a high equivalent current threshold, so that a larger immunity to noise and crosstalk can be obtained.

B. Crosstalk

To measure the crosstalk between two pixels, a second SPAD of the array, next to the observed one, has been turned on. To evaluate the possible performance degradation, a time-resolution measurement, similar to the already described one, has been performed. In this case, to record the data of both detectors, a multichannel TCSPC board [19] has been used.

Fig. 9(a) reports the result obtained with an average count rate of 1.5 Mc/s of both the observed and the
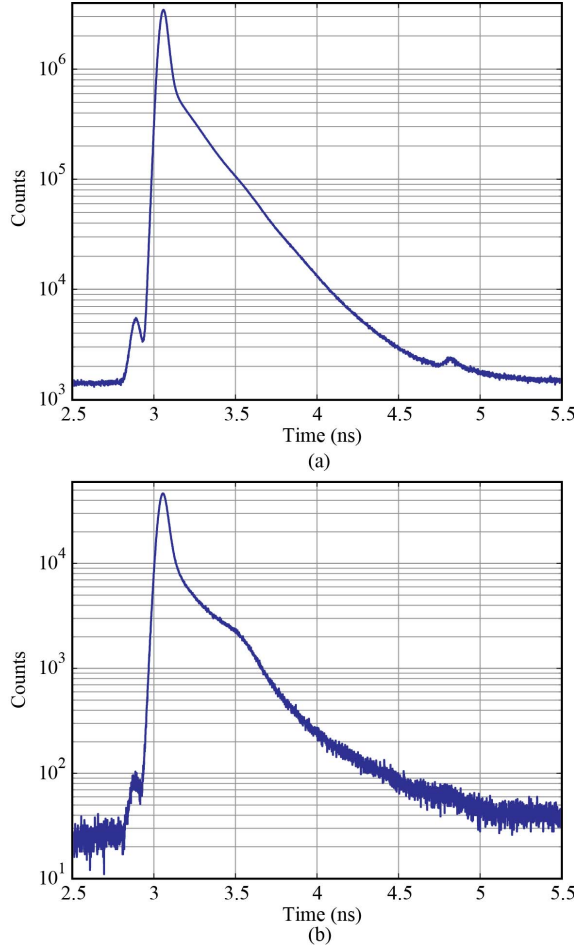
Fig. 9. (a) Time response of the system when a second SPAD of the array is turned ON. (b) Time response of the system when the two SPADs simultaneously detect a photon.

Detection time difference (ns)	FWHM time resolution (ps)	Peak shift (ps)
No interfering SPAD	57.8	0
-62.5	62.4	-3.9
-50	60.3	5.3
-37.5	60.5	0.3
-25	58.9	-1.4
-12.5	59.2	3.6
0	68.5	2.8
12.5	58.8	1.1
25	58.7	0.3
37.5	58.8	0.3
50	58.7	1.1
62.5	58.8	0.3

photon, measured as a macrotime from the beginning of the experiment and a microtime in each excitation cycle. It is thus possible to extract the temporal response of the designed circuit only when the two SPADs detect a photon in the same laser pulse. The result of this measurement is shown in Fig. 9(b): a time resolution of 68.5 ps has been obtained and no peak shift is present. Hence, the crosstalk has a nonnegligible impact on the circuit resolution, but does not introduce distortions in the acquired waveform. A distortion can be noticed in the SPAD diffusion tail. The distortion is not due to the pick-up circuit, but to the optical crosstalk between the SPADs [20]: the optical crosstalk probability is absolutely not negligible compared with the probability of a contemporaneous detection of two photons. Therefore, the acquired waveform is the superposition of the time resolution and the optical crosstalk curves.

The same measurement has allowed obtaining the time resolution and the peak position as a function of the time difference between the photon detections of the observed and of the interfering SPADs; the results are reported in Table V. The only relevant variation, compared with the case with a single SPAD turned on, is the worsening of the time resolution when the two SPADs detect simultaneously a photon. A more relevant peak position shift can be noticed when the interfering SPAD detects a photon between 62.5 and 50 ns before the observed SPAD. The crosstalk is connected to the AQC reset phase: if the observed detector reveals a photon when the interfering AQC is resetting the SPAD, a peak position shift can be noticed. This behavior can be due both to a disturbance read by the pick-up circuit but also to a crosstalk internal to the AQC array: the reset of one AQC may directly couple a disturbance on the observed SPAD cathode.

Since the crosstalk leads only to a slightly resolution worsening, it will not introduce distortions in the measurement or correlations among the data collected by different detectors. Moreover, as shown in Fig. 9(a), the crosstalk in an actual measurement is absolutely negligible and hence, also in the
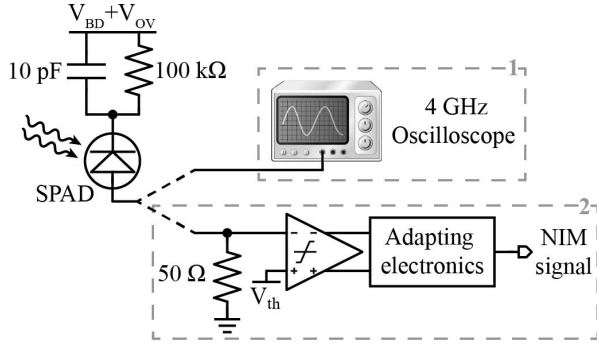
interfering SPADs. No distortions are clearly visible and the obtained time resolution is equal to 63 ps: since the multichannel TCSPC electronics has a time resolution of 25-ps FWHM, the actual resolution of the SPAD and of the pick-up circuit is 57.8 ps, comparable to the value reported in Table II. Moreover, also the peak position shows no shift between this measurement and the one with a SPAD turned ON.

Although this measure well represents the pixel operation in an actual setup, it is not significant for the crosstalk estimation: each SPAD has a count rate equal to 1.9% of the laser frequency, hence the probability that the two SPADs reveal a photon in the same laser pulse is equal to 1.9%.

The interfering SPAD generates disturbances and crosstalk only when it detects a photon and when its AQC quenches and resets the detector, i.e., when an impulsive current is absorbed from the biasing voltages, common among the pixels. Hence, only a small percentage of the data used to build the histogram in Fig. 9(a) is influenced by the interfering SPAD operation.

To obtain a more detailed evaluation of the crosstalk, a second measurement has been performed: the data have been acquired by the TCSPC electronics in time-tag [1] mode. In this case, the TCSPC system does not build up the photon distribution, but records the arrival time of each detected

Fig. 10. Setups employed to estimate the SPAD avalanche current growth.

Fig. 12. Estimated rising edges of the SPAD anode voltage after the detection of a photon. Blue curve—typical waveform. Green curve—steeper voltage growth. Red curve—slower voltage growth.
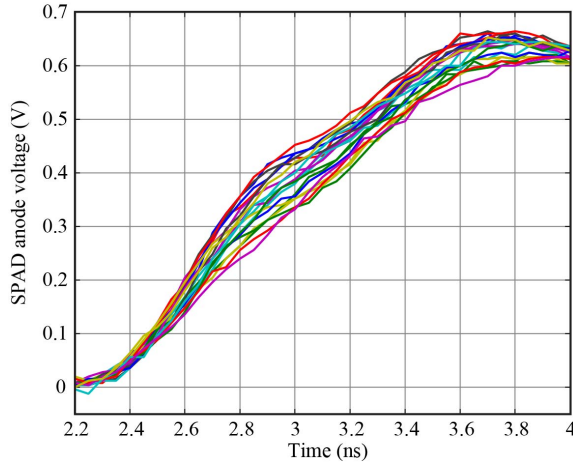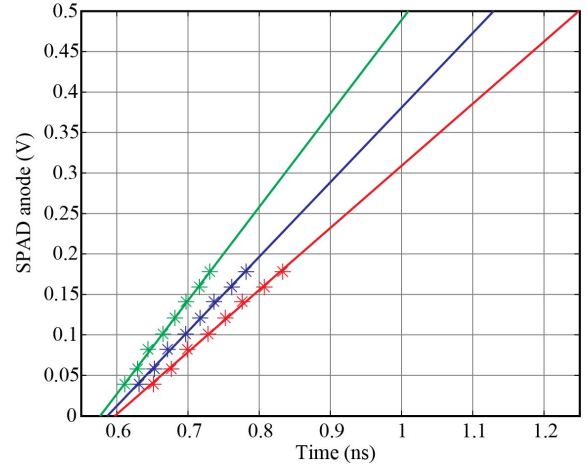

Fig. 11. Measured rising edges of the SPAD anode voltage after the detection of a photon.

presence of a large number of pixels, no significant distortions can be expected.

C. SPAD Avalanche Current Growth

To be able to simulate the pick-up circuit time resolution and to improve its performance, the knowledge of the SPAD avalanche current growth is of the utmost importance. To evaluate the growth of the SPAD current, the setups shown in Fig. 10 have been used. In this case, the SPAD, biased at a 5 V overvoltage, has been illuminated with a 100-KHz pulsed laser, to attain a count rate of about 5 kc/s, so that a passive quenching circuit (the 100-kΩ resistance) can be used without influencing the measure. The external 10-pF capacitance makes the parasitic anode–cathode capacitance negligible, and no current flows through the SPAD parasitics.

In the first measurement, the SPAD anode has been connected directly to a 4-GHz bandwidth oscilloscope input and the internal 50-Ω termination resistance has been used to sense the anode voltage. One thousand acquisitions have been performed and 20 of them are reported in Fig. 11. An average 10%–90% rise time of 1.25 ns and an average maximum current of about 13 mA have been measured. The rise time presents a dispersion of 132-ps FWHM.

The described measurement presents some limitations regarding the assessment of the avalanche current growth: first, due to the temporal alignment at the trigger voltage value, a possible initial dispersion, due to a jitter in the avalanche triggering, cannot be recorded. Second, the oscilloscope sampling rate of 20 GS/s introduces a 50-ps jitter in the acquisition and may lead to an error in the measured dispersion.

Hence, to validate the previous measurement, a second setup, shown in Fig. 10, has been employed. The SPAD avalanche current flows in a 50-Ω resistance, and a fast comparator (ADCMP563) discriminates the time the anode voltage crosses and adjustable threshold. An SPC-130 board has been used therefore to measure the time delay between the photon emission from the laser and the time the anode voltage reaches the threshold value.

With this setup, by changing the comparator threshold voltage, it is possible to reconstruct the behavior of the SPAD anode voltage, and hence of the avalanche current, as a function of the time and, by repeating the measurement, the distribution of the threshold crossing times may be acquired. The acquired distribution peak corresponds to the typical anode voltage trend, whereas the dispersion indicates the limits the voltage grows within.

The result of the measurement is shown in Fig. 12: the SPAD anode voltage average rising (blue crosses) approximately follows a linear trend, which has been interpolated by the blue line. To also consider the SPAD avalanche propagation statistics, the time resolution of the measurement has been considered: the time obtained subtracting half of the FWHM resolution from the peak position has been used to obtain the steeper SPAD current growing (green crosses), while the time obtained adding half of the FWHM resolution to the peak position has allowed to obtain the slower SPAD current growing (red crosses).

Eventually, the trend of the SPAD avalanche current has been evaluated: it presents an average slope of 19 mA/ns and a dispersion, due to the avalanche propagation, increasing at a 21-ps/mA rate. Moreover, by extrapolating the
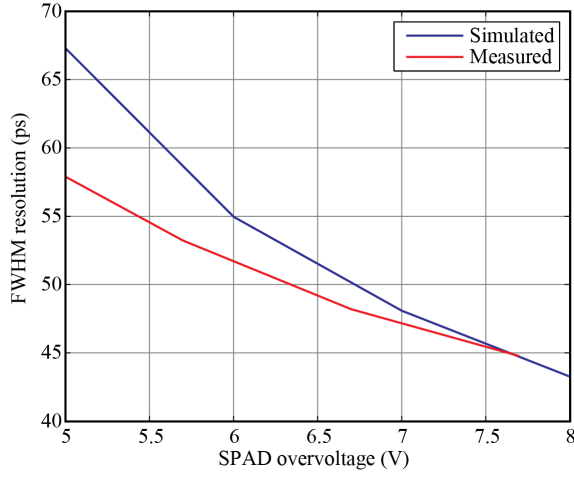
Fig. 13. Comparison of the simulated and measured time resolution obtainable with the designed pick-up circuit connected to a custom SPAD as a function of the SPAD overvoltage.

	Time resolution (ps)	Crosstalk	Dissipated power (mW)	Area (μm^2)
Ref. [7]	35	100 %	0	Discrete components
Ref. [8]	45	Negligible	12	17700
Ref. [10]	34.4	Negligible	100	Discrete components
This work	48.1	Negligible	1.1	15500

shape can be useful to adapt the pick-up circuit to detectors with different characteristics and always keep state-of-the-art performance.

IV. CONCLUSION

In this paper, we presented an integrated read-out circuit for custom technology SPADs, based on a TIA with a 2.2-GHz bandwidth. The main performance of the presented circuit, compared with other pick-up circuits described in the literature, are reported in Table VI.

The 1.1-mW power dissipation, the small area ($15\,500\ \mu m^2$) and the negligible crosstalk make the presented pick-up circuit suitable for large multipixel systems, and the 48-ps time resolution, together with the small discrepancy (14%) between the simulated and the measured data constitutes a solid starting point for the future development of improved performance circuits.

The innovation introduced by the designed circuit, i.e., the direct detection of the detector avalanche current, overcomes the tradeoff between the time resolution and the crosstalk of the classical structures.

Hence, the designed TIA will open the way to the development of large multichannel systems for single-photon timing applications based on custom SPADs, fully exploiting the advantages of these devices over the CMOS ones.

interpolating lines at zero current, an initial dispersion of 20 ps, connected to the avalanche triggering, has been noticed.

However, the described measurement is not directly comparable with the one performed using the fast oscilloscope. Indeed, the obtained waveform is filtered by the comparator input stage, having a 750-MHz bandwidth, whereas the oscilloscope waveform is acquired without filtering effects. Hence, a second measurement with the oscilloscope has been performed.

To reproduce the comparator filtering effect, the bandwidth has been limited to 750 MHz. To collect the current statistics, a 1000 acquisitions have been performed: the resulting waveforms present a dispersion increasing at a 20.4-ps/mA rate, similar to the one obtained with the previous, completely different, setup. Therefore, this measure has confirmed and validated the already obtained data.

Eventually, the SPAD avalanche current growth has been estimated combining the results of the previous measurements: as an example, at a 5 V overvoltage, the avalanche current presents an initial dispersion of about 20 ps (measured with the TCSPC setup) and a rise-time dispersion of 132 ps over an average time of 1.25 ns (obtained from the 4-GHz oscilloscope measure).

Using the measured avalanche trigger and current growth dispersions, it has been possible to simulate the time resolution to be obtained with the designed pick-up circuit. The results of the simulation, compared with the measured data, are shown in Fig. 13, as a function of the SPAD overvoltage. The measured and the simulated performance show a maximum difference of 9 ps at a 5 V overvoltage, corresponding to a 14% error. The good agreement between the simulated and the measured time resolution allows having an important tool for the future development of the current pick-up circuit. In particular, the understanding of the factors that limit the time resolution will allow to further improve the circuit performance and to reach the 34-ps best-in-literature resolution. Moreover, the possibility to estimate the obtainable time resolution starting from the SPAD avalanche current

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