Voltage-controlled cycling endurance of HfO_x-based resistive-switching memory (RRAM)

S. Balatti, *Student Member, IEEE*, S. Ambrogio, *Student Member, IEEE*, Z.-Q. Wang, S. Sills, A. Calderoni, N. Ramaswamy, *Senior Member, IEEE*, and D. Ielmini, *Senior Member, IEEE*

***Abstract*—Resistive-switching memory (RRAM) based on metal oxide is currently considered as a possible candidate for future non-volatile storage and storage-class memory (SCM). To explore possible applications of RRAM, the switching variability and cycling endurance are key issues that must be carefully understood. To this purpose we studied switching variability and endurance in pulsed regime for HfO_x-based RRAM. We found that the resistance window, the set/reset variability and the endurance are all controlled by the maximum voltage V_{stop} which is applied during the negative reset operation. We demonstrate that endurance failure is triggered by a negative set event, where the resistance suddenly decreases during reset. Cycling endurance is studied as a function of time, compliance current and V_{stop}, allowing to develop an Arrhenius-law model which is capable of predicting device lifetime under various condition.**

Keywords: Resistive switching memory (RRAM), cycling endurance, memory reliability, device modeling.

I. Introduction

Resistive switching memory (RRAM) features a number of advantages, such as fast switching [1], [2], low power operation [3] and good scalability [4], thus serving as potential candidate for future mass storage and storage class memory [5], [6]. However, many reliability issues still need to be addressed and understood, such as switching variability and endurance failure. Previous works mainly addressed the switching variability in the quasi-static regime [7]–[12], although operation is carried out in the pulsed regime, *e.g.*, below 1 μs pulse-width. Endurance was also addressed by many previous works [13]–[18], although a systematic study of the impact of voltage, current and pulse-width is still missing.

In this work we focus on cycling variability and endurance failure in HfO_x RRAM at variable maximum (most negative) voltage V_{stop} in the negative reset operation. We discuss the dependence of the resistance distribution on V_{stop} for the low resistance state (LRS) and high resistance state (HRS), highlighting the origin of distribution tails. Then we address cycling endurance, showing that failure is generally induced by negative set where the current suddenly increases during the application of negative voltage. We present a comprehensive study of the impact of V_{stop}, compliance current and pulse-width on the endurance lifetime. Finally, we introduce an Arrhenius model that can account for the cycling endurance as a function of V_{stop} and pulse width. A preliminary study on cycling endurance was reported in [19]. Here we extend the analysis of [19] by addressing the impact of compliance current on endurance, by studying the reversibility of failure through multiple reset or increased compliance current, and by introducing a 2T1R structure to limit the current during negative set.

S. Balatti, S. Ambrogio, Z.-Q. Wang and D. Ielmini are with the Dipartimento di Elettronica, Informazione e Bioingegneria and Italian Universities Nanoelectronics Team (IU.NET), Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy. (E-mail: simone.balatti@polimi.it, stefano.ambrogio@polimi.it, zhongqiang.wang@polimi.it and daniele.ielmini@polimi.it)

S. Sills, A. Calderoni and N. Ramaswamy are with Micron Technology Inc., Boise, ID 83707 USA (e-mail: ssills@micron.com, acaldero@micron.com and dramaswamy@micron.com)

II. RRAM devices and characteristics

We characterized RRAM devices, consisting of a Si-doped hafnium oxide switching layer interposed between a TiN bottom electrode (BE) and a Ti top electrode (TE) [18]. The Ti TE acts also as oxygen exchange layer (OEL) inducing an oxygen deficiency in the active layer by partial oxidation [20]. Fig. 1a schematically shows the device structure, including the RRAM element in series with a transistor in the so called 1T1R architecture. Here, the select transistor was integrated on the same chip of the RRAM device, with the purpose of limiting the current during the set transition [21]. To characterize the device in the pulsed regime we adopted the experimental setup reported in Fig. 1b. Two channels of an arbitrary waveform generator were connected to the TE of the RRAM and the gate of the transistor respectively, while the cell current was measured by the voltage drop across the 50 Ω input resistance of the oscilloscope [22]. This setup allows to collect the switching characteristics of each cycle.

Fig. 2a shows the typical waveform of the voltage applied at the TE, consisting of the sequence of 4 triangular pulses, namely (i) a positive voltage pulse for set transition, (ii) a positive pulse of lower voltage for reading the LRS, (iii) a

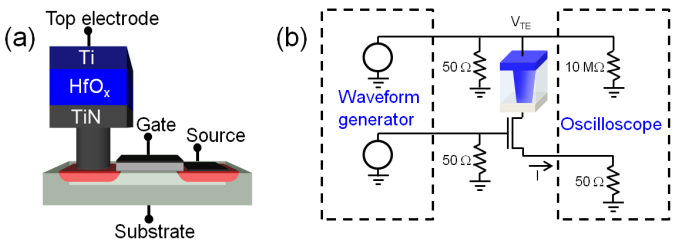

Fig. 1. Schematic layout of the 1T1R structure used in this work (a) and experimental setup (b) including a 2-channels waveform generator (left) driving the gate and TE of the 1T1R cell (center) and an oscilloscope (right) to probe the TE voltage and 1T1R current.

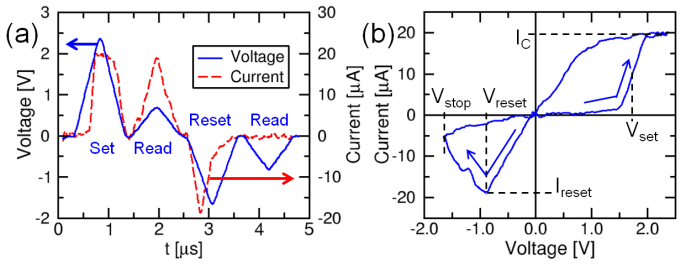

Fig. 2. Measured TE voltage V and current I (a) and typical I-V characteristic (b) obtained from the measured V and I. Parameters are defined as follows: V_{set} is the set voltage marking the current crossing 10 μA, I_C = 20 μA is the compliance current, R is the resistance of the RRAM device, V_{reset} is the reset voltage marking the first increase of resistance, I_{reset} is the corresponding reset current and V_{stop} is the maximum (most negative) voltage in the negative voltage sweep during reset.

negative voltage pulse for reset transition, and (iv) a negative voltage pulse for reading the HRS. Fig. 2a also shows the measured current during the same 4-pulses sequence. An opposite polarity for the read pulses was used to minimize read disturb where, for instance, a positive read voltage might induce partial set transition in HRS. The read voltage was 0.7 V for LRS and -0.8 V for HRS. Read disturb occurred only above 1 V, thus higher than the read voltages used in this work. A pulse-width t_P of 1 μs was used in Fig. 2a and throughout the whole manuscript, except where noted. The transistor was biased at relatively low gate voltage during the set transition, to limit the set current below a compliance current I_C, typically below 50 μA. On the other hand, the transistor was biased with a relatively large gate voltage during the read and reset pulses to minimize the voltage drop across the transistor.

The voltage and current traces in Fig. 2a allow to extract the I-V characteristics of the device in Fig. 2b. The set transition from HRS to LRS takes place as an abrupt increase of the current at the positive set voltage V_{set}. Following the set transition, the current is limited below I_C, equal to 20 μA in Fig. 2, thanks to the low-gate biased transistor. Under negative voltage, the reset transition appears as a more gradual decrease of current starting from the reset voltage V_{reset}. The negative voltage sweep in Fig. 2b was interrupted at a voltage V_{stop} which is a key parameter controlling HRS resistance [20] and failure endurance [19].

III. Cycling Variability

We first studied the impact of V_{stop} on switching variability, we cycled a RRAM device at variable V_{stop} from -1.2 V to -1.9 V, with a step of 0.1 V. A sequence of 10^3 cycles as shown in Fig. 2a was carried out for each value of V_{stop}, to ensure a proper statistical analysis. Fig. 3 shows the cumulative distribution of resistance R for LRS (a) and HRS (b) at increasing V_{stop} with t_P = 1 μs and I_C = 20 μA. An increase of V_{stop} results in an increase of the tails at low and high resistance in the LRS distribution. The tail at low resistance is caused by an overshoot effect due to a parasitic capacitance between the RRAM device and the selector transistor [19], [21], [23], [24]. During a set transition at large V_{set}, due to a relatively high HRS resistance, the current immediately after set might exceed I_C, as a result of the parasitic capacitance charging across the RRAM device. The excess overshoot current causes an overgrowth of the conductive filament (CF) in the set state, thus resulting in a relatively low LRS resistance contributing to the low-resistance tail in Fig. 3a. On the other hand, the high resistance tail in the LRS distribution can be explained by the incomplete set of HRS with relatively high resistance. On the other hand, the HRS distribution in Fig. 3b shows a shift toward large R and a decrease of statistical spread for increasing V_{stop}. The tightening of the distribution with V_{stop} can be understood by the increasing number of defects contributing to the CF depletion during reset, which thus display a smaller Poisson statistics in the number and position within the CF depleted gap.

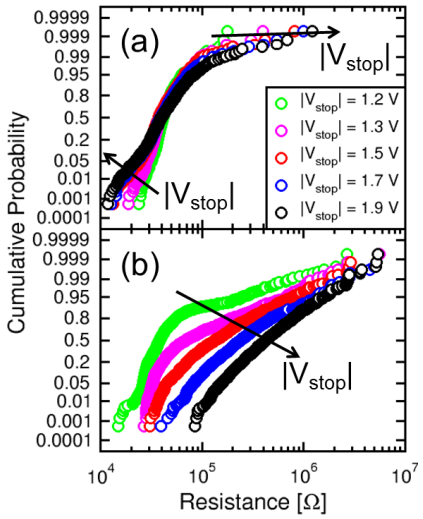

Fig. 3. Distributions of the measured R for LRS (a) and HRS (b) for I_C = 20 μA, t_P = 1 μs and $|V_{stop}|$ increasing from 1.2 to 1.9 V. As $|V_{stop}|$ increases, the LRS tails at both high and low resistance increase and the spread of the HRS distributions decreases.

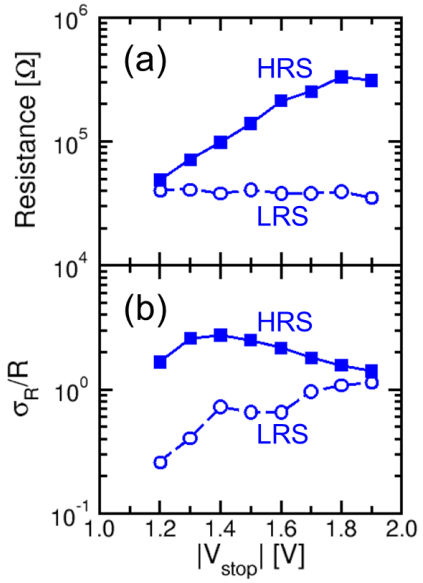

Fig. 4. Median values (a) and normalized standard deviation σ_R/R (b) of resistance as a function of $|V_{stop}|$ for I_C = 20 μA in both HRS and LRS.

The impact of V_{stop} on resistance distributions is summarized in Fig. 4, showing the median resistance (a) and the normalized standard deviation σ_R/R (b) for LRS and HRS as a function of $|V_{stop}|$. The resistance window increases with $|V_{stop}|$ due to an increase of HRS resistance, as the depleted gap formed by ion migration along the CF increases with V_{stop} [20]. On the other hand, LRS resistance remains constant on the average by increasing $|V_{stop}|$, since R is mainly controlled by I_C in the set transition [21]. The normalized standard deviation σ_R/R in Fig. 4b indicates that HRS variability decreases at increasing $|V_{stop}|$ higher than 1.4 V due to the tightening of the distribution in Fig. 3b. On the other hand, LRS variability increases with $|V_{stop}|$ due to the distribution tails at low/high R appearing at large $|V_{stop}|$ in Fig. 3a. These results suggest that a high $|V_{stop}|$ should be used to maximize read margins against program variability and noise in RRAM.

IV. Cycling Endurance

We studied the endurance failure by monitoring all switching characteristics for all cycles during the whole lifetime of the RRAM device. Fig. 5a shows the measured resistance for LRS and HRS during a cycling experiment, for t_P = 1 μs and I_C = 50 μA. The measured resistances are almost constant for about 1.7×10^5 cycles, then the resistance window collapses as the device falls in a state with intermediate resistance between LRS and HRS. The resistance evolution around failure is highlighted in Fig. 5b, showing a gradual decrease of HRS resistance and an increase of LRS resistance lasting around 50 cycles [19]. Note that the failure mode in our device is different from the usually reported stuck-set or stuck-reset states in the literature [12] [13].

To better understand the failure mechanism in our RRAM device, Fig. 6 shows three representative I-V characteristics

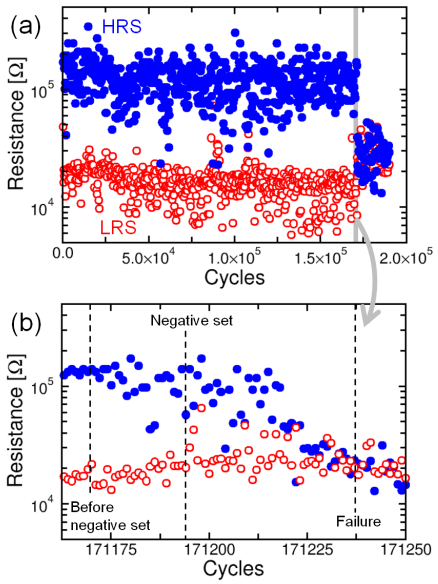

Fig. 5. Measured R as a function of the number of cycles (a) and a close-up of the region in correspondence of failure around 1.7x10^5 cycles (b). Endurance failure is due to collapse of the resistance window at an intermediate resistance level between HRS and LRS. The marked cycles correspond to a standard set/reset cycle, the negative-set event and final window collapse.

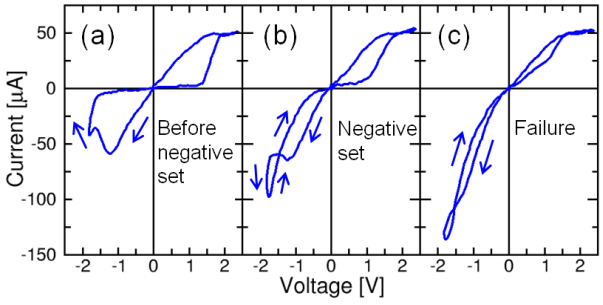

Fig. 6. Measured I-V curves corresponding to the marked locations in Fig. 5b, namely typical switching before negative set (a), negative-set event (b) and failure (c).

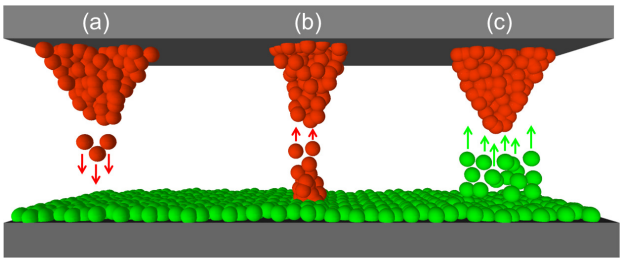

Fig. 7. Sketch of the defects migration during set transition (a), reset transition (b) and negative set (c). In red are reported the defects coming from the TE interface and in green the defects coming from the BE, the arrows show the migration direction, according to the applied voltage.

corresponding to the cycles marked in Fig. 5b and highlighting (i) the device behavior before failure, (ii) the negative-set event responsible for failure and (iii) and the device behavior after failure, respectively. The device shows typical set/reset transitions with well defined LRS and HRS states and $I_{reset} \approx I_C$ in Fig. 6a. Fig. 7 schematically shows the set transition (a) where the positive voltage induces defect migration from the reservoir into the CF region, and the reset transition (b), where the negative voltage induces migration toward the TE thus leaving behind a depleted gap along the CF. The device unexpectedly shows an anomalous reset behavior in Fig. 6b, which we refer to as negative set. In the negative-set process, the application of a negative voltage results in a reset transition followed by an increase of the current to almost 100 μA, *i.e.*, significantly higher than the typical $I_{reset} \approx I_C$. We interpreted this current increase as a defect injection from the interface between the BE and the switching layer. As shown in Fig. 7c, defects during negative reset are injected from the BE interface toward the TE, thus contributing to the defect reservoir of the CF. The negative set current is not limited, since the gate of the transistor connected in series is biased with a large voltage to minimize the series resistance during the reset. As a result, the number of defects injected at negative reset are only limited by the BE interface, resulting in a large increase of the defect reservoir and of the CF area. Since HRS resistance is controlled by the cross section of the CF, HRS resistance significantly decreases after negative set. Any subsequent set transition is inhibited, since the voltage drop across the RRAM device during the application of a positive voltage is smaller than V_{set}. In other words, the compliance current I_C is below

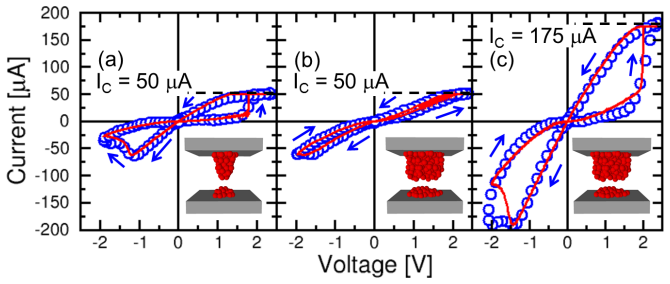

Fig. 8. Measured and calculated I-V curves for typical switching before negative set (a), switching with limited hysteresis after negative set (b) and switching after negative set with increased I_C = 175 μA (c). The set transition cannot take place in (b) due to the insufficient voltage drop across the leaky HRS. Switching can be recovered at large compliance I_C = 175 μA (c), where the higher voltage drop across the RRAM allows for set transition.

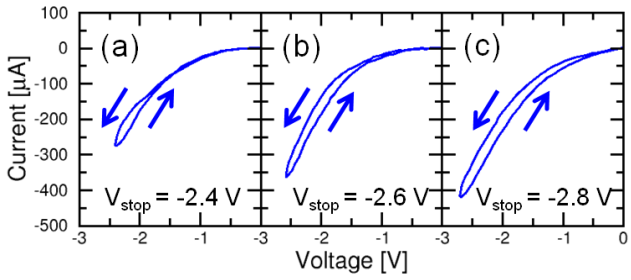

Fig. 9. Measured I-V curves after failure at increasing V_{stop} = -2.4 V (a), -2.6 V (b) and -2.8 V (c). Data show that the HRS leakage after negative set cannot be recovered by repeated reset pulses at increasing $|V_{stop}|$.

the threshold current needed to trigger set transition in the new HRS state after negative set. We found that irreversible endurance failure was always triggered by negative set event in our devices.

To support our interpretation of the final state after the negative set Fig. 8 shows the measured and calculated I-V curves for 3 device and bias conditions. In a typical set/reset cycle (a), the HRS is characterized by a relatively small cross section dictated by the cycling I_C = 50 μA (see inset). The calculated I-V curve in the figure was obtained by our analytical model for set/reset based on ion migration [25]. The I-V curve in Fig. 8b was measured after negative set and shows no hysteresis, similar to Fig. 6c. This is because set transition cannot take place, due to the large CF cross section (see inset) and consequent high conductivity of HRS after negative set. To confirm this interpretation, we calculated the observed I-V curve by considering a leaky HRS with a very large cross section. The calculated I-V curve shows no set transition due to the insufficient voltage drop under positive voltage. To further confirm this interpretation, Fig. 8c shows the measured I-V curve after negative set for a larger I_C, equal to 175 μA in this case. The device again shows set and reset transition, thus confirming that functionality is maintained in the device even after negative set. The larger gate bias in the transistor results in a larger voltage drop across the RRAM device, which thus can reach the set voltage. Calculated I-V curves show good agreement with data assuming the same CF cross section as in Fig. 8b and I_C = 175 μA.

Results in Fig. 8 confirm that the window collapse is due to the large CF cross section induced by unlimited defect injection at negative set. To reduce the CF cross section, we tried to apply repeated reset sweeps at increasing $|V_{stop}|$. Fig. 9 shows the measured I-V curves under negative voltage after negative set for V_{stop} = -2.4 V (a), -2.6 V (b) and -2.8 V (c). Only a minor hysteresis was revealed, with no relevant reduction of the leakage current. A higher resistance could not be achieved even after repeated reset sweeps for 10^3 times at V_{stop} = -2.8 V. These results can be understood in the frame of the physical mechanism for reset [26]: as an increasing negative voltage is applied to the CF, more defects move vertically along the CF direction toward the negatively-biased TE, thus leaving behind a depleted gap. The vertical migration, however, is neither capable of reducing the CF cross section, nor to reduce the number of defects in the reservoir. Therefore, the HRS resistance can hardly be recovered by the reset operation.

Note that, based on the available data, we cannot rule out that negative set failure takes place at a localized path away from the original CF. However, this looks rather improbable, since the electric field and current density, which are at the origin of Joule-heating and consequent degradation are maximum at the CF [26]. In fact, electric field is higher at the CF, since the high-resistance depleted gap is much thinner than the original thickness of pristine HfO_x [26]. Also, HRS is known to be affected by a leakage current which is much larger than the pristine condition. Therefore, we conclude that due to the high field and high current density, negative set most probably takes place at the CF.

V. Impact of V_{stop}

Fig. 10 reports the measured number of cycles to failure N_C as a function of $|V_{stop}|$ at increasing I_C = 10 μA, 20 μA and 50 μA. Endurance steeply decreases for $|V_{stop}|$ larger then 1.6 V. This can be explained by the critical role of V_{stop} in inducing breakdown of the BE interface, so that the probability of a negative set increases for increasing V_{stop}.

For $|V_{stop}|$ smaller then 1.6 V, instead, N_C sharply increases. To better understand the sharp increase of the endurance at low $|V_{stop}|$, Fig. 11a shows the resistance for LRS

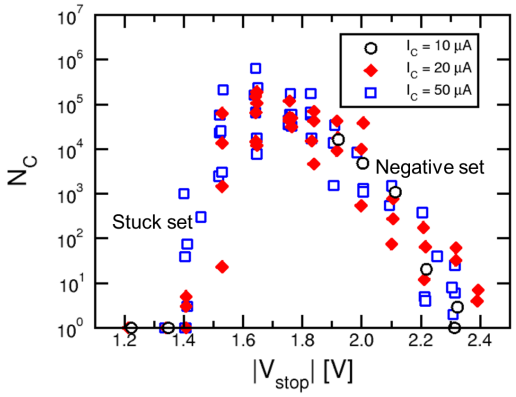

Fig. 10. Measured N_C as a function of V_{stop} for variable I_C, namely I_C = 10, 20 and 50 μA. Endurance decreases sharply with $|V_{stop}|$ in the negative-set regime, with no obvious dependence on I_C.

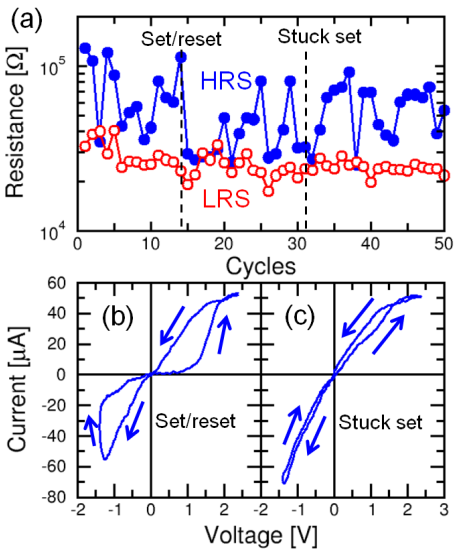

Fig. 11. Measured R as a function of cycles for relatively low V_{stop} = -1.4 V (a) and measured I-V curves corresponding to successful reset (b) and stuck set (c). The fluctuating resistance window is due to randomly occurring reset transition, with no reset failure due to insufficient V_{stop}.

and HRS during a cycling experiment with V_{stop} = -1.4 V. The HRS resistance largely fluctuates between about 10^5 Ω and the LRS resistance around few 10^4 Ω, because the applied negative voltage is not sufficient to guarantee a complete reset transition for all cycles. This is highlighted in Fig. 11 showing 2 selected I-V characteristics from Fig. 11a, corresponding to a reset operation (negative sweep) followed by a set operation (positive sweep). Fig. 11b shows the case of a complete reset transition while in Fig. 11c the reset transition does not take place. The random fluctuation in Fig. 11a indicates that reset transition can take place stochastically during cycling, as a result of the random fluctuation of the characteristic V_{reset} at each cycle [20]. Note that this random 'stuck-set' behavior is not a real failure of the cell, rather it constitute a malfunction due to the insufficient V_{stop}. In fact, we verified that the correct device cycling behavior can be recovered at any time after random stuck-set by using a larger V_{stop}.

VI. Impact of Set/Reset Current and Pulse-Width

Fig. 10 also shows that the impact of I_C on N_C is negligible. This can be understood be recalling that I_C controls the cross section of the CF, while maintaining constant electric field, temperature and current density during set and reset [26], [27]. The local temperature and field at the BE interface controlling the negative set event are thus still dictated by V_{stop}, thus explaining the independence from I_C in Fig. 10.

To prevent CF overgrowth during negative set and the consequent collapse of resistance window, the current during the negative voltage sweep for reset should be limited below a compliance level. Current control under negative V_{TE} is not straightforward in the 1T1R, since the transistor current is dictated by the potential difference between the gate and the intermediate node between the transistor and the RRAM. The latter potential depends on the voltage division between RRAM and transistor, thus current control requires ad-hoc waveforms of the gate voltage and an accurate prediction of the resistance for the LRS, which is generally not possible due to resistance fluctuations [8]. On the other hand, the current during reset can be easily controlled in the 2-transistors/1-resistor (2T1R) structure in Fig. 12a, where a second transistor is connected to the top electrode of the RRAM device. During set transition, the bottom transistor in Fig. 12a can act as current limiter, while the top transistor is biased to high conductance to minimize voltage drop. On the other hand, during reset transition, the bottom transistor is biased to high conductance while the top transistor is used to limit the current during reset operation. We verified that the top transistor does not affect the usual set/reset characteristics (Fig. 12b), while it allows to limit the current during negative set, as shown in Fig. 12c, thus preventing filament overgrowth.

Fig. 12d shows endurance as a function of V_{GS2}, for constant $V_{stop} = -1.65$ V, corresponding to the peak of N_C in Fig. 10. At small V_{GS2} the current compliance set by the top transistor is lower than I_{reset}, therefore the cell cannot reset and endurance is limited by the stuck-set behavior, similar to the regime at low $|V_{stop}|$ in Fig. 10. At larger V_{GS2}, N_C increases above 10^6 then decreases again toward the 1T1R value as the top transistor is no longer limiting the negative set current.

To study the impact of pulse-width t_P on endurance, we conducted cycling experiments for increasing t_P, in the range between 100 ns and 1 ms, at constant compliance current I_C = 50 μA. Fig. 13a shows N_C as function of V_{stop} for increasing t_P. The endurance shows the same dependence on V_{stop} independently on t_P, featuring the 2 regimes of stuck-set at low V_{stop} and negative set at high V_{stop}. The endurance curves display a shift toward smaller voltage for increasing t_P, which can be explained by the V-accelerated nature of the switching [28]. As t_P increases, the voltage needed to induce set and reset transitions decreases. Similarly, based on the voltage-accelerated nature of negative set, the voltage needed to induce a negative set decreases, thus resulting in the observed shift to lower V_{stop} of the endurance curve in Fig. 13a.

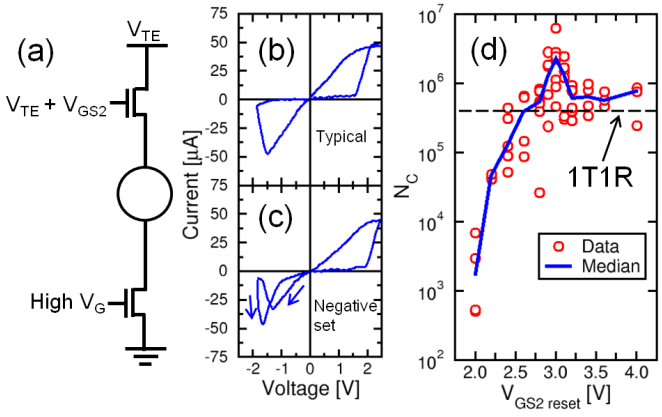

Fig. 12. Schematic of the 2T1R structure biased for the reset operation (a), I-V curves for typical set/reset behavior (b) and negative set (c), and measured N_C as a function of V_{GS2} for V_{stop} = -1.65 V (d). Data show an increase of endurance by almost 10x in 2T1R at V_{GS2} = 3 V thanks to suppression of filament overgrowth during negative set (c).

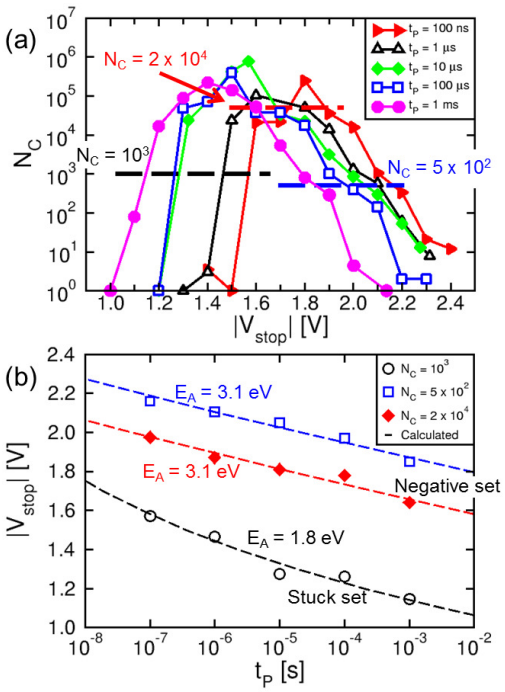

Fig. 13. Measured N_C as a function of V_{stop} for increasing t_P (a) and extracted V_{stop} from (a) at various N_C for the stuck set and negative set regimes (b). Different values of E_A are obtained for the 2 failure regimes at small and large V_{stop}.

VII. Modeling of Endurance

To better understand the voltage-controlled N_C in Figs. 10 and 13, we extracted V_{stop} at constant N_C in the stuck-set and negative-set regimes in Fig. 13a. We considered 3 values of N_C, namely (a) for $N_C = 10^3$, in the stuck-set regime where N_C increases with V_{stop}, (b) $N_C = 5 \times 10^2$ in the negative-set regime where N_C decreases with V_{stop}, and (c) $N_C = 2 \times 10^4$ in the same regime. The extracted V_{stop} is shown in Fig. 13b as a function of t_P, thus allowing to assess the voltage-acceleration of endurance for different regimes. Voltage acceleration in Fig. 13 can be generally explained by a model where defect migration is activated by the local field and temperature [21], [26]. In this model, the local temperature T depends on V_{stop} according to the general Joule heating expression given by [21], [29]:

$$T = T_0 + \frac{V_{stop}^2}{8\rho k_{th}} = T_0 + \alpha V_{stop}^2, \tag{1}$$

where T_0 is the room temperature, ρ is the effective electrical resistivity, k_{th} is the effective thermal conductivity and α is equal to $(8\rho k_{th})^{-1}$. According to the Arrhenius model, the time t_P for completing a certain process is controlled by the local temperature T by:

$$t_P = t_0 e^{\frac{E_A}{kT}}, \tag{2}$$

where t_0 is a characteristic constant and E_A is the energy barrier for the specific process described by t_P, *e.g.*, defect migration during reset or defect injection during negative set.

Fig. 13b shows the calculated V_{stop} as a function of t_P based on Eqs. (1) and (2). For the stuck-set regime of the endurance curve, where the device is in LRS, we used α = 434 K/V^2, that is the value typically used for a continuous CF. For the negative set regime of the endurance curve, where the failure is due to a defects injection from the bottom electrode, we used α = 27 K/V^2, which describes instead a discontinuous CF since negative set generally takes place after reset transition (see Figs. 6b and 7c). The different values of α can be understood by the additional contribution to k_{th} in the insulating gap in the interrupted CF [26], which makes the product ρk_{th} larger for the negative set, compared to the stuck set condition. Different values of E_A where used in the calculations of Fig. 13b, namely, E_A = 1.8 eV for the stuck-set regime and E_A = 3.1 eV for the negative set regime. Note that E_A = 1.8 eV is comparable to the value used for calculating defect migration during set and reset [21], [25]. This is consistent with the stuck set condition, which describes the minimum t_P needed to complete the reset transition in the device. On the other hand, the larger E_A used for the negative set process can be understood by the stable nature of the BE interface featuring no OEL, thus resulting in a relatively high barrier for defect injection during negative set.

To quantitatively account for voltage-controlled endurance in Fig. 13, we introduced an Arrhenius-based degradation function f_d, describing the device degradation during a single cycle and given by:

$$f_d = \int e^{-\frac{E_A}{kT}} dt, \tag{3}$$

where E_A = 3.1 eV, T is the local temperature given by Eq. (1), and the integral is done over one set/reset cycle. Fig. 14a shows the measured N_C taken from Fig. 13a, plotted as a function of the calculated f_d assuming E_A = 3.1 eV. All data fall on the same universal line on the log-log scale, indicating that the degradation function f_d can provide a quantitative description of degradation after cycling. In the Arrhenius model of Eq. (3), failure occurs when the f_d calculated over all the cycles reaches a threshold value $f_{d,th}$. Therefore, the maximum number of cycles can be obtained by:

$$N_{C,max} = \frac{f_{d,th}}{f_d}, \tag{4}$$

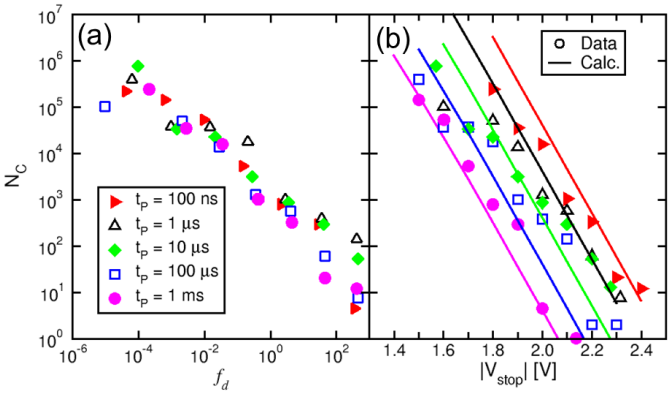

Fig. 14. Measured N_C as a function of the degradation function f_d from Eq. (3), and measured and calculated N_C as a function of V_{stop} (b). Data display a universal behavior in (a), supporting the validity of f_d as a quantitative description of cycling degradation.

where cycling endurance is calculated as the ratio of the threshold degradation divided by the single-cycle degradation in Eq. (3). Fig. 14b shows the measured and calculated N_C for different V_{stop} and t_P. The calculations, obtained with Eq. (4), show a good agreement with data, which further confirms the proposed Arrhenius model for cycling degradation and endurance failure. The model can be used for predicting endurance failure at variable voltage, pulse-width and pulse-shape, *e.g.*, rectangular pulse and variable set/reset ratio.

VIII. Conclusions

We studied switching variability and endurance under pulsed operation in RRAM device. We show that V_{stop} is a key parameter which controls resistance window, switching variability and endurance. Increasing V_{stop} improves resistance window and switching variability while degrading cycling endurance. Endurance failure is induced by negative set, namely a defect injection from the BE, which cannot be recovered by multiple reset pulses. Increasing $|V_{stop}|$ results in a shorter cycling as a result of a stronger probability for negative set. An Arrhenius model is finally introduced to predict V_{stop}-controlled endurance at variable pulse width t_P.

References

[1] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, and M. Tsai, "Evidence and solution of over-reset problem for HfO_x based resistive memory with sub-ns switching speed and high endurance," in *IEDM Tech. Dig.*, 2010, pp. 460–463.

[2] M. D. Pickett and R. S. Williams, "Sub-100 fJ and sub-nanosecond thermally driven threshold switching in niobium oxide crosspoint nanodevices," *Nanotechnology*, vol. 23, p. 215202, 2012.

[3] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, and D. J. Wouters, "Control of filament size and reduction of reset current below 10 μa in NiO resistance switching memories," *Solid State Electronics*, vol. 58, pp. 42–47, 2011.

[4] B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, "10x10 nm^2 Hf/HfO_x crossbar resistive RAM with excellent performance, reliability and low-energy operation," *IEDM Tech. Dig.*, pp. 31–34, 2011.

[5] H. S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. Chen, and M.-J. Tsai, "Metal-oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, June 2012.

[6] S. Sills, S. Yasuda, J. Strand, A. Calderoni, K. Aratani, A. Johnson, and N. Ramaswamy, "A copper ReRAM cell for storage class memory applications," *IEEE VLSI-Technology Tech. Dig.*, pp. 1–2, 2014.

[7] S. Balatti, S. Ambrogio, D. C. Gilmer, and D. Ielmini, "Set variability and failure induced by complementary switching in bipolar RRAM," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 861–863, 2013.

[8] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO_x resistive-switching memory (RRAM): Part I - Set/Reset variability," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2912–2919, Aug 2014.

[9] A. Fantini, L. Goux, R. Degraeve, D. J. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y.-Y. Chen, B. Govoreanu, and M. Jurczak, "Intrinsic switching variability in HfO_2 RRAM," *International Memory Workshop IMW*, pp. 30–33, 2013.

[10] W.-C. Luo, J.-C. Liu, Y.-C. Lin, C.-L. Lo, J.-J. Huang, K.-L., Lin, and T.-H. Hou, "Statistical model and rapid prediction of RRAM SET speed−disturb dilemma," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3760–3766, 2013.

[11] X. Guan, S. Yu, and H.-S. P. Wong, "On the switching parameter variation of metal-oxide RRAM-Part I: Physical modeling and simulation methodology," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1172–1182, 2012.

[12] P. Huang, B. Chen, Y. Wang, F. Zhang, L. Shen, R. Liu, L. Zeng, G. Du, X. Zhang, B. Gao, J. Kang, X. Liu, X. Wang, B. Weng, Y. Tang, G.-Q. Lo, and D.-L. Kwong, "Analytic model of endurance degradation and its practical applications for operation scheme optimization in metal oxide based RRAM," *IEEE IEDM Tech. Dig.*, pp. 597–600, 2013.

[13] Y. Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. S. Kar, D. J. Wouters, G. Groeseneken, J. A. Kittl, M. Jurczak, and L. Altimime, "Balancing SET/RESET pulse for > 10^{10} endurance in HfO_2/Hf 1T1R bipolar RRAM," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3243–3249, 2012.

[14] C. Chen, L. Goux, A. Fantini, A. Redolfi, S. Clima, R. Degraeve, Y. Chen, G. Groeseneken, and M. Jurczak, "Understanding the impact of programming pulses and electrode materials on the endurance properties of scaled Ta_2O_5 RRAM cells," *IEDM*, pp. 355–358, 2014.

[15] S. Deora, G. Bersuker, M. Sung, D. Gilmer, P. Kirsch, H.-F. Li, H. Chong, and S. Gausepohl, "Statistical assessment of endurance degradation in high and low resistive states of the HfO_2-based RRAM," *Reliability Physics Symposium (IRPS), 2013 IEEE International*, pp. MY.2.1–MY.2.5, April 2013.

[16] H. Chung-Wei, I.-T. Wang, C.-L. Lo, M.-C. Chiang, W.-Y. Jang, C.-H. Lin, and T.-H. Hou, "Self-rectifying bipolar TaO_x/TiO_2 RRAM with superior endurance over 10^{12} cycles for 3D high-density storage-class memory," in *VLSI Technology (VLSIT), 2013 Symposium on*, June 2013, pp. T166–T167.

[17] H. Lv, X. Xu, H. Liu, R. Liu, Q. Liu, W. Banerjee, H. Sun, S. Long, L. Li, and M. Liu, "Evolution of conductive filament and its impact on reliability issues in oxide-electrolyte based resistive random access memory." *Scientific Reports*, no. 7764, pp. 1–6, 2014.

[18] A. Calderoni, S. Sills, and N. Ramaswamy, "Performance comparison of O-based and Cu-based ReRAM for high-density applications," in *Memory Workshop (IMW),* 2014 *IEEE* 6*th International*, May 2014, pp. 1–4.

[19] S. Balatti, S. Ambrogio, Z.-Q. Wang, S. Sills, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Pulsed cycling operation and endurance failure of metal-oxide resistive (RRAM)," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, Dec 2014, pp. 14.3.1–14.3.4.

[20] S. Ambrogio, S. Balatti, S. Choi, and D. Ielmini, "Impact of the mechanical stress on switching characteristics of electrochemical resistive memory," *Adv. Mater.*, vol. 26, no. 23, pp. 3885–3892, 2014.

[21] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," *IEEE Trans. Electron Devices*, vol. 58, pp. 4309–4317, 2011.

[22] S. Koveshnikov, K. Matthews, K. Min, D. Gilmer, M. Sung, S. Deora, H. Li, S. Gausepohl, P. Kirsch, and R. Jammy, "Real-time study of switching kinetics in integrated 1T/ HfO_x 1R RRAM: Intrinsic tunability of set/reset voltage and trade-off with switching time," *IEEE IEDM Tech. Dig.*, pp. 486–488, Dec 2012.

[23] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiO_x brought about by reducing a parasitic capacitance," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033506, 2008.

[24] T. Sakamoto, M. Tada, M. Miyamura, N. Banno, K. Okamoto, N. Iguchi, and H. Hada, "Impact of overshoot current on set operation of atom switch," *Jpn. J. Appl. Phys.*, vol. 53, pp. 04ED071–04ED073, 2014.

[25] S. Ambrogio, S. Balatti, D. Gilmer, and D. Ielmini, "Analytical modeling of oxide-based bipolar resistive memories and complementary resistive switches," *Electron Devices, IEEE Transactions on*, vol. 61, no. 7, pp. 2378–2386, July 2014.

[26] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM - Part II: Modeling," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2468–2475, 2012.

[27] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive switching by voltage-driven ion migration in bipolar RRAM - Part I: Experimental study," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2461–2467, 2012.

[28] D. Ielmini, F. Nardi, and S. Balatti, "Evidence for voltage driven set/reset processes in bipolar switching RRAM," *IEEE Trans. Electron Device*, vol. 59, pp. 2049–2056, 2012.

[29] D. Ielmini, F. Nardi, and C. Cagli, "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories," *Nanotechnology*, vol. 22, no. 25, p. 254022, 2011.