# A low-power CMOS ASIC for X-ray Silicon Drift Detectors low-noise pulse processing

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## 1 Introduction

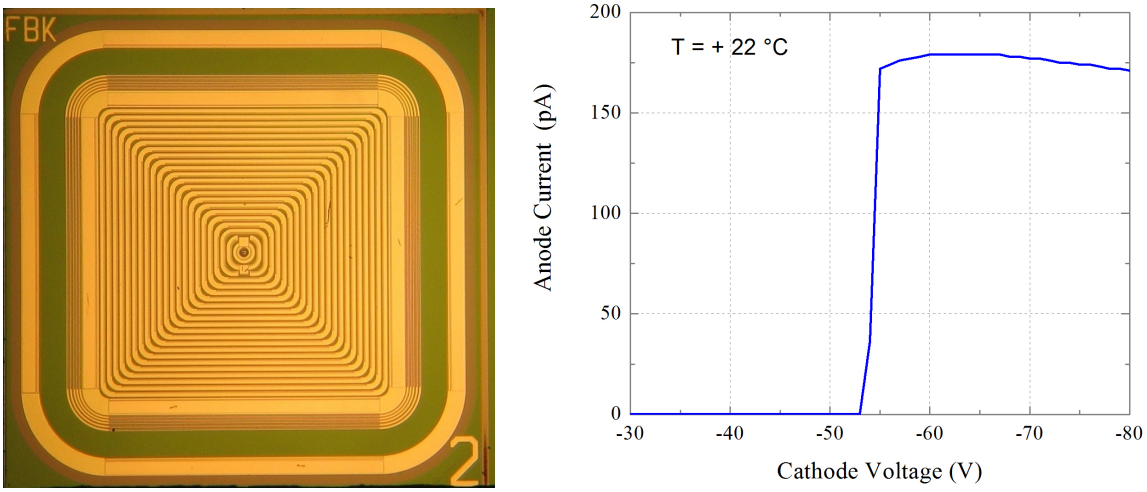
The study and the development of Silicon Drift Detectors (SDDs) for high-resolution X-ray spectroscopy is a subject of research and growing interest [1–3]. The development of the SDDs technology, since its invention by Gatti and Rehak [4], made it possible to achieve high resolution X-ray spectroscopy and imaging because of their small read-out anode geometry and therefore their anode capacitance, which leads to reduction of the series noise contribution of the electronics in the detection system. Besides, the low anode current of the SDDs, attainable at temperatures below $-20^{\circ}$C, makes it possible to achieve a very low noise detection system by keeping the parallel noise component at low levels. However, the achievable performance depends both on the quality of the detector as on the performance of the Front-End Electronics (FEE). Therefore, a proper design of the FEE circuit, based on Application Specific Integrated Circuit (ASIC), is required to achieve high-resolution spectroscopy.

In this paper we present the measurement results of a low-noise low-power Application Specific Integrated Circuit (ASIC), called VEGA-1, designed and optimized for analog pulse processing of signals from SDDs using the minimum possible electrical power, as required for application in space missions with detectors having several thousands of acquisition channels.

The specifications of the ASIC are described in section 2 . The SDD is described in the section 3. Section 4 presents a brief description about the VEGA-1 ASIC. The experimental results are presented in section 5, and section 6 concludes the paper.

## 2 Specifications of the VEGA-1 ASIC

VEGA-1 was designed to fulfil all the requirements for reading out large-area multi-anode linear monolithic SDDs for X-Ray spectroscopy and imaging in an energy range from 500 eV to 60 keV. The required energy resolution is better than 260 eV FWHM at 6 keV, corresponding to an Equivalent Noise Charge (ENC) of FEE/detector system lower than 27 electrons r.m.s.. The reference




(a) (b)

**Figure 1**. The 10 mm$^2$ FBK quad-SDD. (a) Back (Anode) side of the SDD. (b) Readout anode leakage current at 22°C: the SDD is fully depleted at a bias voltage lower than −55 V.

SDDs for which VEGA-1 has been designed are 450 $\mu$m thick, with an effective area of 76 cm$^2$ read out by two rows of 112 anodes with a pitch of 970 $\mu$m and an anode capacitance of about 350 fF. A detailed description of this detector, designed for the LOFT mission [5, 6], can be found in [7]. The aforementioned SDDs have a nominal anode current of about 0.7 pA at −32°C, but the value can increase up to 10 pA at the end of their life due to the radiation damage in the space mission. The detector is presently under construction but its potentialities have been demonstrated in previous prototypes [8]. The FEE must have less than 500 $\mu$W total power consumption per channel in order to be suitable for its use in systems with a very large number of channels ($0.5 \times 10^6$); at the same time, it shall accomplish all functionalities and requirements of an ADC-ready ASIC devoted to high-time-resolution X-ray spectroscopy.

## 3 The Q10 Silicon Drift Detector

The detector used for the measurements is a square SDD — named Q10-SDD — with a thickness of 450 $\mu$m and an effective area of 10 mm$^2$. The back (Anode) side of the detector is shown in figure 1 (a). A small $n^+$ pad in the detector center forms the read-out anode. An integrated voltage divider is implemented in the SDD in order to generate the proper biasing potentials for the cathodes and consequently forming the drift field. The innermost drift cathode, which is biased at a separate voltage, shields the anode from the noise of the drift cathode chain. The front (P) side of the SDD is a uniform $p^+$ implant constituting the entrance window for the radiation. The detector, designed at INFN, has been fabricated at FBK in Trento [9]. Figure 1(b) shows the measured readout anode leakage current of the aforementioned SDD as a function of the back side voltage, while the front side was left floating. By increasing the bias voltage of the outmost cathode, the depleted volume advances from the back side to the front side, and reaches the front

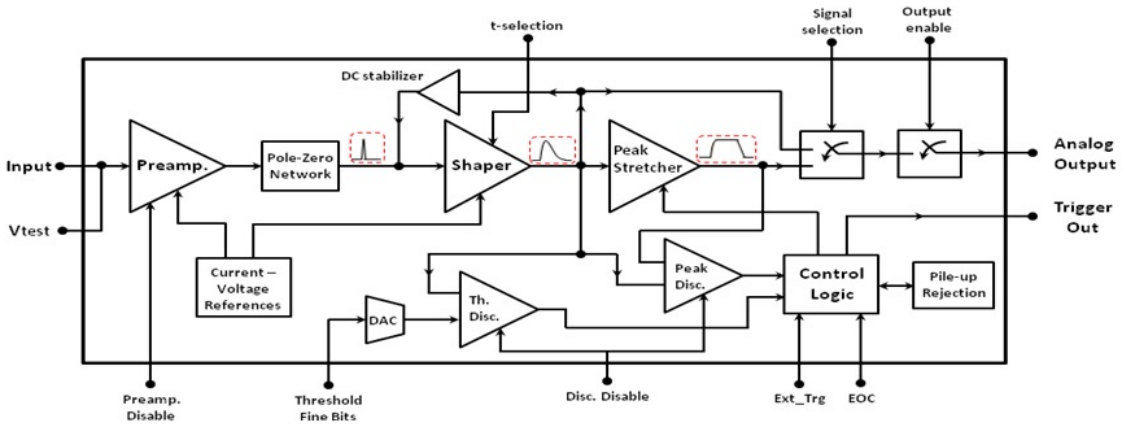



**Figure 2**. Block diagram of the read out FEE circuit.

side at $V_{\text{bias}} = -55\,\text{V}$. The measured anode current is about 180 pA at $+22^{\circ}\text{C}$ when the SDD is fully depleted, which corresponds to a current density of $1.8\,\text{nA/cm}^2$.

## 4 The VEGA-1 ASIC

The VEGA-1 ASIC has been designed in 0.35-$\mu$m CMOS Technology and manufactured at Austriamicrosystems [10]. This technology offers four metal layers, two polysilicon layers and high-resistive poly ($1.2\,\text{k}\Omega/\square$), thus allowing the required integration density. The low-noise characteristics of the MOSFETs in this technology have been studied and proved in previous works [11, 12].

Figure 2 shows the block diagram of the VEGA-1 ASIC, consisting of an analog and a digital/mixed-signal section. The analog section includes a low-noise charge sensitive preamplifier, a RC-CR shaper with digitally selectable shaping times from 1.6 $\mu$s to 6.6 $\mu$s, and a peak stretcher/sample-and-hold circuit. The digital/mixed-signal section includes an amplitude discriminator with coarse and fine threshold level settings, and a peak discriminator. A logic circuit performs pile-up rejection, signal sampling, trigger generation, channel reset, and controls the ASIC configuration, including the possibility to disable the preamplifier and the discriminator. The VEGA-1 has been designed and manufactured in single and 32-channel versions with dimensions of $200\,\mu\text{m} \times 500\,\mu\text{m}$ per channel. Full details on the design and the functionalities of the VEGA-1 ASIC are presented in [13].

## 5 Experimental results

A photograph of the VEGA-1 bonded to the Q10-SDD is shown in figure 3. The ASIC is placed on top of the SDD in order to minimize the distance between the input pad of the ASIC and the anode of the SDD, thus minimizing the stray capacitances at the ASIC input: in this way the series noise contribution can be kept as low as possible. A kapton foil separates the ASIC back contact from the SDD for electrical isolation.

The VEGA-1 ASIC, together with the Q10-SDD, has been placed in a thermostatic chamber and tested with $^{55}$Fe and $^{241}$Am radiation sources at $-30^{\circ}\text{C}$. Figure 4 shows the shaper output

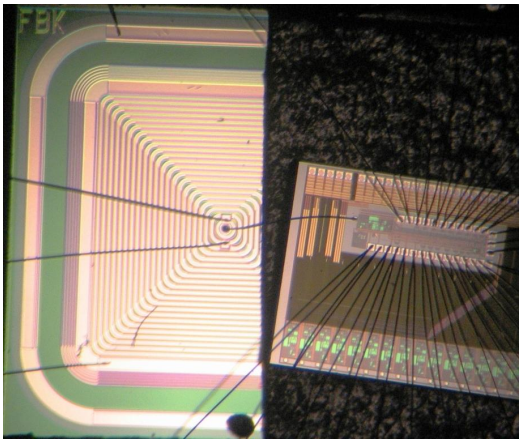



**Figure 3**. Photograph of the VEGA-1 ASIC bonded to the 10 mm$^2$ FBK SDD. A kapton foil separates the ASIC from the SDD.

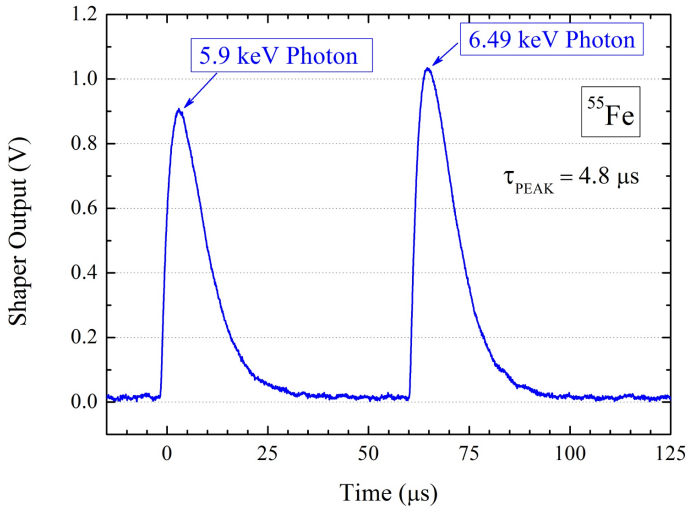



**Figure 4**. Measured shaper output with SDD of 10 mm$^2$ at $-30$°C and 4.8 $\mu$s peaking time. The two peaks correspond to 5.9 keV and 6.49 keV photon energies of $^{55}$Fe radiation source.

signal resulting from the acquisition of two photons at 5.9 keV and 6.49 keV from $^{55}$Fe. Since the ASIC has a dynamic range of 60 keV, a very low-noise amplifier has been used at the output of the ASIC in order to amplify the signal by a factor of 10 and monitor it on the oscilloscope operating in single shot triggering mode. This acquisition highlights the high signal to noise ratio of the system.

Figure 5 shows the $^{55}$Fe spectrum acquired at $-30$°C and 3.6 $\mu$s peaking time. The pulser is set at 450 eV and the measured energy resolution is 140 eV FWHM, corresponding to an ENC of 16 electrons r.m.s.. The line width of the $^{55}$Fe Mn K$_\alpha$ line is 185 eV FWHM, well below the upper limit of 260 eV required by the project specifications, although the LOFT SDD has a larger anode capacitance and so a higher noise is expected.

Figure 6(a) shows the $^{241}$Am spectrum acquired at $-30$°C and 3.6 $\mu$s peaking time. In this measurement, the pulser is set at 500 eV and has a measured line width of 163 eV FWHM. Figure 6(b) shows the $^{241}$Am spectrum of figure 6(a) in more details. As it can be seen, all important

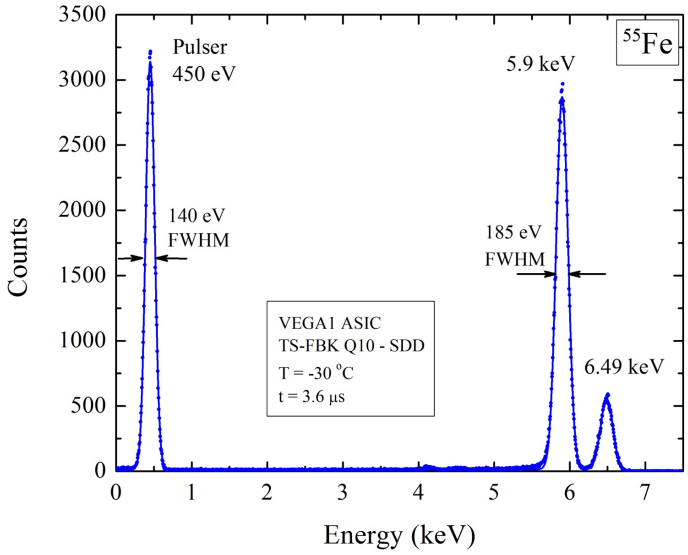



**Figure 5**. $^{55}$Fe spectrum acquired with SDD of 10 mm$^2$ at $-30$°C and 3.6 $\mu$s peaking time. The measured energy resolution of the pulser is 140 eV FWHM, corresponding to the ENC of 16 electrons r.m.s. .

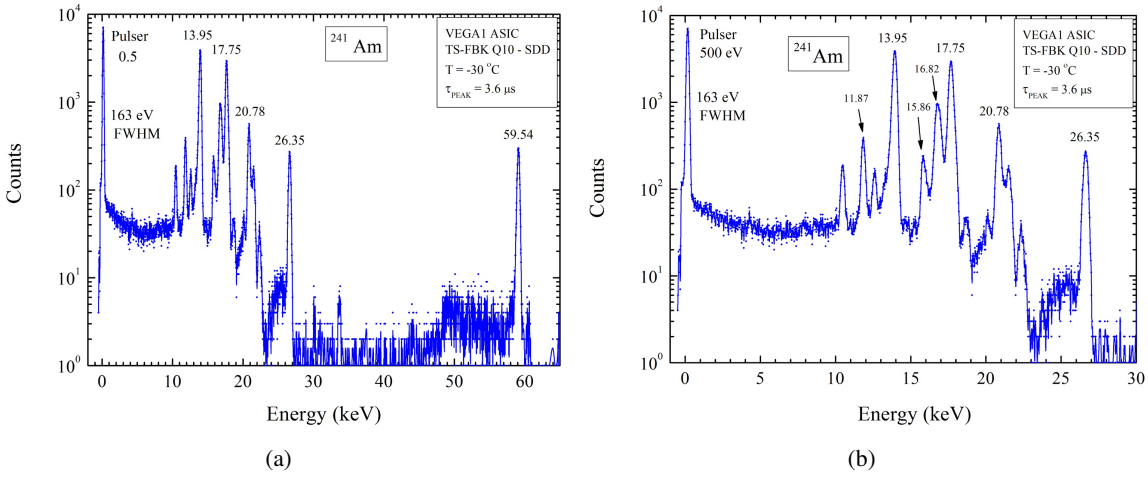



**Figure 6**. $^{241}$Am spectrum acquired with SDD of 10 mm$^2$ at $-30$°C and 3.6 $\mu$s peaking time. An energy resolution of 163 eV FWHM is measured on the pulser line. (a) The acquired $^{241}$Am spectrum up to 60 keV. (b) Focus of the spectrum of the left figure up to 30 keV.

energy lines of $^{241}$Am are completely visible. An energy resolution of about 262 eV FWHM is measured at the 13.95 keV line of $^{241}$Am. This measurement also proves the required operative energy range (500 eV to 60 keV) of the VEGA-1 ASIC.

Figure 7 shows the measured linearity and linearity error determined from the mono-energetic lines of the $^{241}$Am spectrum of figure 6(a), deriving a linearity error between $-0.7\%$ and $+1\%$ in the 13–59 keV energy range.

Figure 8 shows the comparison between the measured ENC of the VEGA-1 ASIC without and with the detector connected. A minimum ENC of 16 electrons r.m.s. (equivalent to 140 eV FWHM)

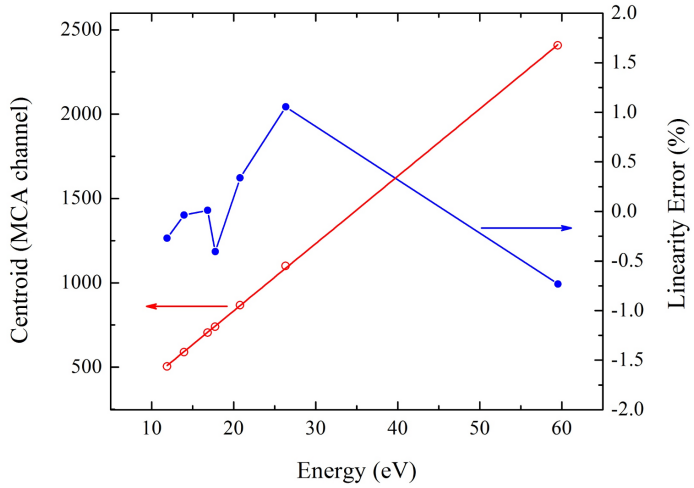



**Figure 7**. Measured linearity (red) and linearity error (blue) of the whole FEE circuit loaded with 10 mm$^2$ FBK quad SDD for $^{241}$Am spectrum of figure 7 at 3.6 $\mu$s peaking time and $-30$°C.

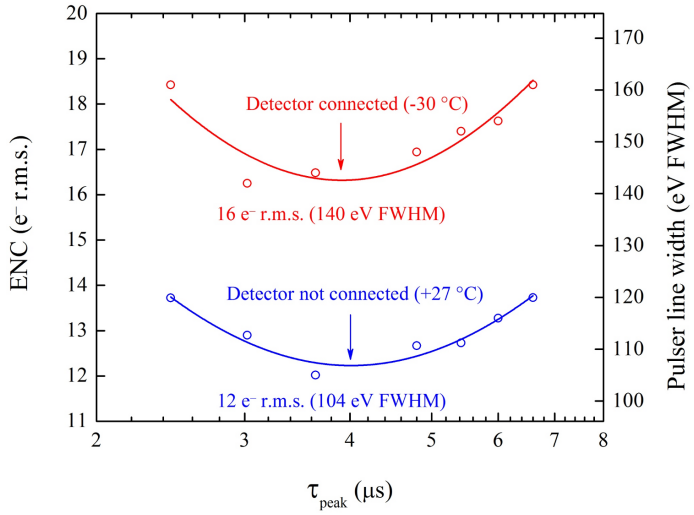



**Figure 8**. The measured noise of the FEE circuit before (blue line) and after (red line) bonding to the detector. A minimum intrinsic ENC of about 12 electrons r.m.s. at 3.6 $\mu$s shaping time and +27°C is measured for the FEE. A minimum ENC of about 16 electrons r.m.s. at 3.0 $\mu$s shaping time and $-30$°C is measured for the FEE bonded to the 10 mm$^2$ FBK quad SDD.

is measured at $-30$°C and 3.0 $\mu$s peaking time when the FEE input is connected to the SDD; whereas, the measured minimum intrinsic noise of the ASIC without detector is 12 electrons r.m.s. (equivalent to 104 eV FWHM), at 3.6 $\mu$s peaking time and room temperature. The noise increment is due to the additional capacitance at the input of the ASIC (due to the anode capacitance of the SDD and the stray capacitance), as well as the leakage current of the detector.

A total power consumption of 482 $\mu$W is measured for the single channel version of VEGA-1 ASIC. Since the implemented current/voltage references circuit is common to all the 32 channels in the multi-channel version, a total power consumption of about 420 $\mu$W per channel is expected for the 32-channel version.

**Table 1**. VEGA-1 ASIC and Quad-SDD features.

| *Parameter* | *Value* |
|---|---|
| Technology | AMS 0.35 $\mu$s CMOS C35B4C3 |
| Input charge | Negative |
| Dynamic range | 500 eV–60 keV |
| Pulse shaping | CR-RC |
| Shaping times | 1.6 $\mu$s to 6.6 $\mu$s (3 bits selectable) |
| Linearity error | from $-0.7\%$ to $1\%$ |
| ENC (intrinsic, $T = +27^{\circ}$C) | 12 electrons r.m.s. (without detector) |
| ENC (intrinsic, $T = -30^{\circ}$C) | 16 electrons r.m.s. (with detector) |
| Voltage supplies (Analog) | +3.3 V, +2 V |
| Voltage supplies (Digital) | +3.3 V |
| Power consumption | 482 $\mu$W (single channel version)<br>420 $\mu$W/ch (32 channel version) |
| SDD active area | 10 mm$^2$ |
| SDD thickness | 450 $\mu$m |
| $I_{\mathrm{ANODE}}$ | $\sim$ 180 pA @ $+22^{\circ}$C |

Table 1 summarizes the main experimental results of the VEGA-1 ASIC and also the characteristics of the Q10-SDD.

## 6 Conclusion

We have presented the experimental test of the VEGA-1 ASIC designed and manufactured for pulse processing of signals coming from monolithic silicon drift detectors. VEGA-1 performs high-resolution X-ray spectroscopy and imaging in the energy range from 500 eV to 60 keV with very low power consumption. A minimum ENC of 16 electrons r.m.s. at 3.0 $\mu$s peaking time and $-30^{\circ}$C is measured when connected to a 10 mm$^2$ Q10-SDD while the minimum intrinsic (without detector) ENC is 12 electrons r.m.s. at 3.6 $\mu$s peaking time and room temperature. A total power consumption of 482 $\mu$W is measured in the single channel version of the ASIC, and about 420 $\mu$W per channel is expected in the 32-channel version.

## Acknowledgments

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