Dual Channel Time-to-Digital Converter Module with 10 ps resolution and 320 ns full scale range

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We present a dual-channel Time-to-Digital Converter (TDC) module designed to accurately measure time intervals with 10 ps resolution, about 21 ps rms precision and 125 fs rms differential non-linearity, over a 320 ns full scale range and up to 4 Mconv/s per channel. The module can also operate the two channels in parallel, as a single TDC converter, in order to improve timing performance to about 15.3 ps rms. An USB 2.0 interface provides power supply and allows fast data transfer to a computer, where a dedicated software interface handles measurement data and plots. Thanks to excellent timing performance, compact dimensions and low power consumption, the dual channel TDC module is suitable for advanced multi-channel time measurements at the picosecond level.

Introduction: Many applications in life-science and medical research, such as Fluorescence Lifetime Imaging Microscopy (FLIM) and Diffuse Optical Tomography (DOT) make use of Time-Correlated Single-Photon Counting (TCSPC) techniques [1] as powerful tools for the reconstruction of fast, low intensity and repetitive optical waveforms. TCSPC technique consist of detecting and measuring the photons arrival time: after many acquisition, the histogram of these arrival times provides the optical waveform of interest, with picosecond resolution with no need of expensive hundreds of GHz bandwidth electronics.

TCSPC techniques exploit single-photon sensitivity photodetectors, such as photomultipliers tubes (PMT), micro-channel plates (MCP) or single-photon avalanche diodes (SPADs) [2]. However other applications, not just related to photo detection, require the accurate measurement of time-interval, down to the picosecond level, and even in a multi-channel approach, like [3].

For all those applications, extremely precise time measurement instrumentation must provide picosecond resolution with a very low Differential Non-Linearity (just a few percent of the LSB time-bin). State-of-the-art time measurement instrument [4] make use of Time-to-Amplitude Converters (TACs) to perform time-interval measurements by means of an intermediate conversion into an analogue voltage before obtaining the digital code through an Analog-to-Digital Converter (ADC). Instead, Time-to-Digital Converters (TDCs) perform a direct conversion of time-intervals into digital code; recent improvements in their linearity make these device a valid alternative to TACs, above all when multi-channel instrumentation is a must.

In this letter we present a novel electronic instrument, namely a dual-channel time measurement system with 10 ps resolution (i.e. Least Significant Bit, LSB) over a 320 ns full scale range (FSR) with a DNL better than 1.5 % LSB rms. These performance make the module the best candidate for low-consumption, high performance, low-cost, compact, multi-channel timing instrumentation.

Module architecture: The Dual channel module is shown in Fig. 1 and has 85 mm x 60 mm x 60 mm dimensions and employs six SMA connectors for the input signals that define the time intervals to be measured. An USB B plug allows to upload measurements to a remote PC and provides the necessary power supply (hence the power plug is not used). The core component of the module is an application-specific integrated TDC circuit, fabricated in a 0.35 µm CMOS technology [5], which is fed by two independent inputs, namely a START and a STOP pulse and provides a 15 bit output bus. The chip requires a 100 MHz reference clock with high stability and low jitter, in order to perform precise conversions..

A single printed circuit board TDC-Card [6] hosts the TDC chip, the input signals front-end circuitry and the logics needed for data acquisition and pre-processing. The total power consumption is less than 400 mW at the maximum conversion ratio of 4 Mconv/s. As shown in Fig. 2, the Dual channel TDC module is composed by four boards: two independent TDC-Cards, a data processing board, and a main board for power supplies and two further independent input channels.

The main board generates the necessary +3.6 V, +2.1V and -3.3 V from the 5 V provided by the USB connection, by means of high efficiency DC/DC converters. Their output noise is filtered to reject supply disturbance responsible of time jitter performance degradation, using linear regulators (which provide the standard +3.3V, +1.8 V and -3V to the TDC-Card) and proper decoupling capacitors. The main board provides two further SMA connectors for an extra couple of START/STOP signals (called common channel inputs) and the corresponding signal-conditioning front-end electronics, identical to the one used in the TDC-Card. Eventually, two separate Altera MAX V CPLDs (one for the START and other one for the STOP path, in order to minimize electrical crosstalk) provide these START/STOP signals to the TDC-Card in according to the proper selection signals.

Each TDC-Card has two SMA connectors, for START and STOP input signal, and a front-end circuitry to convert any kind of input pulses into a standard 3.3 V LVCMOS signals, by means of an ultra-fast low-jitter CMOS comparator (LT1711 by Linear Technology) for each input and a dual channel 12 bit resolution DAC (AD5627R by Analog Devices) for setting the input reference voltages. A first CPLD receives the START/STOP pulses provided both by the local board and those by the main board: a proper logics selects the desired START and STOP pulses and the respective synchronism edges that define the time interval to measure, according to the dedicated control signals. This CPLD feeds the selected START/STOP signals to the TDC chip. A second CPLD handles TDC control signals, performs data readout, and provides the time measurement result on the output bus after a pre-elaboration process. This CPLD provides also the information on conversion rates and valid START/STOP via an independent serial SPI interface.

front *back*

Fig. 1 *Dual Channel TDC module's frontside, with SMA input (START and STOP) connectors for the two independent channels, and backside, with additional SMA input connectors for the common channel and the USB plug for data upload to a PC. The power supply plug is not needed when the USB is plugged in.*

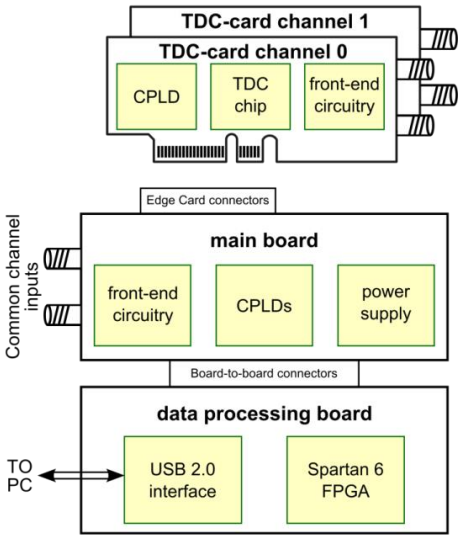

Fig. 2 *Dual Channel TDC module architecture: two TDC-Card are connected to the main board, containing power supply generators and the common channels signal conditioning. The data processing board processes and uploads data to a remote PC, via the USB 2.0 interface.*

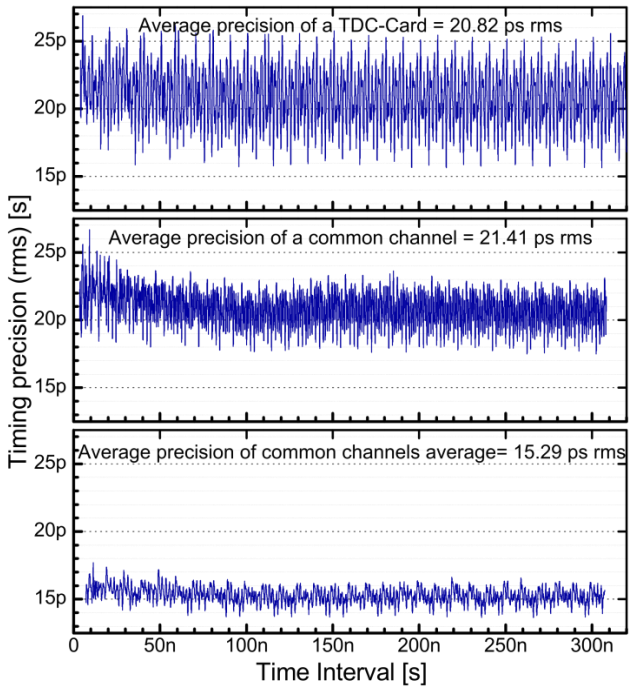

Fig. 3 *Timing precision of the TDC-Card (top), when using the module common channel input (center) and the average of the two, when the TDC-Cards are running in parallel (bottom).*

The data processing board is based on a Spartan 6 FPGA and a dedicated USB 2.0 high-speed controller. The FPGA process the two TDC-Card 15 bits results, in order to generate the time arrival histograms of the two independent measurement channels, with 320 ns full scale range (FSR) and 10 ps resolution (LSB). The FPGA can also compute a single histogram, when the two TDC-Cards are run in parallel, with the same START and STOP pulses via the common channel inputs, in order to average the two conversions, thus improving resolution, precision and accuracy. Eventually data are sent to the host PC via the USB controller and a Labview software interface plots the histograms.

Experimental results: We performed an in-depth characterization of the module for assessing timing precision, differential non-linearity, maximum conversion rate and power consumption.

Since the time histograms are computed and stored inside the FPGA, the total data transfer to the host PC is drastically reduced compared to the total amount of conversions. In this way the module allows each TDC-Card to convert up to its maximum conversion rate (about 4 Mconv/s) and the software interface is able to plot measurement results in real time. The total power consumption in less than 1.2 W at the maximum conversion rate, so the module can be supplied by the USB plug.

Concerning timing measurements, we compared the overall module performance to those of the single TDC-Card [6]. Fig. 3 shows the module timing precision along the overall 320 ns FSR: measurements performed by a single channel when using the common SMA input (Fig. 3 center) show timing precision of 21.41 ps rms, just slightly a minor worse than the 20.82 ps rms of one TDC-Card alone (Fig. 3 top). This is due to the presence of more components in the common channel signals path, resulting in a slightly higher time jitter. We also measured the timing performance using the common channel to provide the same time interval to both TDC-Cards and then to average the results in order to improve resolution. In this case (Fig. 3, bottom), the timing precision is about 15.29 ps rms with an 1.4 improvement factor, in according to the maximum theoretical improvement of $\sqrt{2}$.

Finally, we compared DNL, by means of a code density test. Fig. 4 shows a worsening in the non-linearity performance when the TDC-Card measures time intervals through the common channel inputs (see Fig. 4 top in respect to Fig. 4 bottom). As can be seen, electrical cross-talk between START and STOP common signals impacts the first 35 ns of the full scale range. Even the non-linearity of the averaged measurements is the same of the one measured with the single common channel input, because electrical crosstalk in the main board affect both paths in the same way, hence the average of the two TDC-card result cannot improve DNL performance.

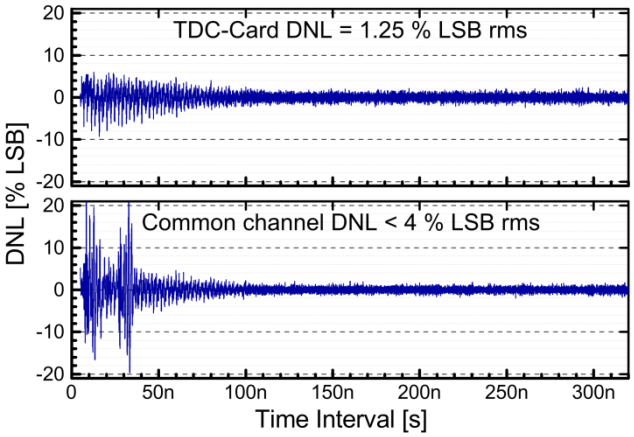

Fig. 4 *DNL of the TDC-Card (top) and the same TDC-Card using the module common channel input (bottom).*

Conclusion: We presented a novel electronic module able to perform two independent time-interval measurements by means of two TDC-Cards with less than 1.2 W total power consumption. This module, thanks to the 21 ps rms precision and 125 fs rms differential non-linearity over the whole 320 ns full scale range, with up to 4 Mconv/s per channel, plus the compact dimensions and the low power consumption, enables a large number of advanced application where multi-channel accurate time-measurements are required at the picosecond level.

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