Integrated Circuit for Sub-Nanosecond Gating of InGaAs/InP SPAD

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***Abstract*—We present a novel integrated circuit for sub-nanosecond gating of InGaAs/InP SPADs (Single-Photon Avalanche Diodes). It enables the detector in well-defined time intervals (longer than 500 ps) and strongly reduces the afterpulsing effect. It includes a fast pulser with rising/falling edge shorter than 300 ps (20% - 80%), a wide-band comparator and hold-off logic circuitry. The fast avalanche quenching reduces the charge flow in the SPAD, thus decreasing the afterpulsing, a detrimental effect that limits the maximum count rate of InGaAs/InP SPADs. The wide-band SiGe comparator guarantees very low timing jitter of the acquired waveforms: less than 100 ps (FWHM) at 5 V excess bias voltage, when operated with InGaAs/InP SPAD, whereas we estimate that the time jitter of the circuit is less than 30 ps.**

***Index Terms* — single-photon counting; single-photon detector, single-photon avalanche diode (SPAD); active quenching circuit; afterpulsing; InGaAs/InP SPAD.**

I. Introduction

The detection of very faint (down to the single-photon level) and fast (picosecond time scale) light signals in the near-infrared range is nowadays a key technology for many scientific experiments. Measurement of fluorescence decays (in physics, chemistry and biology) [1], single molecule detection, characterization of new materials, non-invasive testing of VLSI circuits [2], single-photon source characterization [3], fiber optics testing [4], laser ranging in space and telemetry [5], quantum cryptography [6], quantum computing and studies in quantum physics are among the most common applications.

Different kinds of single-photon detectors have been developed in the past, but only microelectronic detectors have the advantage of high reliability and robustness, and they can be very compact and portable. Single-Photon Avalanche Diodes (SPADs) proved to be a good choice because they have high photon detection efficiency and low timing jitter. Silicon SPADs are sensitive up to 1100 nm, while InGaAs/InP SPADs can be employed to detect photons from 900 nm to 1700 nm. Due to the low energy bandgap of the InGaAs absorbing layer and to high defect concentration in compound materials, these detectors suffer from high Dark Count Rate (DCR). In order to limit these spurious counts, this SPAD must be operated at low temperature, usually in the range 200 K – 250 K. Another unwanted noise source, particularly strong in InGaAs/InP SPAD, is afterpulsing: when an avalanche is triggered, strong current flows through the p-n junction, some carriers get trapped in deep levels and then are released after a delay [7]. Such detrapping is temperature dependent (slower at low temperature) and usually requires several tens of microseconds in standard operating conditions. A typical countermeasure is to operate InGaAs/InP SPADs in gated mode: the detector is enabled for a short time window (T_{ON}) synchronous with the optical waveform to be measured. The OFF period following an avalanche must be long enough to let the carriers be released, but this seriously reduces the maximum count rate. Afterpulsing can be mitigated by using a fast quenching circuit that reduces the amount of charge carriers flowing through the device, by lowering the bias voltage below the breakdown voltage as quickly as possible (less than 1 ns).

In order to accomplish these requirements and have a wide range of programmability for all the parameters (T_{ON}, bias voltage, temperature, etc.) to fit different applications, various photon-detection modules have been developed [8][9]. These detection systems are based on discrete components for both gate pulse generator and avalanche comparator: this approach guarantees very low timing jitter (the contribution from the front-end electronics is less than 10 ps), but they are power hungry and introduce stray capacitances and inductances that impair the quenching time. Several integrated Active Quenching Circuits (AQC) have been developed in the past, especially for silicon SPADs [10][11], but usually they operate in free-running mode and, when a gate is introduced, the timing jitter worsen. Fast gating and low timing jitter are usually in contrast because high-speed gating with sharp edges gives large feed through spikes at comparator input through the SPAD junction capacitance. With a simple single-ended front end circuit, a high threshold would be needed to avoid such spurious pulses and to detect only the avalanche ones, thus impairing timing performance [12]. Integrated solutions specifically designed for gating and quenching InGaAs/InP SPADs have been presented in literature, but the photons

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detected either during the rising edge or at the beginning of the gate are not correctly marked. In [13] the quench transistor at the SPAD anode is active during the gate opening in order to avoid false detections given by the capacitive feedthrough, but it also diverts the avalanche current from the readout path, impairing the detection of photons during gate rising-edge. Similarly, in Ref. [14][15] a masking circuit discards all the clicks in the first part of the gate. Recently gigahertz sinusoidal gating approaches have been widely exploited [16][17][18]: the afterpulsing is highly reduced since very short gate time - few hundreds of picoseconds - is employed. However, the quenching time and the gate time are bonded together and thus there is no flat sensitivity for at least several nanoseconds for reconstructing optical waveforms.

In this paper we present a new integrated circuit (in the followings, Fast-Gated Active Quenching Circuit, FG-AQC) that employs a differential sensing in order to reject gate coupling [12] and achieve very short quenching time, while keeping a fast gate pulser. Therefore, photons arriving during the rising and falling edges are properly detected with low timing jitter.

Internal circuitry of the AQC is detailed in Section 2, whilst Section 3 shows simulations and experimental measurements employing an InGaAs/InP SPAD with 25 µm active area diameter. Section 4 summarizes and concludes this paper.

II. Fast-Gated Circuit Architecture

The integrated circuit has four main blocks (see Fig. 1a): (i) pulser, with fast transition time (less than 300 ps) for SPAD gating; (ii) low-propagation delay differential SiGe comparator, with programmable threshold for avalanche sensing; (iii) hold-off logic, which masks gate inputs for keeping the SPAD OFF for a programmable time after each avalanche; (iv) low impedance output driver, with internal monostable.

The pulser receives the "GATE" signal and increases the SPAD bias voltage above the breakdown level during the ON time (T_{ON}) of the external gate signal. The SPAD cathode is biased at high voltage, V_{POL}, whereas its anode is driven by the FG-AQC through the M_P and M_N MOSFETs from 0 V to V_{PP}, where V_{PP} is the supply voltage of the high-voltage section (~ 5 V) of the chip. Therefore, SPAD excess bias voltage is $V_{EX} = V_{POL} - V_{BD}$, where V_{BD} is the SPAD breakdown voltage, and the undervoltage (i.e. the voltage drop below the breakdown level during the OFF time) is $V_{UV} = V_{PP} - V_{EX}$. The same gate signal is applied also to a "dummy" structure that is used to mimic the SPAD parasitics, but without having any avalanche. Such structure can be either a capacitor or, better, a structure very similar to the main SPAD, but with higher breakdown voltage, hence not able to detect photons.

A SiGe fast comparator senses the signal on R_S resistors and discriminates the small differential signal, due to the avalanche, from the common-mode feed-through signal, due to the gate. The output pulse from the comparator marks the arrival time of a single photon and feeds the following blocks:

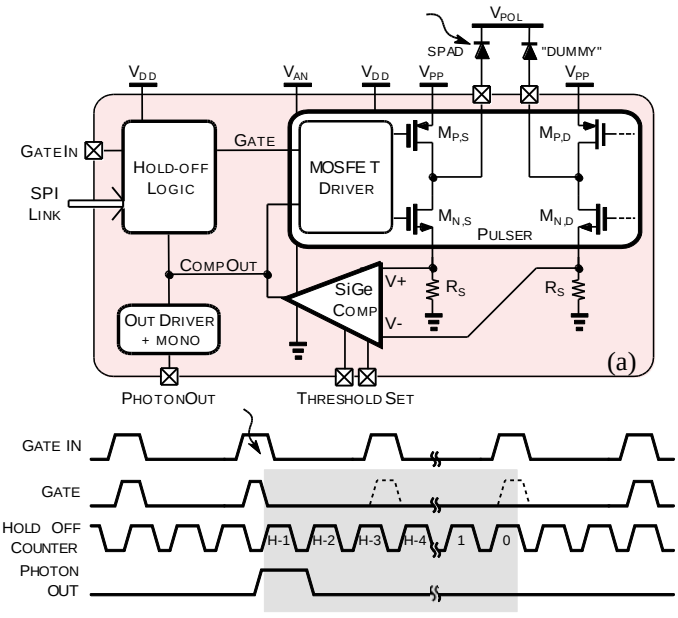

Fig. 1. (a) Block diagram of the fast-gated chip and its connections to the SPAD. (b) Timing diagram of the main signals of the integrated circuit: the SPAD is ON only when both the Gate IN signal is high and the hold-off is not active (outside the shadowed region). After each avalanche, a Photon Out pulse is output, the avalanche is quenched and the hold-off counter starts to measure the hold-off time interval (H periods of its reference clock).

(i) the pulser MOSFET driver, in order to quench the avalanche in the shortest time; (ii) the hold-off logic, in order to mask subsequent gate pulses; (iii) the output monostable, in order to output a fixed duration pulse through a high-current pin, able to drive 50 Ω loads. The comparator presents low-propagation delay thanks to the 0.35 µm SiGe BiCMOS technology we employed, where high-speed bipolar transistors (f_T up to 40 GHz), 3.3 V MOSFETs and 5 V MOSFETs are available.

The hold-off logic keeps the SPAD quenched for a programmable time in order to limit the afterpulsing effect. It stops the "GATE IN" signal during the hold-off time after each avalanche (see Fig. 1b). Therefore, a high-repetition-rate gate signal can be used without having strong afterpulsing.

Overall dimensions of the core of the chip are 100 µm × 370 µm. This elongated shape makes it possible to design narrow pitch linear arrays with fast-gated SPADs and all the electronics on the side. The power consumption is around 30 mW even at high-count rate (gate frequency = 100 MHz, output count rate ~ 1 Mcps).

A. Current Sensing and High Speed Comparator

The purpose of this part of the circuit is to sense the SPAD current and output a digital pulse. The comparator has four stages (see Fig. 2) and reads differentially the avalanche current sensed through two resistors R_S that are in series with the SPAD and "dummy" paths, when transistors M_N are ON.

The first comparator stage is a level shifter for setting the detection threshold and for shifting input signals in order to adapt them to the common-mode voltage of the following stage. It is implemented by controlling the bias current of pMOS transistors M_{IN}, in a source follower configuration. The

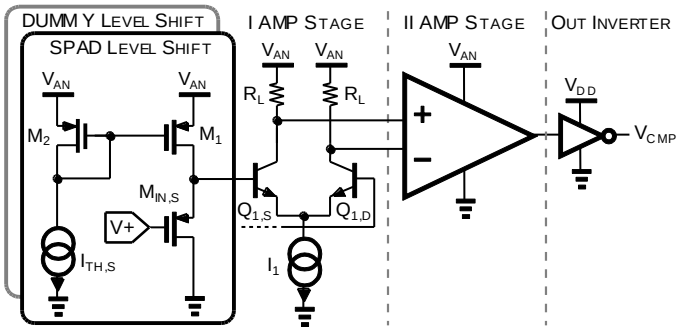

Fig. 2. The four stages of the fast differential comparator are shown here: level shift stages (only the SPAD one is reported in this figure) adapt input common mode and set the threshold; first and second amplifying stages read the differential voltage and drive the following on-chip CMOS gates through the OUT inverter.

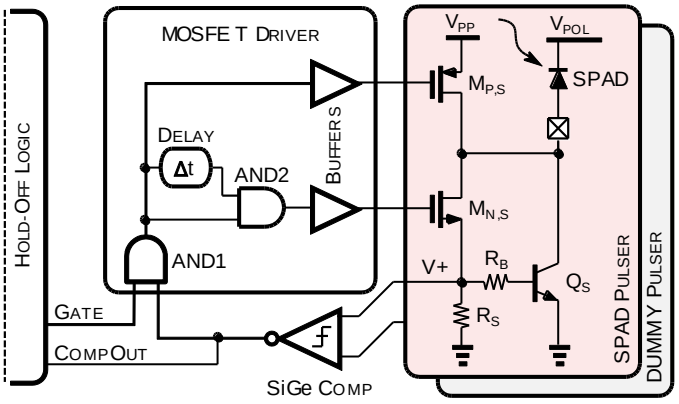

Fig. 3. Fast pulser (and its driving logic) for enabling the SPAD. Only SPAD half circuit is represented. AND1 gate is used to quickly quench the detector when an avalanche is detected, whilst BJT improves the gate rising edge.

gates of these transistors are directly connected to the sense resistors R_S and guarantee high impedance inputs. The source voltage of M_{IN} transistors is adjusted by programming the bias current through a couple of current mirrors (transistors M_1-M_2). Bias currents (I_{TH}) can be adjusted through external voltages so that the V_{GS} voltage, and hence the comparator threshold, can be finely tuned in a ±100 mV range. Bandwidth of this stage is about 1 GHz, limited by the input parasitism ($C_{SPAD} + C_{PAD}$, ~ 1.5 pF), since the low frequency pole is compensated by the zero with time constant C_{GS}/g_m.

The second stage is made by a bipolar differential stage ($Q_{1,S} – Q_{1,D}$), with resistive load, that amplifies the small differential signal between the SPAD anode and the "dummy" one. This simple configuration is preferred to those with positive feedback for achieving high-speed switching time [19] since additional transistors would increase the capacitive load at these very critical nodes, without introducing significant improvements. The bipolar stage switches all available current between the two arms with a low differential input voltage, approximately $4 \cdot V_T$ (where $V_T = kT/q$ is the thermal voltage and is about 25 mV at room temperature), but also the output differential voltage has a limited excursion. Hence, a second bipolar differential stage with single-ended rail-to-rail output stage is used in order to achieve a level suitable for 3.3 V CMOS gates. Finally, an inverter, with minimum W/L ratio, interfaces the second amplifying stage with the CMOS logic. All these stages are designed to have fast $1 \rightarrow 0$ transition of the output signal, which is the one that occurs when a photon is detected, in order to minimize the quenching time of the SPAD.

B. Gate Driver Logic and Pulser

This section of the circuit is used to quickly enable the SPAD, according to the pattern given by the externally-provided gate signal, and to actively quench the avalanche. As shown in Fig. 1a, by switching ON and OFF M_N and M_P transistors, the SPAD can be either enabled or disabled. MOSFET drive logic, simplified in Fig. 3, is designed to prevent cross conduction between these two transistors. When the detector has to be activated, first the anode is left floating (both p-type and n-type MOSFETs are kept OFF) for 2 ns, and then connected to ground through M_N and the sense resistors R_S. To generate this pattern, we used the AND2 gate and the delay line Δt. In order to have a fast avalanche quench, the propagation time of the signal switching ON M_P transistor is minimized through asymmetric sizing of transistors therein. Furthermore, AND1 gate, directly driven by the comparator output, bypasses all the delay introduced by the hold-off logic for having a quick gate disable. In addition, M_P and M_N transistors are sized for minimum switching time and, since they have to drive a relative large capacitance (~ 1.5 pF), their W/L ratio is big (~ 1000), for ensuring good performance even at low excess bias voltages.

In order to speed-up the rising edge of the gate, an additional BJT transistor and its resistor are added to each half of the pulser. When the gate is turned ON, both $M_{N,S}$ and $M_{N,D}$ gates are raised and thus a common mode spike appears on both sensing resistors of SPAD and "dummy". Such spike turns ON bipolar transistors Q_S and Q_D that help $M_{N,S}$ and $M_{N,D}$ to lower the anode voltage.

Resistors R_B ensure their correct bias during the gate turn on: even if a photon is detected when BJT transistors are ON, a fraction of the avalanche current flows through R_S and the comparator can sense it. Both resistors R_S and R_B have the same value of 100 Ω. The device area of the BJTs is sized to guarantee the minimum propagation time when a photon is detected in the middle of the gate rising edge. As soon as the switch-on transition is concluded, the common mode spikes finish and the BJTs switch off.

C. Hold-Off Logic

Concerning afterpulsing effect, typical time constants of charge carrier release in InGaAs/InP SPAD are in the order of few microseconds [20], but to satisfy requirements of various applications and to exploit this circuit with other SPADs fabricated in different materials, the hold-off time has to span from tens of nanosecond to hundreds of microseconds. This makes it possible to employ the present circuit also with silicon SPAD, where the time constants are in the nanosecond range. To have this wide range of programmability, we included a 17-bit programmable counter, clocked at 100 MHz

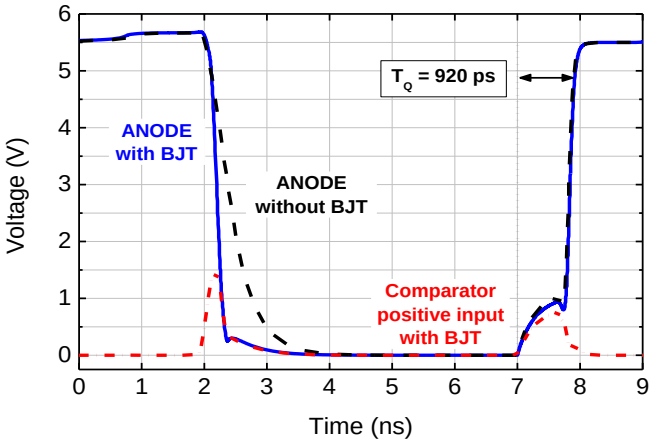

Fig. 4. Simulated waveforms at SPAD anode and at comparator positive input at 230 K. Anode voltage is reported with and without Q_S and Q_D BJT transistors that speed up the transition. The spike at the positive input of the comparator, due to the capacitive coupling of the gate, is rejected since the same signal is also present at the negative input. Instead, the pulse at time = 7 ns is due to a simulated photon detection. The avalanche is quenched in T_Q < 1 ns, both with and without BJTs.

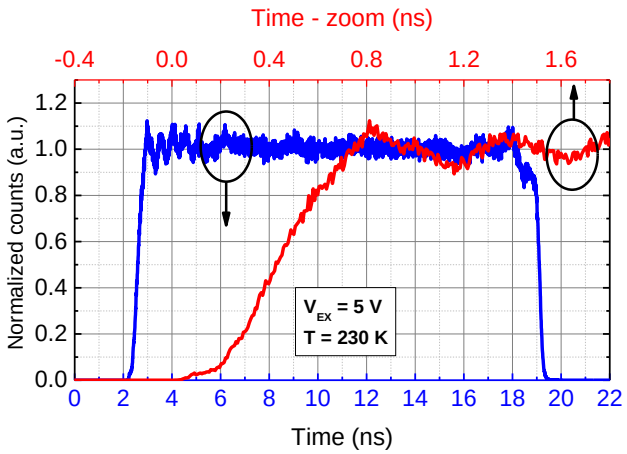

Fig. 5. With 20 ns electrical gate, the SPAD is ON within a 17 ns window. A zoom on the fast rising edge shows that transitions times are shorter than 300 ps (20% – 80%).

for programming the hold-off time up to 1.3 ms with a resolution of 10 ns. The counter is preloaded with a word (H in Fig. 1b) through a SPI compatible interface. When a photon is detected, subsequent gates are discarded by the logic and the counter decreases its value until zero. Gate signal is provided again to the SPAD starting from the following entire gate period, to avoid different gate widths that would introduce distortion in the acquired waveform. The counter is synthetized using Linear-Feedback Shift Register technique to minimize layout area. The 100 MHz clock can be selected either from an internal ring oscillator or from an external source.

III. Simulations and Experimental Results

Extensive post-layout simulations were performed on the FG-AQC exploiting a complete SPAD model [21].

The comparator has low propagation delay: the average switching time is 250 ps with 15% spread when the input amplitude is in the range from 50 mV to 200 mV. This low amplitude-to-time dispersion is a key parameter to guarantee uniform response within the gate, especially on the edges where avalanche pulses are smaller.

When a photon is detected, the comparator output goes low. We reduced such fall time to less than 100 ps in order to keep the intrinsic time jitter on avalanche detection as low as possible.

The quenching time T_Q is less than 1 ns, as shown in Fig. 4. The first part is given by the passive quenching of the sense resistor R_S, whereas in the second one, after the propagation time of the comparator and of the driving logic, the anode is actively driven to V_{PP} voltage. Unlike other approaches, the quench time is fully independent from the duration of the ON time.

Fig. 4 also shows the improvements on the gate aperture edge (falling edge in this figure) given by the additional bipolar transistors Q_S and Q_D. The simulated edge transition duration is 220 ps (20% – 80%), instead of about 1 ns with only MOS transistors (the circuit was simulated with 5 V excess bias with a gate amplitude of 5.5 V at 230 K). By lowering the gate amplitude, common-mode spikes decrease, thus BJTs conduction is lower and the improvement decreases. At room temperature, the quenching time is slightly longer, but still below 1 ns.

Experimental characterization confirms the simulated results. All tests were performed at 230 K with a 25 µm InGaAs/InP SPAD [20] mounted on a custom-designed PCB placed on top of a four-stage thermo-electric cooler inside a dry chamber. Unless otherwise specified, excess bias voltage is 5 V and the gate pulse amplitude is 5.5 V. The breakdown voltage is 63.1 V at 230 K.

Fig. 5 reports the sensitivity of the system when a 20 ns gate pulse is provided to the FG-AQC. The detector is illuminated with CW ambient light and the temporal distribution of incoming photons is acquired by means of TCSPC technique. Since the SPAD detection efficiency is proportional to its excess bias, either ringing oscillations or overshooting of the electrical gate waveform are reproduced in the counts distribution. The oscillations (about 10% of the steady state value) at the beginning of the gate are mainly due to the resonance of the LC circuit made of the inductance of the bonding wires and the SPAD capacitance, triggered by the fast rising edge (< 300 ps, 20 – 80%). It should be noted that there is no photon accumulation at the beginning of the gate window, as opposite to what reported for non-optimized gating circuits. The resulting sensitivity window is about 3 ns shorter than external electrical pulse. Sensitivity windows as short as 150 ps can be obtained, even though with reduced peak efficiency (about 25% of the full one). The full gate amplitude is reached with T_{ON} greater than 500 ps (see Fig. 6). With very short gates, the charge that flows inside the device is further reduced because the short gate reduces the quenching time, like in the sine-gate approach [18]. Since the control logic is fully static, there is no limitation on the maximum duration of

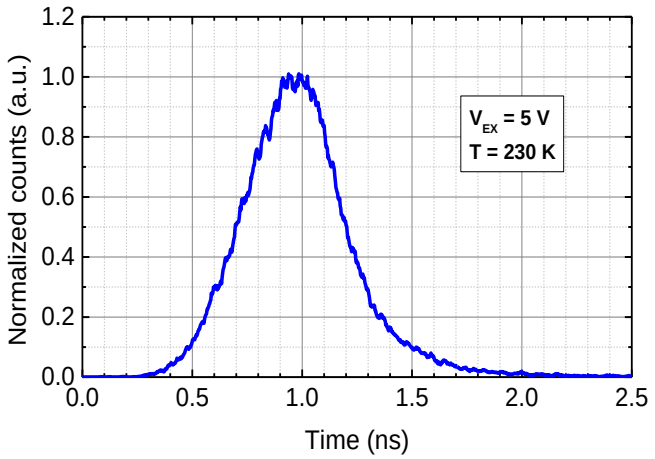

Fig. 6. Sensitivity within a 500 ps (Full-Width at Half Maximum, FWHM) gate window. Full photon detection efficiency is reached despite the very narrow gate. As a reference, the normalized value is taken from the steady-state value of a much longer (20 ns) window.

the gate and the chip can also be employed in free-running mode (i.e. the SPAD is ON until an avalanche event occurs).

In order to estimate the quenching time and the avalanche charge, we measured the electroluminescence emitted by the SPAD itself. As discussed in [22], this photon emission is representative of the current flowing through the junction. The faint emission is measured with an InGaAs/InP SPAD module [8], coupled to the SPAD under test by means of a focusing lens in order to increase the collection efficiency. As shown in Fig. 7, the luminescence (and thus the current) is reduced to 10% of its peak value in less than 2 ns, while 80% of the charge flows through the device in 1 ns.

The integral of the curves is proportional to the charge and the charge ratio (QR), between a specific curve and the reference one at V_{EX} = 5 V is reported in the legend of Fig. 7.

Afterpulsing probability was measured with a setup based on a CPLD (Complex Programmable Logic Device) and a pulsed laser. The laser provides pulses that trigger an avalanche with almost 100% probability. Then the CPLD

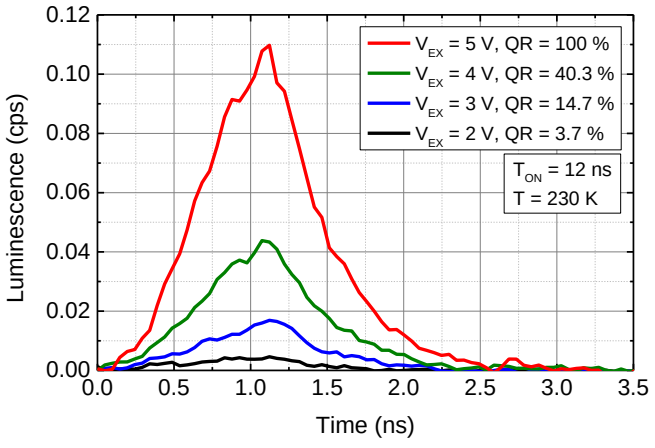

Fig. 7. Electroluminescence of the InGaAs/InP SPAD operated with the FG-AQC, at various excess bias voltages. The exponential decay is partially due to the tail of the InGaAs/InP SPAD module employed for these measurements, whose decay time constant is about 250 ps. Acquisition time is 2 hours for each curve.

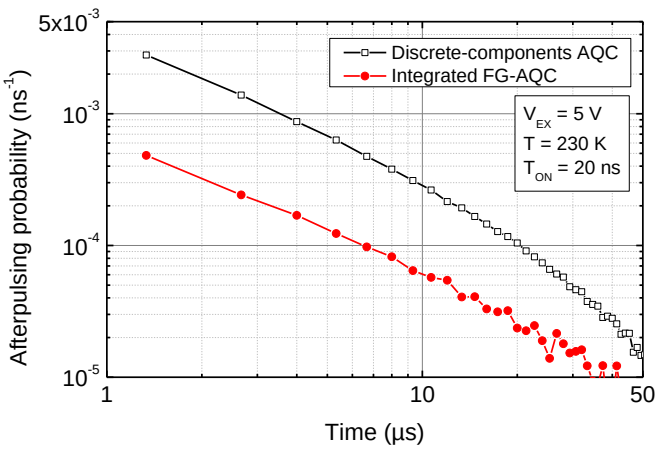

Fig. 8. Comparison of afterpulsing probability densities obtained with the integrated circuit presented here and the module described in Ref. [8], using InGaAs/InP SPADs from the same family.

registers the avalanches in the following gates. With the same procedure, the same operating conditions and a detector of the same family [20], we compared the FG-AQC with the system presented in Ref. [8] (see Fig. 8). The integrated circuit guarantees an afterpulsing probability that is four times less than that achieved with discrete components module.

The temporal response of the system is characterized employing a picosecond pulse laser at 1550 nm (pulse width is 20 ps FWHM) that uniformly illuminates the active area of the device. The comparison between the FG-AQC and the discrete components module is shown in Fig. 9. The curves are

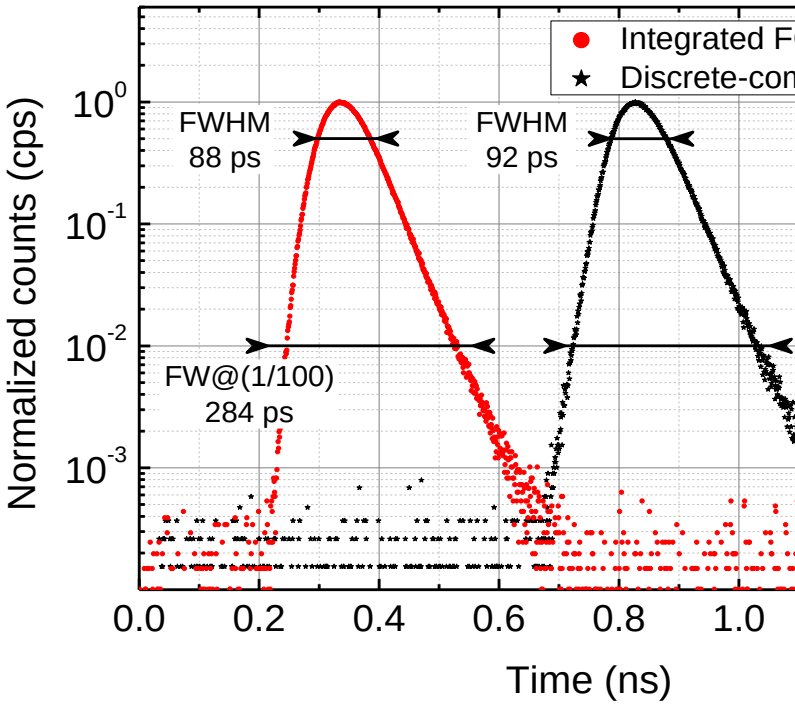

Fig. 9. Temporal response to a 20 ps laser pulse: comparison between integrated FG-AQC and a discrete component module. The same clean and sharp response is registered in both cases and neither distortions nor artifacts are reported. The two curves are shifted in time for representation purposes.

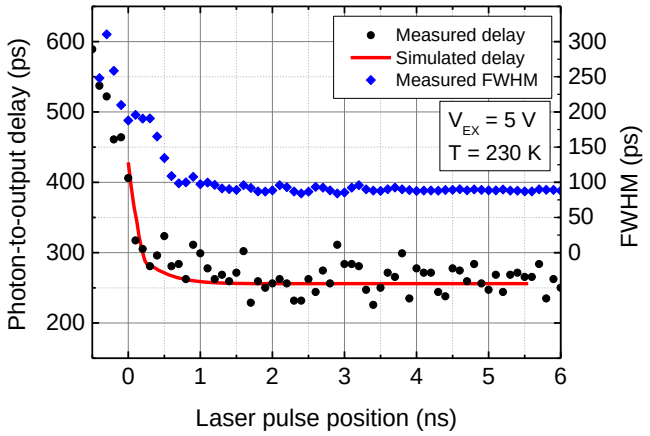

Fig. 10. Delay between the photon arrival time (i.e. the laser pulse position) and the output pulse, moving the laser inside the gate. The origin of the time axis is placed at the beginning of the gate rising edge. Experimental data match very well the simulation results. On the right axis, the measured Full-Width at Half-Maximum of the temporal response is reported: it increases only during the initial 500 ps, due to the gate edge. Measurement time for each point is 30 s.

comparable: with an excess bias of 5 V, their widths (in terms of FWHM) are less than 100 ps and their full widths at 1/100 of the maximum are about 300 ps.

Since the timing performance depends on the SPAD device, we measured the response of the circuit employing a silicon SPAD, which has a lower intrinsic timing jitter compared to the InGaAs/InP one. A 20 µm silicon SPAD is illuminated with a pulsed laser (pulse width is 10 ps FWHM) at 830 nm. We measured a timing jitter of 39 ps (FWHM), comparable with what obtained with state-of-the-art non-gated single-photon detection modules, thus demonstrating that the FG-AQC introduces very little timing jitter.

The fast-gated AQC was designed to guarantee sharp time filtering and the ability to detect photons even during the rising edge of the gate with low distortion. By adjusting the time delay between the laser pulse and the gate window at 100 ps step, we acquired the responses of the FG-AQC during the gate opening. From each TCSPC waveform, we calculated the relative position between the laser pulse and the fitted peak of the SPAD response (fitting was needed in order to compensate for amplitude variations, especially when the laser is moved outside the gate). The matching between experimental data and post-layout simulations is very good, as shown in Fig. 10. The propagation delay increases only near the gate edge, i.e. in the first 500 ps, where there is also a widening of the timing response due to the time-varying excess bias on the gate edge. Given the typical tail of the SPAD temporal response [11][20], even few photons arriving before the gate give an output inside it, represented by the points with negative time values in Fig. 10. However the number of these events is several order of magnitude below the signal detected inside the gate.

IV. CONCLUSIONS

We presented a SiGe BiCMOS integrated circuit for the operation of SPADs in gated mode. The chip was designed to be mounted close to the cooled detector, inside the same package and at low temperature (~ 230 K). The low propagation delay and the fast switching time guarantee prompt avalanche quenching for reducing the charge flow within the SPAD. This reduces the afterpulsing probability of InGaAs/InP SPAD by a factor of four over a state-of-the-art discrete component system. Sharp time filtering is achieved thanks to the integrated fast pulser with 300 ps edges. Sub-nanosecond gate width can be obtained and, since the design is fully static, the circuit can be also used in free-running mode.

The high speed and low jitter comparator makes it possible to achieve timing resolution better than 100 ps with InGaAs/InP SPAD with an excess bias of 5 V. Timing jitter increases to about 200 ps just in proximity of the rising edge of the gate due to the time varying excess bias. Low power consumption and slim size will enable its integration in arrays for multi-pixel systems.

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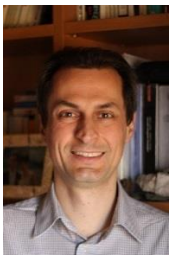

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