SPAD Figures of Merit for Photon-Counting, Photon-Timing, and Imaging Applications: A Review

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***Abstract*— Single-photon avalanche diodes (SPADs) emerged as the most suitable photodetectors for both single-photon counting and photon-timing applications. Different complementary metal–oxide–semiconductor (CMOS) devices have been reported in the literature, with quite different performance and some excelling in just few of them, but often at different operating conditions. In order to provide proper criteria for performance assessment, we present some figures of merit (FoMs) able to summarize the typical SPAD performance (i.e. photon detection efficiency, dark counting rate, afterpulsing probability, hold-off time, and timing jitter) and to identify a proper metric for SPAD comparisons, when used either as single-pixel detectors or in imaging arrays. The ultimate goal is not to define a ranking list of best-in-class detectors, but to quantitatively help the end-user to state the overall performance of different SPADs in either photon-counting, timing, or imaging applications. We review many CMOS SPADs from different research groups and companies, we compute the proposed FoMs for all them and, eventually, we provide an insight on present CMOS SPAD technologies and future trends.**

***Index Terms*— CMOS imagers, figure of merit, photon counting, single-photon avalanche diode (SPAD).**

I. Introduction

SINCE 60's, Single-Photon Avalanche Diodes (SPADs) have been deeply studied and used in several fields where single-photon sensitivity is required such as fluorescence correlation spectroscopy (FCS) [1], fluorescence lifetime imaging (FLIM) [2], positron emission tomography (PET) [3], as well as laser (LIDAR/LADAR) [4] and 3-D optical ranging [5]. In all these applications, the intensity and time-dependent waveform of very faint optical signals can be acquired by counting photons (photon-counting) in real time, within time bins down to the microsecond time scale. Also, the waveforms of very fast events, down to the picosecond timescale, can be reconstructed by repetitively acquiring the arrival time (photon-timing), exploiting Time-Correlated Single-Photon Counting (TCSPC) for building the histogram.

Although many single-photon sensitive devices already existed, SPADs have gained attention because of some advantages over photomultiplier tubes (PMTs) and multi-channel plates (MCPs), which require high bias voltages, are bulky and sensitive to magnetic fields, and cannot be integrated with complementary metal-oxide semiconductor (CMOS) electronics. Conversely, SPADs are small, rugged, easy to integrate in large array, and are insensitive to magnetic fields, making them suitable for medicine and space application [6]. Until ten years ago, SPADs were fabricated solely through fully custom processes, whose flexibility provided devices with thick depleted regions, engineered electric fields, dedicated annealing steps and gettering processes to minimize lattice damages for improving noise, yield, and uniformity. Custom SPADs provide best-in-class performance in terms of detection efficiency, noise and timing jitter [7]–[14]. However, because of dedicated processes and the impossibility to integrate proper quenching and processing electronics with the detector, custom SPADs are best suited for small (up to about a hundred) pixel arrays [15].

From the early 2000s onwards, it was possible to exploit standard CMOS technologies to fabricate SPADs, with the main advantage of monolithic integration on the same chip of photodetectors, analog avalanche sensing and quenching electronics, and digital circuitry for implementing smart photon-counting and photon-timing on-chip processing. As a matter of fact, researchers started to develop compact and cost-effective multi-pixel SPAD-based image sensors that represent a viable solution for all those applications where bulky and expensive intensified (I-CCDs) or electron-multiplying charge-coupled devices (EM-CCDs) are used, although there is still room for improvements regarding fill-factor, quantum efficiency and optical stack optimization.

In the last years, many groups worldwide developed different SPAD structures in different CMOS technology nodes [16]–[48] for coping with the different issues, including but not limited to premature edge breakdown, tunneling effects, electric field uniformity, sensing electronics complexity, and wide depleted region thickness. Very often each group performed measurements in different experimental conditions (e.g. breakdown voltage, excess bias, hold-off time, average count rate, wavelength, etc.), which better maximized the target data, and often considered to have reached the novel state-of-the-art performance in one or another parameter. In such a maze of variables and measurements, it is difficult to make a fair comparison between different SPAD designs and CMOS technologies, and to envision a clear trend, unless a subset of representative parameters is found.

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To this purpose, we propose a comprehensive Figure-of-Merit (FoM) based on well-assessed typical SPAD performance, like photon detection efficiency, noise, dead-time, timing jitter, fill-factor [49], and other well-known quality meters, like Signal-to-Noise Ratio, Noise Equivalent Power, and Detectivity. Our aim is not to outline a ranking list, but to define a proper user-friendly metric to help SPAD users to compare detection performance in different application fields (photon-counting and photon-timing) and also as single pixels or as SPAD array imagers.

We consider also Silicon Photomultipliers (SiPMs) [50]–[57], which can overcome some limitation of SPADs, since they provide large area and are made of hundreds or thousands of SPAD microcells connected in parallel – thus behaving like a single detector, but with the capability to resolve the number of imping photons. In analog SiPMs, each SPAD is integrated with its own quenching resistor and the avalanche currents are summed up to provide the detector analog output. Instead, digital SiPMs provide active quenching circuits into each microcell and further on-chip digital electronics.

The paper is organized as follows: Section 2 briefly describes the main SPAD parameters; Section 3 defines the proposed FoMs and Section 4 shows and comments how they apply to a broad selection of SPADs and SiPMs either reported in literature or commercially available.

II. Main SPAD Parameters

Photon Detection Efficiency (PDE) is defined as the ratio of the number of detected photons and the number of photons incident on the photoactive area. This ratio depends on absorption probability and on triggering efficiency [49].

Apart from signal fluctuations due to its own Poisson statistics, SPAD's main noise source is due to spurious counts, which are either uncorrelated or correlated to signal photons. The uncorrelated contribution is due to ignitions caused by carriers generated through Shockley-Read-Hall processes, trap-assisted tunneling (TAT), or Poole-Frenkel emission and is referred to as Dark Counting Rate (DCR) [49]. Instead, correlated noise comes from different sources, such as optical and electrical crosstalk (among different pixels) and afterpulsing (within the same pixel). The latter is caused by carriers that get trapped during an avalanche current pulse and are released when the SPAD is newly biased above breakdown (V_{BD}), thus igniting an "afterpulse". If N_{DET} photons are detected and N_{AP} additional correlated counts are generated, the afterpulsing probability P_{AP} can be defined as:

$$P_{AP} = N_{AP}/N_{DET} \tag{1}$$

Of course, afterpulsing is a cascade process and N_{AP} counts will generate $N_{AP} \cdot P_{AP}$ counts and so on. Therefore, for N_{DET} detected photons the number of measured counts N_{MEAS} is:

$$\begin{aligned} N_{MEAS} &= N_{DET} + N_{DET}\,P_{AP} + \ldots = N_{DET} \cdot \sum_{n=0}^{\infty} P_{AP}^{n} \\ &= \frac{N_{DET}}{1 - P_{AP}} \end{aligned} \tag{2}$$

Hence, because of afterpulsing, the number of real photons is always lower than the measured number of ignitions; if such afterpulsing probability is high enough, SPAD saturation can occur. In order to reduce afterpulsing, a dead-time T_{DEAD}, (from tens to hundreds of nanoseconds) is enforced to the SPAD after each ignition, allowing the trapped carriers to be released. Apart from reducing P_{AP}, long dead-time lowers the maximum count rate to $1/T_{DEAD}$, in case of active reset, or to $1/(e \cdot T_{DEAD})$ with passive reset [58] (e being the Euler number).

Finally, the SPAD timing jitter (photon-timing precision) is the statistical spread of output pulse on-set compared to the true photon arrival time [59] and is quoted by the Full-Width at Half Maximum (FWHM) of the distribution histogram.

III. Figures of Merit

Single-photon detectors are exploited in three main approaches, namely photon-counting (for measuring the intensity of slowly varying optical signals, in the μs range), photon-timing (for reconstructing very fast optical waveforms, in the ps range) and photon-imaging (for acquiring one- or two-dimensional images). In the first two modes, one or few dozen independent detectors usually suffice, whereas imaging requires large arrays at least hundreds of detectors, hence pixel pitch and fill-factor do play an important role.

A. Photon-Counting Applications

In photon-counting, performance are commonly quoted as Noise Equivalent Power (NEP), Signal-to-Noise Ratio (SNR), specific detectivity (D*), and Dynamic Range (DR). In this paragraph, we will study their dependence on SPAD parameters in order to define a new unique FoM.

For a SPAD, SNR is given by [49]:

$$SNR = \frac{S}{\sqrt{S+N}} = \frac{PDE \cdot \Phi_S \cdot T_{INT}}{\sqrt{PDE \cdot \Phi_S \cdot T_{INT} + DCR \cdot T_{INT}}} \tag{3}$$

where Φ_S is the signal photon-rate and T_{INT} is the integration time employed to count photons.

NEP is defined as the minimum signal intensity required to achieve SNR = 1 within 1 Hz bandwidth [60] and quantifies detector sensitivity:

$$NEP = h\nu \cdot \frac{\sqrt{2 \cdot DCR}}{PDE} \tag{4}$$

A lower NEP denotes better SPAD performance. Specific detectivity D* is a measure of the minimum detectable radiant power and takes into account the photoactive area [61]:

$$D^* = \frac{\sqrt{Area}}{NEP} \Rightarrow \; i.e.\; f\left(PDE, \sqrt{Area}, \frac{1}{\sqrt{DCR}}\right) \tag{5}$$

Moreover, in photon-counting applications it is desirable to have a high dynamic range, defined as the ratio between maximum S_{MAX} and minimum S_{MIN} detectable signals:

$$DR = S_{MAX}/S_{MIN} \tag{6}$$

The maximum achievable photon flux, Φ_{MAX}, is limited by the dead time, T_{DEAD}, imposed after each ignition and the afterpulsing probability, P_{AP}, taking also into account the wasted count rate due to noise, i.e. the DCR.

Therefore:

$$\Phi_{MAX} = \left(\frac{1 - P_{AP}}{(e) T_{DEAD}} - DCR \right) \approx \frac{1 - P_{AP}}{(e) T_{DEAD}} \tag{7}$$

The approximation is usually valid, since SPADs have DCR from tens to thousands of counts per second, i.e. much lower than the inverse of typical dead times of some tens of nanoseconds. Eventually, given a certain integration time T_{INT}, the maximum achievable signal can be written as:

$$S_{MAX} = \Phi_{MAX} \cdot T_{INT} \tag{8}$$

The minimum detectable signal (S_{MIN}) represents the photon count needed to reach SNR = 1, as a function of the integration time [49], and for most cases it is given by:

$$S_{MIN} \approx \sqrt{DCR \cdot T_{INT}} \tag{9}$$

We can express dynamic range as:

$$DR = \frac{\Phi_{MAX} \cdot T_{INT}}{\sqrt{DCR \cdot T_{INT}}} \Rightarrow \; i.e. \; f\left(\frac{1}{\sqrt{DCR}}, \Phi_{MAX} \right) \tag{10}$$

Both D* and DR increase with improved performance, so we define the photon-counting FoM_C considering all device parameters appearing in these two quantities, i.e. efficiency, noise, active area, and maximum achievable photon flux:

$$FoM_C = PDE \cdot \frac{\sqrt{Area}}{\sqrt{DCR}} \cdot \frac{1 - P_{AP}}{T_{DEAD}} \tag{11}$$

where we considered $T_{INT} = 1\ s$. The dimensions of FoM_C for photon-counting is m, since the square root of DRC is given as s^{-1} and T_{DEAD} is quoted in s, the detector's area is given as m^2, and PDE and P_{AP} are dimensionless. Table I shows the FoM_C values computed for a large number of custom SPADs, CMOS SPADs, and SiPMs; as can be seen, typical values range from $10^{-2}\ m$ to $10^{3}\ m$. Since PDE depends on photon wavelength, spot FoM_C values could be quoted for application-specific wavelengths or an average PDE value could be used as representative over the range of interest.

B. Photon-Timing Applications

In photon-timing applications, SNR still plays an important role. Fig. 1 shows the typical photon-timing response of a SPAD to a laser pulse of negligible width. The Gaussian component of the timing waveform is described as:

$$f(n) = \frac{PDE \cdot \Phi_S}{\sigma \cdot \sqrt{2\pi}} \cdot T_{BIN} \cdot \exp\left[-\frac{(n \cdot T_{BIN} - \mu)^2}{2 \cdot \sigma^2} \right] \tag{12}$$

where n is the number of bins, T_{BIN} is the histogram bin width, Φ_S is the signal photon rate, μ is the time at which the timing peak occurs, and σ is given by $FWHM = 2\sigma\sqrt{2\,ln\,2} = 2.35\sigma$. The peak value is given by:

$$S_{PEAK} = \frac{PDE \cdot \Phi_S}{k \cdot FWHM} \cdot T_{BIN}, \quad \text{where } k = \sqrt{\frac{\pi}{4\,ln\,2}} \tag{13}$$

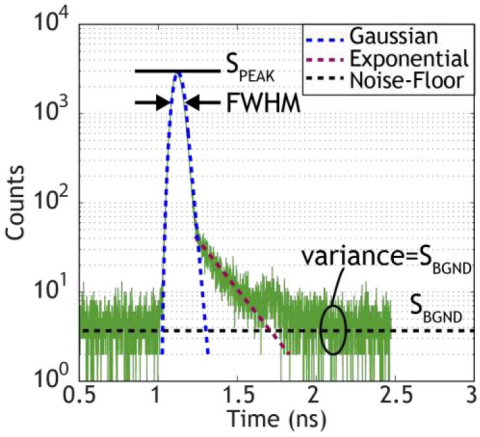

Fig. 1. Typical timing waveform of a SPAD, with its components described in the text, and the Signal-to-Noise ratio defined as the ratio between the timing peak and the noise background.

The background level is set by dark counts as:

$$S_{BGND} = DCR \cdot T_{BIN} \tag{14}$$

and its standard deviation is $\sqrt{S_{BGND}}$, since DCR follows a Poisson distribution.

Hence, considering a unit T_{BIN}, SNR can be written as:

$$SNR = \frac{S_{PEAK}}{\sqrt{S_{BGND}}} = \frac{PDE \cdot \Phi_S}{k \cdot FWHM} \cdot \frac{1}{\sqrt{DCR}} \tag{15}$$

Hence SPADs with higher PDE, lower DCR, and narrower timing response will exhibit better SNR. Therefore we can define the photon-timing FoM_T as:

$$FoM_T = PDE \cdot \frac{\sqrt{Area}}{\sqrt{DCR}} \cdot \frac{1 - P_{AP}}{T_{DEAD}} \cdot \frac{1}{FWHM} = \frac{FoM_C}{FWHM} \tag{16}$$

where we considered as signal flux the maximum achievable one, and we added the area to consider its influence on the dark count rate. Eq. (16) highlights the relationship existing between FoM_T and FoM_C. The dimensions of FoM_T are $m \cdot s^{-1}$. As done for FoM_C, Table I shows also the FoM_T values computed for a large number of custom SPADs, CMOS SPADs, and SiPMs; as can be seen, typical values range from $10\ m \cdot s^{-1}$ to $10^7\ m \cdot s^{-1}$. Also similar to FoM_C, PDE should be evaluated at the specific wavelength of the desired application or the PDE average could be computed over the range of interest.

C. SiPM Case

Concerning the application of the proposed FoM to SiPMs, some comments are necessary. From a technological standpoint, in order to assess the quality of a SiPM, namely the quality of the SPADs composing the SiPM (either analog or digital) microcells, the SiPM microcell could be treated as an individual SPAD. Hence FoM_C and FoM_T equations apply, when considering the parameters of the individual microcell. However, since in datasheets only the overall SiPM performance is reported, in Table I we inferred the microcell parameters in this way: the microcell PDE is obtained by

TABLE I

MAIN SPAD PARAMETERS FOR SEVERAL SPADS AND SIPMS AND THEIR COUNTING AND TIMING FIGURES-OF-MERIT. BEST PERFORMANCE FOR EACH CATEGORY ARE IN BOLD

Ref.	V_{EX}/V_{BD} (V/V)	PDE_{PEAK} (%) @ (nm)		Area (μm^2)	DCR @ RT (cps)	AP (%)	FWHM (ps) @ (nm)		Φ_{MAX} (Mcps)	FoM_C counting (m)	FoM_T timing (m/s)
Custom SPADs											
[7]	20/55	60	[650]	1,963	550	n.a.	93	[820]	27.6 ^	31.3	336,510
[8]	n.a.	70	[700]	25,447	500 *	0.5	350	[825]	**35**	**774.8**	2,213,594*
[9]	5/n.a.	50	[550]	7,854	2,500 *	1	**35**	**[850]**	13	118.7	**3,390,663***
[10]	5/n.a.	60	[650]	7,854	2,500 *	n.a.	100	[850]	13	142.4	1,424,079*
[13]	10/n.a.	62	[650]	**196,350**	150,000	n.a.	400	[650]	1	0.7	1,773
[14]	n.a.	**73**	**[650]**	7,854	**250**	0.5	800	n.a.	12	49.0	61,212
SiPMs											
[50]	3.3/25	31	[420]	780	200	n.a.	**54**	[410]	25	15.3	283,653
[51]	n.a.	35 ^	n.a.	17.2	312	n.a.	163 ^		**100**	8.2	50,416
[52]	1.5/n.a.	45	[410]	208	13,700	<0.1	171	[470]	6.7	0.4	2,173
[53]	5/95	55	[520]	1,500	375	n.a.	200 *	[440]	27.6 ^	30.4	151,800
[54]	2.6/65	56	[450]	1,550	250	n.a.	250 *		27.6 ^	38.5	153,941
[55]	5/26	43	[420]	960	160	n.a.	163 ^		5	5.3	32,309
[56]	3.75/25	**80**	[420]	1,575	277	n.a.	163 ^		27.6 ^	**52.7**	**323,007**
[57]	2.5/24.5	48.6	[420]	**1,800**	**92**	0.6	600 *		3	6.4	10,749
800 nm CMOS SPADs											
[16]	5/25	28	[470]	38.5	900	7.5	60	[710]	12.3	0.7	11,872
[17]	2.5/21	20	[470]	32.2	**50**	~ 0	50	[710]	**31.3**	**5.0**	**100,466**
[18]	5/16	**32**	**[460]**	**113**	600	2.6	**41**	**[820]**	17.7	2.5	59,979
[19]	5/25.5	26	[460]	38.5	350	~ 0	115	n.a.	25	2.2	18,746
350 nm CMOS SPADs											
[20]	5/25	**55**	**[420]**	**1,963**	155	3.9	75	[780]	**48.1**	**94.1**	**1,254,969**
[21]	3.3/n.a.	36	[460]	78.5	750	23	80	[670]	4	0.5	5,823
[22]	4/28	13	[600]	400	5000	40	80	[637]	27.6 ^	1.0	12,685
[23]	5/48	34.4	[450]	19.6	**50**	n.a.	80	n.a.	10	2.2	26,922
[24]	5/17.7	35	[460]	38.5	646	~ 0	163 ^	n.a.	1.9	0.2	996
[25]	3.3/28	33	[450]	400	300	4.5	160	[470]	4.7	1.8	11,193
[26]	4/n.a.	32	[455]	250	1000	6	70	[420]	7.3	1.2	16,686
[27]	5/24	42	[450]	314	4900	27	**39**	**[820]**	27.6 ^	2.9	75,266
[28]	5/n.a.	20	[465]	28.3	186	n.a.	230	[637]	16.6	1.3	5,631
[29]	2/18.9	13.2	[610]	78.5	750	23	80	n.a.	4	0.2	2,135
180 nm CMOS SPADs											
[30]	0.5/10.2	2.5	[470]	**78.5**	60000	~ 0	163 ^		33.3	0.03	185
[31]	2.5/10	11	[450]	49	200000	~ 0	**27**	**[650]**	**200**	0.34	12,754
[32]	3.5/20.3	20	[470]	50.3	**180**	~ 0	80	n.a.	66.7	**7.05**	**88,142**
[33]	1.5/11	17.4	[470]	**78.5**	13000	~ 0	163 ^		25	0.34	2,074
[34]	4/20	**36**	**[600]**	**78.5**	5000	50	165	[790]	0.7	0.03	191
130 nm CMOS SPADs											
[35]	1.7/10	**34**	**[450]**	78.5	105	~ 0	144	[637]	10	2.94	20,412
[36]	2/9.4	26	[480]	58.1	220	n.a.	128	[408]	27.6 ^	3.69	28,809
[37]	1.4/14.4	28	[500]	50.3	60	~ 0	200	[470]	10	2.56	12,818
[38]	1.5/12	30	[425]	19.6	230	n.a.	198	[408]	27.6 ^	2.42	12,207
[39]	0.5/11.3	2	[570]	**100**	1000	~ 0	163 ^		**83.3**	0.53	3,232
[40]	0.73/n.a.	27.5	[500]	24.6	160	~ 0	140	[637]	10	1.08	7,702
[41]	1/n.a.	25	[480]	58.1	100	0.1	**61**	n.a.	10	1.91	31,241
[42]	2/20	25	[560]	50.3	**18**	1	88	[654]	66	**27.58**	**313,372**
90 nm CMOS SPADs											
[43]	0.13/10.4	16	[470]	**50.3**	16000	32	398	[637]	0.6	0.01	14
[44]	0.5/10	36	[410]	3.1	250	0	107	[470]	16.6	0.67	6,219
[45]	1.4/14.9	**38**	**[690]**	32.2	**70**	0.4	**82**	**[470]**	**66.4**	**17.13**	**208,885**

* The commercial module is internally cooled, DCR is considered at the operating (unknown) temperature.

^ Since the value was not reported in the paper, the median of the values of all the other devices was considered in the computations.

dividing the SiPM PDE by fill-factor (FF). This was necessary because the PDE specified in the SiPM datasheets takes into consideration also the geometrical losses. The microcell area is computed by multiplying the total SiPM area by the fill-factor (FF) – which gives the total photoactive area – and by dividing the result by the number of microcells (N). Finally, the microcell DRC is obtained by dividing the total SiPM DCR by the number of microcells (N). Note that, for a fair comparison, the median DCR of a SiPM microcell can be lower than the total DCR divided by the number of microcells, since in large SiPMs the overall noise is affected by hot-pixels and crosstalk [49].

Instead, from an application standpoint, SiPM consisting of N microcells could reach a maximum achievable photon

flux, Φ_{MAX}, being theoretically N-times higher than the one of a single SPAD microcell, but in practice limited by the analog noise of the front-end electronics. Moreover, SiPM PDE and total area are affected by the fill-factor FF, which will further limit the achievable $\mathrm{FoM_C}$ for a SiPM. In a similar way the $\mathrm{FoM_T}$ for a SiPM could theoretically reach N times the $\mathrm{FoM_T}$ of the microcell (thanks to the increased maximum achievable photon flux). However in practice it is limited by the degradation of the SiPM overall DCR and FWHM performance, when compared to the single microcell ones, and to the ability of the digital electronics to properly count events few hundred of picoseconds apart.

D. Imaging Applications

CMOS SPADs typically have worst performance than custom SPADs, but they can be integrated together with on-chip electronics, resulting in monolithic large arrays with thousands of pixels, which can provide either 2D, 3D (distance-resolved), or time-resolved images and videos.

In most imaging applications, the sensor is used to count the number of incoming photons, either in free-running or in gated-mode. For this reason, the imaging $\mathrm{FoM_I}$ can be derived starting from $\mathrm{FoM_C}$, by further adding three fundamental parameters for array imagers: i) fill-factor; ii) number of pixels; iii) maximum frame-rate. Another important item is crosstalk probability among pixels, but this value is usually not reported in literature as it is generally negligible, thus we will not consider it. Hence, $\mathrm{FoM_I}$ should take into account efficiency, noise, fill-factor (FF), number of pixels (N), maximum frame-rate ($\mathrm{f_{MAX}}$), and maximum count rate:

$$FoM_I = PDE \cdot \frac{\Phi_{MAX}}{\sqrt{DCR}} \cdot FF \cdot N \cdot f_{MAX} \qquad (17)$$

where we considered $T_{INT} = 1\ s$, as for $\mathrm{FoM_C}$. The dimensions of $\mathrm{FoM_I}$ for imaging applications is frame per second (*fps*), since the ratio between Φ_{MAX} and DRC, as well as PDE and imager dimensions (pixel count and fill-factor) are dimensionless, while maximum frame-rate is given as frame per second.

Table III shows the $\mathrm{FoM_I}$ values computed for a large number of CMOS SPAD imagers; as can be seen, typical values range from $5 \cdot 10^3$ fps to 10^8 fps. The previous consideration about PDE still holds.

IV. Discussion

We reviewed a large number of papers on Silicon SPADs and SiPMs presented in scientific literature or commercially available. Table I reports a detailed list of state-of-the-art SPAD-based pixels, fabricated in both custom and CMOS technologies, with their main parameters and corresponding $\mathrm{FoM_C}$ and $\mathrm{FoM_T}$ values. The analyzed SPAD technologies are seven: custom technologies, two submicron (0.8 μm and 0.35 μm), three deep-submicron (DSM) (0.18 μm, 0.13 μm and 90 nm) technologies, and single-cells of digital and analog SiPMs. Submicron technologies are based on Local Oxidation (LOCOS) isolation processes, while deep-submicron ones exploit Shallow-Trench Isolation (STI) processing.

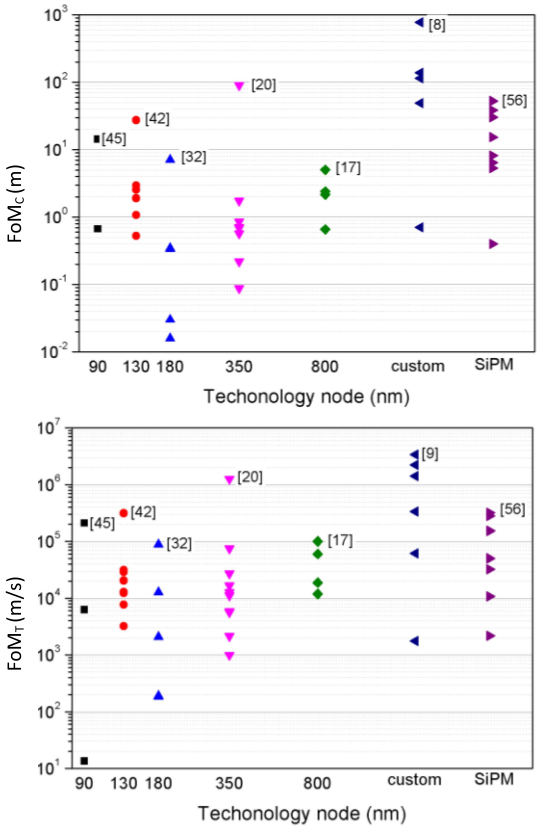

Fig. 2. $\mathrm{FoM_C}$ for photon-counting (top) and $\mathrm{FoM_T}$ for photon-timing (bottom) applications vs. technology node for the data listed in Table I. Only the best-in-class for each technology node are shown with the reference.

Photon detection efficiency, dark count rate, and afterpulsing probability are rated at the same excess bias. If parameters were rated at more than one excess bias in the original paper, we considered the one that provides the best FoM. When not specified in the original paper, we considered afterpulsing to be almost negligible (<0.5%). When some data – useful to compute the FoMs – are not reported in the paper, the median of the values of all the other devices was considered in the calculations. We also report the wavelength of the peak PDE and the wavelength at which timing response was characterized. In addition, the table also lists breakdown voltage and operating excess bias, even if they do not appear in any FoM, because they give an approximate idea on electric field strength and depletion width, both influencing noise and time jitter performance [49].

In Table I, we computed $\mathrm{FoM_C}$ and $\mathrm{FoM_T}$ considering the maximum PDE. If needed for specific applications, it is still possible to compute the FoM at a particular wavelength. In principle, also $\mathrm{FoM_T}$ should be computed with the intrinsic SPAD time jitter at the desired wavelength. Since timing jitter depends not only on the SPAD itself and on its active area size, but also on readout circuitry and measurement set-up, we computed $\mathrm{FoM_T}$ by employing the best time jitter reported by the respective authors.

For some commercially available SPAD modules ([8]–[10]), we reported DCR at low temperature (instead of room temperature as reported for the other SPADs), since those SPADs

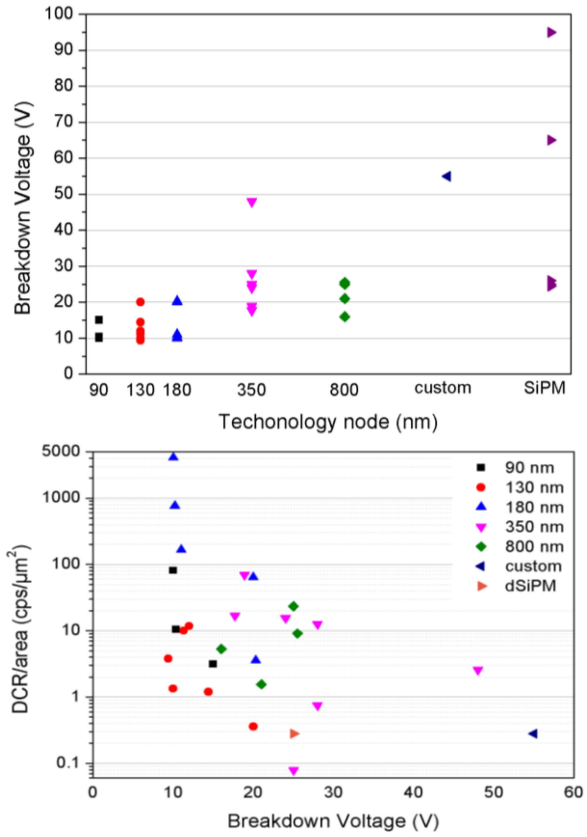

Fig. 3. Breakdown voltage vs. technology node (top) and DCR/area ratio vs. breakdown voltage (bottom) for different technology nodes and CMOS SPADs, all listed in Table I.

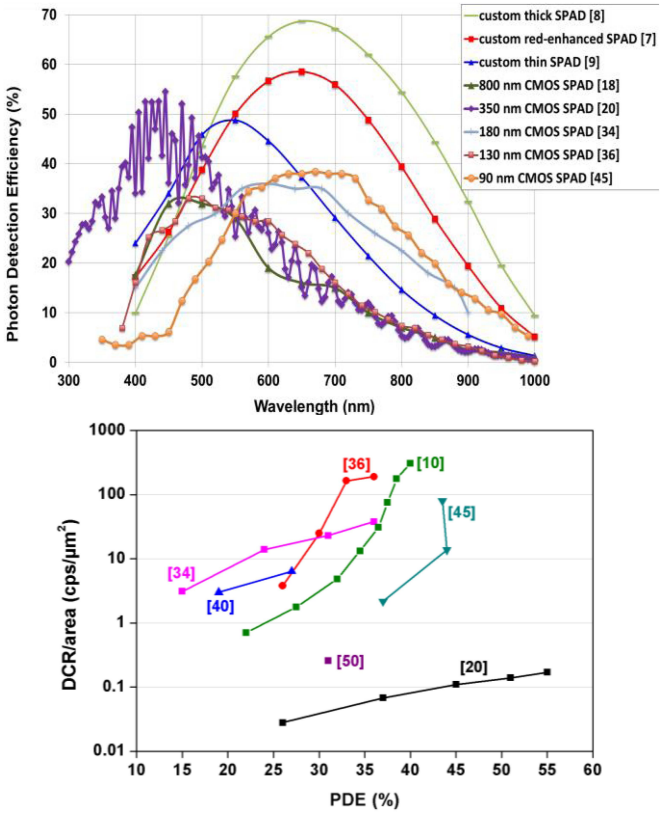

Fig. 4. Spectral Photon Detection Efficiency (top) and DCR/area ratio vs. peak PDE at different excess bias (bottom) for some CMOS technologies and custom SPADs [7]–[10], for comparison.

are internally cooled and no information about DCR at room temperature is reported in the datasheet.

Among CMOS SPADs, the performance of "older" nodes shows minor spread: this is related to the fabrication of almost "standard" structure devices (i.e. shallow p-diffusion in n-well, with p-doped guard-ring). On the contrary, for scaled devices, different structures were proposed: [30], [32], and [33] implemented a standard structure device; [34] and [43] presented a reverse n+/p-well structure. While these structures are not amenable to scaling and thus to improve fill-factor in SPAD arrays, [31] presented an STI-bounded SPAD, where shallow trenches are used as guard-ring in place of low-doped diffusions, thus allowing to shrink SPAD dimension down to 2 μm; and in [39] a scalable n+/p-well diode, with deep n-well insulation is reported.

Nonetheless, all those structures proved to be very noisy because of the high doping concentrations and consequently high electric fields (typical of scaled technologies), which boost tunneling and field-enhanced carrier generation effects. Indeed, as Fig. 3 (top) shows, most of DSM implementations have lower breakdown values resulting in higher DCR/area ratio, due to increased tunneling contribution, as proved by Fig. 3 (bottom). Also, the presence of shallow trenches increases the density of deep-level carrier generation centers at the Si/SiO_2 interface, and the limited duration and effectiveness of annealing and drive-in diffusion steps do not help in reducing impurities, traps, and defects concentrations [35], [36].

However, new structures (especially in 130 nm and 90 nm technologies) were proposed to mitigate the aforementioned effects. In [35], the STI was moved away from the active-area by laying out "dummy" polysilicon; in [37], [40], [42], [44], and [45], a "virtual" guard-ring was used to space shallow tranches from the high-field region, thus avoiding the injection of undesired carriers into the avalanche zone, and proper implant layers were adopted to create junctions where the electric field is lower. In [36] and [41], the STI is surrounded by a p-type passivation to prevent carrier injection (a similar solution is found in [38]) and a lower n-well doping is used to reduce tunneling contribution so that comparable or even better performance are achieved, compared to LOCOS SPADs.

FoM_C and FoM_T values vs. technology node are shown in Fig. 2. It is clearly visible that custom SPADs exhibit better performance than CMOS SPADs, whereas there is no particular trend among CMOS SPADs at different technology nodes. In fact, the overall performance of CMOS SPADs depends more on their structure (guard-ring to prevent edge breakdown, specific diffusions to reduce electric field, ad-hoc structures to reduce crosstalk, such as shallow-trench isolation), and on the cleanness of production processes than on the employed technology node. For instance, the outstanding performance obtained in [20] is mainly related to the much lower DCR/area ratio, at least one order of magnitude better than in other SPADs manufactured in the same technology node, whereas other parameters are comparable.

TABLE II

PDE FOR CUSTOM AND CMOS SPADs WITH HIGHEST EFFICIENCY AND CORRESPONDING COUNTING AND TIMING FIGURES-OF-MERIT AT DIFFERENT WAVELENGTHS AND AVERAGE VALUE IN THE 300 nm – 900 nm SPECTRAL RANGE

Ref.	PDE Peak (%)	PDE @ 650 nm (%)	PDE @ 800 nm (%)	Average PDE (%)	Peak FoM_C (m)	Peak FoM_T (m/s)	@ 650 nm FoM_C (m)	@ 650 nm FoM_T (m/s)	@ 800 nm FoM_C (m)	@ 800 nm FoM_T (m/s)	Average FoM_C (m)	Average FoM_T (m/s)
[8]	70	68.7	54.4	40.8	774	2,213,594	760	2,172,485	602	1,720,279	452	1,290,209
[9]	50	37.2	14.6	25.6	119	3,390,663	88	2,522,654	35	990,074	61	1,736,020
[10]	60	58.6	39.4	34.4	142	1,424,079	140	1,390,850	94	935,145	82	816,472
[14]	73	73	58	47.4	49	61,212	49	61,212	39	48,634	31.8	39,746
[50]	31	11	<1	12.6	15	283,653	5.4	100,651	<0.5	<9,150	6.2	115,291
[52]	45	8	2.5	14.6	0.4	2,173	0.07	386	0.02	121	0.12	705
[54]	56	20	8	32.8	38.5	153,941	13.7	54,979	5.5	21,992	22.5	90,165
[56]	80	17.6	<8	38.8	52.7	323,007	11.6	71,062	5.3	32,301	25.5	156,658
[57]	48.6	8	2.5	12.3	6.4	10,749	1.1	1,769	0.3	553	1.6	2,720
[18]	32	15	6	14.2	2.5	59,979	1.1	28,115	0.5	11,246	1.1	26,616
[20]	55	15.1	5.3	22.4	94.1	1,254,969	25.8	344,546	9.1	120,933	38.3	511,115
[34]	36	34.5	22.5	22	0.03	191	0.03	183	0.02	120	0.02	117
[35]	34	15	4.5	13.7	2.9	20,412	1.3	9,005	0.4	2,702	1.2	8,225
[45]	38	36.8	25.9	20.1	17.1	208,885	16.6	202,289	11.7	142,372	9.1	110,489

TABLE III

MAIN IMAGER PARAMETERS FOR SEVERAL SPAD ARRAYS AND THEIR IMAGING FIGURE OF MERIT

Ref.	Shutter	Processing	# Pixels	Bits/pixel	Pitch (μm)	FF (%)	PDE (%)	DCR (cps)	f_{MAX} (kfps)	Φ_{max} (Mcps)	Power (mW)	FoM_I (kfps)
[17]	-	Multiplex.	4×8	1	75	0.57	17.5	50	70^	16^	-	5
[19]	-	Multiplex.	32×32	1	58	1.14	12	350	70^	24.9	6	131
[64]	-	Event-driven	64×48	1	45	9.6^	26	370	70^	16^	-	4465
[21]	-	Event-driven	4×112	1	25	12.57	40	750	70^	3.9	-	225
[28]	Rolling	Multiplex	128×128	1	25	4.50	20	186	2.4	24.9	363	646
[5]	Global	Parallel	64×32	9+9+9	150	3.14	50	100	100	48	50	15434
[65]	Rolling	Parallel	60×48	8+8	85	0.53	35*	245	46	25	35	393
[26]	Global	Multiplex.	64×4	8	26	34	32	1000	150	5	200	661
[27]	Global	Parallel	32×32	8	100	3.14	43	4000	100	7	165	153
[66]	Rolling	Multiplex.	32×32	1	75	8	42.4	7000	70^	4	-	116
[67] I	-	Multiplex.	1024×8	1	24	4.90	6	80	0.95	16^	-	41
[67] II	-	Multiplex.	1024×8	1	24	44.30	23	5700	0.95	16^	-	168
[68]	-	Multiplex.	128×96	10	44.65	3.19	28	100	70	10	40	7685
[69]	Rolling	Multiplex.	512×128	1	24	5	46	366	156	10	1650	122911

The maximum count rate (Φ_{MAX}) is directly influenced by the afterpulsing probability: reduced afterpulsing allows shortening the dead time, hence to increase the maximum achievable count rate. In particular, DSM technologies benefit from lower excess bias and reduced SPAD (and electronics) area. Both conditions help in reducing afterpulsing probability, thus allowing to boost the count rate [62], [63].

Fig. 4 (top) shows the spectral PDE of custom and CMOS SPADs with the highest reported efficiency. Thick custom SPADs present higher PDE in the Near Infra-Red (NIR) because of the wider absorption region (and higher V_{BD}) than CMOS ones. Ref. [20] reports a CMOS (0.35μm technology) SPAD that reaches the highest peak PDE in the Near Ultra-Violet (NUV) thanks to the use of shallow diffusions that defines the SPAD active volume, but the efficiency drops down in the NIR (see Table II).

No PDE trend is visible moving from submicron to deep sub-micron technologies: indeed the PDE is strictly related to the SPAD design and only marginally dependent on the employed technology node. For instance, the aforementioned alternative DSM implementations reach lower fields and have wider depleted zone, thus exhibiting enhanced and broader spectral response. Conversely, lower PDE values are achieved by standard p+/n-well junction, whose high doping concentrations cause a shrinkage of the depleted layer width.

Fig. 4 (bottom) shows DCR/area ratio vs. peak PDE of some CMOS SPADs reported in Table I, representative of different technological nodes. The lower the DCR at higher PDE, the better is the overall performance of the SPAD.

Concerning the imaging performance, Table III reports the performance of SPAD arrays designed only for photon counting imaging applications as reported in [5], [17], [19], [21], [26]–[28], and [64]–[69]. We excluded from the

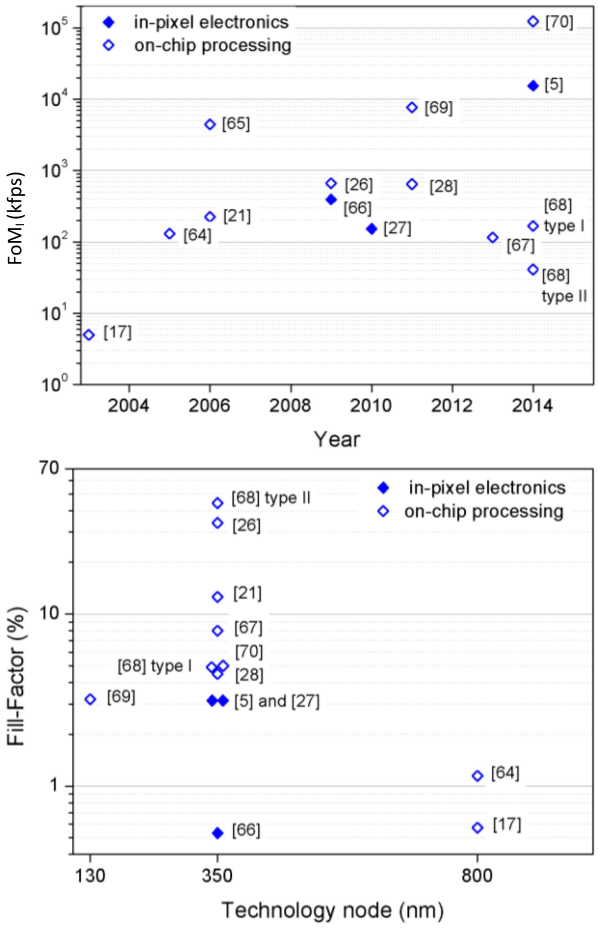

Fig. 5. FoM$_I$ for imaging applications vs. production year (top) and Fill-Factor reached by SPAD imagers in different technology nodes (bottom). Ref. [66] (published in 2013) and [67] (2014) are not shown, since no sufficient data was available to compute the FoM$_I$.

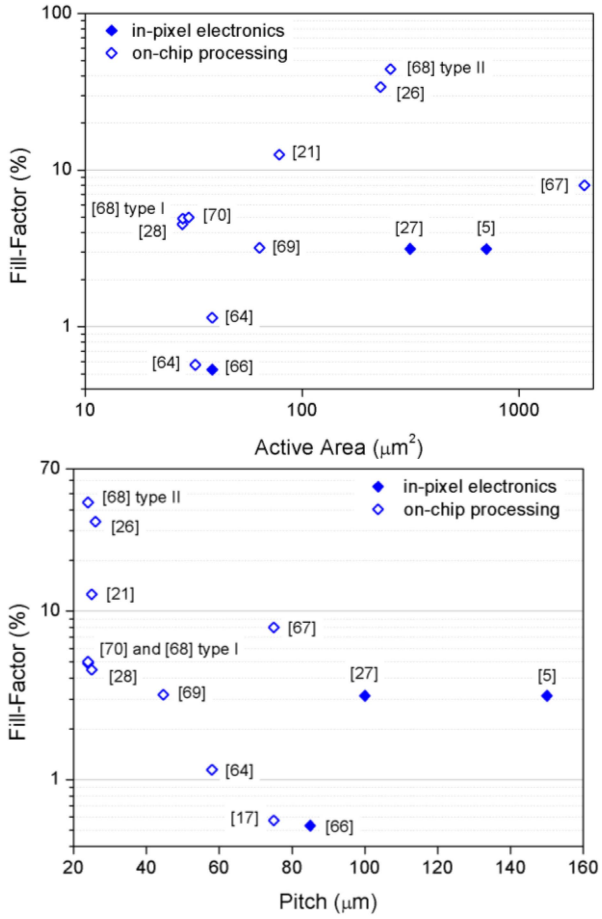

Fig. 6. Fill-Factor of many CMOS SPAD imagers vs. the effective SPAD active area (top) and pixel pitch size (bottom).

comparison the arrays for timing applications (with integrated TDC), because the performance of these sensors depends much more on the timing electronics than on the SPADs itself and this goes beyond the scope of this discussion.

Fig. 5 (top) shows the trend of FoM$_I$ versus year of publication. The clear improvement during time is linked above all to cleaner and more sophisticated technologies and to new features such as shallow trench isolation. Fig. 5 (top) reports the most representative imagers with both in-pixel electronics and those imagers with on-chip, but off-pixel, electronics. Of course, in-pixel electronics affects overall pixel dimensions and, eventually, fill-factor. To this aim, Fig. 5 (bottom) shows the fill-factor of the imagers presented in Table III: as can be seen, arrays with in-pixels electronics show lower fill-factors and more scaled technologies do not result in higher fill-factor, since the SPAD detector itself requires some area overhead (e.g. insulated dependent well, guard-ring, well contact, trench, etc.) that often becomes the ultimate limit to the pixel area.

Even if in-pixel electronics becomes more and more compact in deep-submicron technologies, the desire to reduce the overall pixel pitch forces to design SPADs with smaller and smaller active area. This trend is clearly visible in Fig. 6 (top), where the SPAD active area decrease does not correspond to a simultaneous fill-factor increase. Moreover, Fig. 6 (bottom) shows that the increase of fill-factor in those imagers with 25-30 μm pitch is reached because the electronics is still integrated on-chip, but off-pixel, and not because of the employed scaled technology node.

V. Conclusion

We proposed for the first time three new figures of merit to compare the performance of SPAD detectors, elaborated by analyzing the main SPAD parameters that influence the performance in real photon-timing, photon-counting and imaging applications. The proposed FoMs can help the end-user to choose the most suitable device for the specific application of interest, which can be either the counting of single photons with single or few pixels, the measurement of the photon arrival time with single or few pixels, or the acquisition of both 2D photon-counting and 3D photon-timing images with multi-pixel SPAD arrays.

As expected, we found that custom SPADs present better performance than CMOS SPADs when few pixels are needed, but a fair comparison is often not possible, since datasheets of commercial SPAD modules do not report the DCR at room temperature. Conversely, when multi-pixel arrays are required, CMOS SPADs are the only choice to provide real imaging at single-photon level. Among different CMOS SPADs, the FoMs are not strictly influenced by the manufacturing process nodes, but they also depend on the surface and bulk process cleanness

and uniformity and on the design of the vertical SPAD cross-section and electric field. State-of-the-art CMOS SPADs are designed in 0.35 μm technologies, where very low DCR and very large (30-100μm) SPAD diameters are fabricated, at the expenses of large (5 mm $\times$ 5 mm) chips with just 1k – 2k pixel count. On the contrary, more scaled technologies allow one to exploit advanced cross-sections, hence achieving a much smaller pitch and chip dimensions, and higher (up to 10k-15k) pixel count, but with the drawback of very small SPAD dimensions (few micrometer diameters) and higher noise density.

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