High fill-factor 60×1 SPAD array with 60 sub-nanosecond integrated TDCs

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***Abstract* — This paper presents a high-fill factor 60×1 linear array of Single-Photon Avalanche-Diodes (SPADs) and 60 integrated Time-to-Digital Converters (TDCs). The 100 µm diameter SPAD has high photon detection efficiency (50% at 420 nm), very low dark count rate (2.5 kcps at room temperature) and negligible crosstalk (about 0.1% between adjacent pixels). The TDC resolution is 250 ps and its single-shot precision of 200 ps rms is limited just by the quantization noise. Very good linearity (DNL = 5% LSB rms, INL = 30% LSB rms) is achieved thanks to the sliding scale technique. The overall fill-factor of the array is 52%. This chip is suitable for many advanced spectroscopic applications, since it provides 60 independent single-photon detectors and the corresponding counting and timing electronics within just one integrated circuit.**

***Index Terms* — Single-Photon Avalanche-Diode (SPAD); CMOS imagers; Time-to-Digital Converter (TDC); Time-Correlated Single-Photon Counting (TCSPC); Time-of-Flight (TOF) measurements; Spectroscopy.**

I. Introduction

Single-Photon Avalanche Diodes (SPADs) are solid state devices providing single photon sensitivity at low bias voltage, ruggedness and hardness to magnetic field. They can be used in many biomedical applications, also in combination with Magnetic Resonance Imaging (MRI), and in other scientific and industrial fields. The development of SPADs in CMOS technologies enabled the fabrication of large arrays with in-pixel electronics, both for counting the number of detected photons [1]-[3] and for time-stamping their arrival time [4],[5].

Linear arrays of SPADs generally provide higher fill-factor than squared ones, because the electronics is laid out on one side of the detector. Combined with diffraction gratings, they can be used in spectroscopic applications, to acquire simultaneously different spectral lines, with neither scanning nor moving stages. So far, linear arrays reported in literature have some limitations: either they offer a low number of SPADs [6], or integrate low performance detectors [7],[8], or provide just gated-counting operation [8],[9], or require expensive and bulky external timing electronics [10].

In this paper, we present a 60×1 linear array with large (100 µm diameter) SPADs, which provides single-photon sensitivity and either counts the number of detected photons (photon-counting mode) or directly measures the time delay between a synchronization pulse and the detection of a return photon (photon-timing mode). This array can be used in compact and portable photon-timing detection heads for Raman scattering spectroscopy, in order to extract some specific spectral lines, for Fluorescence Lifetime Imaging (FLIM) or Förster Resonance Energy Transfer (FRET) imaging of samples with relative long time constants, for 3D ranging and LIDAR (Light Detection and Ranging) applications, based on photon Time-of-Flight (TOF), in order to simultaneously detect composition and distance of pollution clouds, etc. Furthermore, the capability to count photons at very high frame rate is demanded in high throughput photon correlation applications, such as Fluorescence Correlation Spectroscopy (FCS), or to study fluids fluxes (e.g. blood flow in arteries), which cause intensity gradients in either transmitted or reflected light.

Section II describes the structure of the SPAD array, Section III presents the performance of the in-pixel SPADs and Time-to-Digital Converters (TDCs), Section IV concludes the paper with a comparison to the present state-of-the-art.

II. Structure of the 60x1 array

The linear array we developed is based on 60 smart pixels, each containing a 100 µm diameter round SPAD detector and a TDC. The chip is fabricated in a standard high-voltage 0.35 µm CMOS technology. Fig. 1 shows the micrograph of the chip, with overall dimension of 9.3 mm x 2 mm, and a zoomed view of some pixels. The pitch is 150 µm and the achieved fill-factor is 52%, much higher than the one achievable with squared arrays (typically 1%-5% with no microlenses [1]-[5]).

Each pixel has a structure similar to the one presented in [11] and [12], but with a wider SPAD. It includes a 6 bit counter (used either to count the incoming photons or as the coarse stage of the TDC) and a 4 bit TDC interpolator. The 60 fully independent pixels operate in parallel, with no multiplexing during either detection or TDC conversion, in a global-shutter mode. Just one time stamp per pixel can be generated in each frame. The maximum frame rate in both photon-counting and photon-timing mode is 1.7 Mfps (i.e. 600 ns minimum frame-time). In photon-counting mode, at every frame the SPAD array provides 60 words of 6 bits each (i.e. the single-frame photon-counting dynamics is 2^6 = 64 photons).

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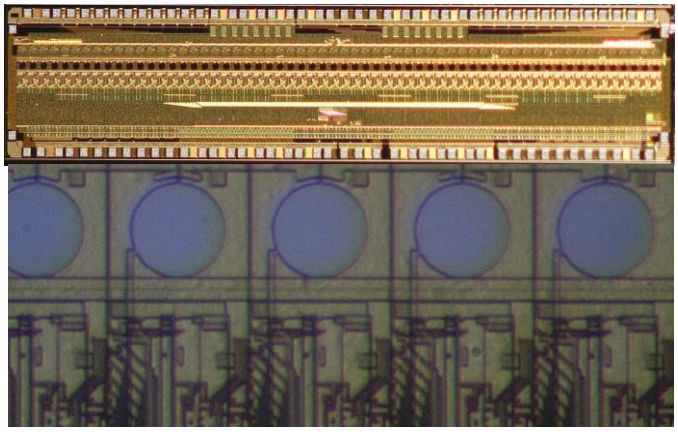

Fig. 1. Micrograph of the 60×1 CMOS SPAD array with TDCs (top) and detail of some pixels (bottom): SPADs have 100 µm diameter and the pitch (i.e. center to center distance) is 150 µm.

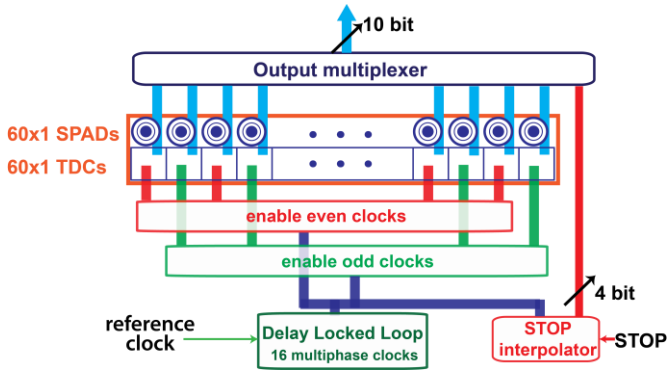

Fig. 2. Schematics of the 60×1 array chip: the DLL generates 16 multiphase clocks (bottom dark blue bus), two separate enable blocks for even and odd pixels let clock signals reach only the enabled pixels (red and green buses), the output multiplexer for readout (cyan buses).

If some applications require increased dynamic range, many frames can be accumulated within the same FPGA used for chip readout. In photon-timing mode, at every frame the SPAD array provides 60 words of 10 bits each (i.e. single-frame time-bin down to 250 ps and 256 ns full-scale range). Even and odd pixels can be independently switched-off in order to further reduce cross-talk probability or obtain more separate confocal acquisition spots.

Simplified schematics of the array chip is shown in Fig. 2: it comprises the array of pixels, the global timing electronics (Delay Locked Loop and STOP interpolator) and the readout circuit. The in-pixel TDC is composed by two stages: a 6 bit coarse counter, providing 4 ns resolution, and a 4 bit fine interpolator, for reaching 250 ps resolution, thanks to a global Delay-Locked-Loop line. The latter generates 16 multiphase clocks dividing the reference clock into 16 intervals: with a 250 MHz clock, such a duration is 250 ps. The START pulse to each TDC is given by the corresponding SPAD, while the STOP is common to all array pixels and is provided by the external electronics (e.g. a pulsed laser). Since START and STOP signals are asynchronous with respect to the reference clock, we exploited the sliding scale technique [13] [14], which improves overall conversion linearity, because different parts of the TDC characteristic are exploited to convert the same time interval. In this way TDC non-linearities are transformed into stochastic jitter.

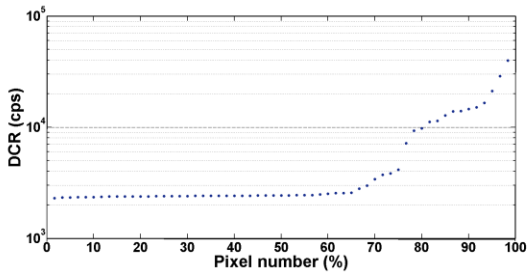

Fig. 3. Dark Count Rate (DCR) distribution at V_{EX} = 5 V and at room temperature of the 100 µm CMOS SPADs of the array chip.

The photon-timing resolution, i.e. the LSB (Least Significant Bit) of the TDC, can be adjusted from 250 ps to 800 ps, by simply changing the reference clock frequency from 250 MHz to 80 MHz. Since the TDCs provide 10 bits, the Full Scale Range (FSR) consequently ranges from 256 ns to 820 ns.

III. Array Characterization

We characterized the performance of SPADs and TDCs. In summary, SPADs have low Dark Count Rate (DCR) of 2.5 kcps at room temperature, and high Photon Detection Efficiency (PDE) in the near-UV of 50 % peak at 420 nm (without considering fill-factor). TDCs show excellent Differential Non-Linearity (DNL), just 5.3% LSB rms.

A. SPAD performance

In [15] we presented an experimental characterization of SPADs fabricated in the same 0.35 µm technology. Fig. 3 shows DCR distribution of the SPAD array at 5 V excess bias (V_{EX}), with no cooling. The median DCR in timing mode is 2.5 kcps, slightly higher than the DCR of a single 100 µm SPAD [15] because, with no cooling, the power dissipation of the timing electronics increases the temperature of the chip. Such DCR increase indicates a temperature increase of about 5°C, which causes a breakdown variation of about 600 mV, a consequent reduction of the excess bias and, eventually, a variation of the PDE of less than 5%. The DCR density (i.e. DCR per unit area) is as low as 0.32 cps/µm^2, which is better than the best single CMOS SPADs reported in literature (0.36 cps/µm^2 [16], 0.75 cps/µm^2 [17], 1.19 cps/µm^2 [18]).

At V_{EX} = 5 V the PDE is 50% at 420 nm, 20% at 300 nm and 650 nm, and 5% at 800 nm. The high PDE in the near ultra-violet was achieved thanks to a thin antireflection coating, optimized for those wavelengths.

We measured the crosstalk probability by keeping the array in a dark box and by operating it in timing mode: SPADs were activated with 300 ns gate windows and the arrival time of one ignition per frame per pixel was recorded, until reaching about 10^7 events. The cross-correlation between the measured arrival times in adjacent pixels was then computed and the theoretical cross-correlation with no crosstalk (a triangular distribution, from -300 ns to +300 ns) was subtracted. The final cross-correlation histogram is shown in Fig. 4. The crosstalk probability *Xtalk* can be computed as:

$$Xtalk = \frac{N_{xy}}{N_x + N_y} \quad (1)$$

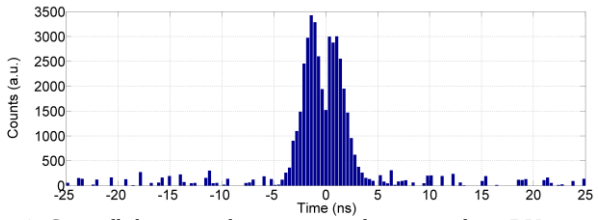

Fig. 4. Crosstalk histogram between two adjacent pixels at 5 V excess bias, with 10^7 counts per pixels.

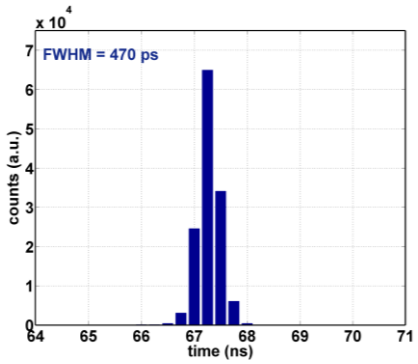

Fig. 5. Single-shot precision of one pixel of the array, where each bin (i.e. LSB) is 250 ps.

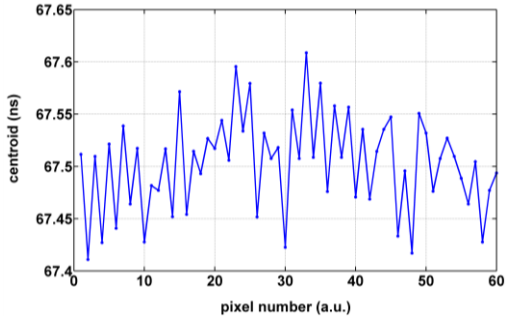

Fig. 6. Centroid of the arrival time histogram (about 150,000 conversions) in each pixels of the array.

where N_x and N_y are the total counts accumulated in pixel x and y, considering only the ideal triangular distribution, and N_{xy} are the counts within ±5 ns in the cross-correlation histogram [19]. Such ±5 ns time window was selected because there is no cross-correlation outside this time interval, as shown in Fig. 4. The crosstalk histogram presents two peaks, one due to pixel x that causes crosstalk on pixel y and vice versa for the other one. The crosstalk probability at 4 V, 5 V, 6 V excess bias between adjacent pixels is 0.078%, 0.13%, and 0.18%, respectively, whereas crosstalk between non adjacent pixels is lower than 10^{-7}.

B. TDC performance

We measured the single-shot precision (i.e. the standard deviation of TDC conversions when a constant time interval is measured many times) and the linearity of all TDCs. We set the TDC resolution at 250 ps and employed a pulsed laser at 850 nm with 40 ps Full Width at Half Maximum (FWHM). The timing jitter of the 100 µm SPAD at 850 nm is about 300 ps FWHM [15]. For each pixel, we acquired about 150,000 conversions, resulting in an overall single-shot precision of 200 ps rms (i.e. 470 ps FWHM), for each SPAD+TDC, and a pixel-to-pixel variance on the jitter of just 23.7 ps rms over the whole array.

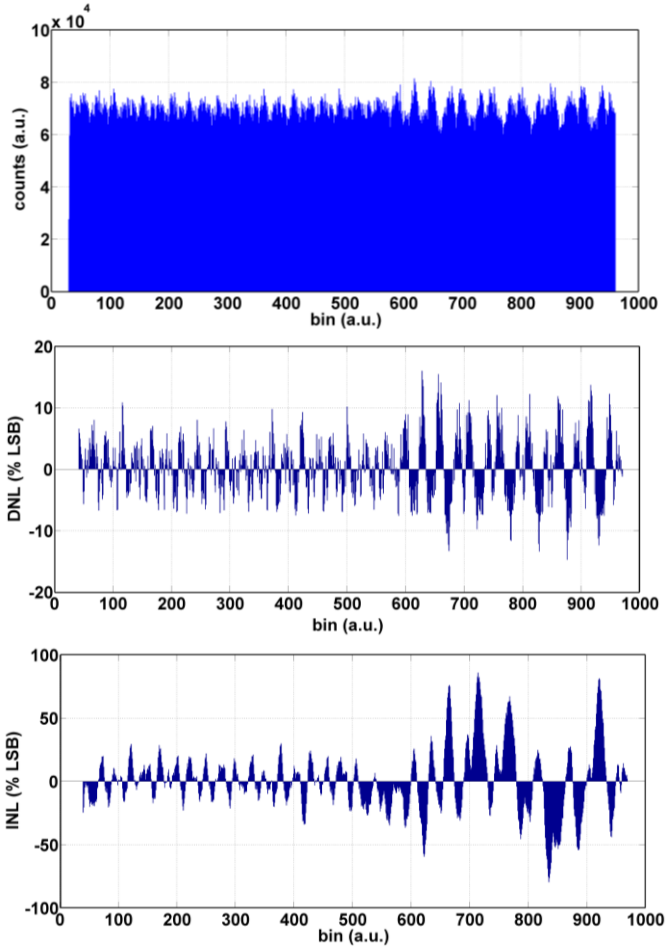

Fig. 7. Code density test (top), with 70,000 counts per each TDC bin, computed DNL (center), and INL (bottom).

The typical timing response of one pixel of the array to a narrow (FWHM < 40 ps) pulsed laser is shown in Fig. 5, whereas Fig. 6 shows the very good uniformity across the array: the maximum difference in the centroids of the 60 pixels is just 205 ps (less than one bin) and their standard deviation is 46.5 ps rms.

We tested Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) through a code density test, by collecting about 70,000 uniformly distributed counts per TDC channel (Fig. 7 top). In the computation of DNL and INL we skipped the first and last 10 ns of the gate window, since those data are affected by the gate-on/gate-off edges. Center and bottom plots of Fig. 7 show DNL and INL of one pixel of the array over the TDC range. The average DNL and INL across all pixels are 5.3% LSB rms and 30.2% LSB rms, respectively. Such a good linearity is due to the TDC architecture implementing the sliding scale technique. This performance can be further improved with a better layout of the printed circuit board, since we noted a strong coupling between the 100 MHz readout clock and the TDC reference clock, which causes a disturbance at 100 MHz, clearly visible in the code density test of Fig. 7. A deterioration of the linearity is also visible for long measured time (i.e. START at the beginning of the range), because of power supply disturbances due to the switching of digital signals at the beginning of a new frame.

IV. Conclusions

We presented a 60×1 linear array with large (100 µm diameter) SPADs, the highest (52%) fill-factor presented in literature for SPAD arrays and 250 ps resolution TDCs.

In Table 1, we compare the main characteristic of the present array with other linear SPAD arrays developed in either CMOS [8]-[10] or custom [6] technologies. Only the one reported in Ref. [6] is a complete system with two separate chips, one with 32x1 SPAD detectors and the other one with 32x1 channels of timing electronics (Time-to-Amplitude Converter, TAC), but it achieves lower fill-factor (15.7%) and higher DCR (7.3 kcps with 50 µm diameter SPADs). In Ref. [8], very large arrays were presented for Raman Spectroscopy, with a 1 bit gated counter (gate window adjustable with 250 ps steps) integrated into each pixel. Two arrays were described therein: a first one shows low DCR, but also low fill-factor (4.9%) and low PDE (6% peak), whereas a second type achieves high fill-factor (44.3%), but also high DCR (5.7 kcps for a 255 μm^2 active area SPAD). The 64x1 array presented in Ref. [9] has 15.8 µm side SPADs with good performance (34% fill-factor, 32% peak PDE and 1,000 cps DCR) and was designed for FLIM applications. However it provides only time gated counting, with gate windows adjustable at steps of 800 ps. Finally, in Ref. [10] an array of high performance SPADs (50% PDE and 150 cps DCR with 50 µm diameter SPADs), developed in the same technology of this work, is reported, but with no on-chip electronics. In conclusion, the array presented herein successfully combines SPADs with extremely good detection performance and accurate integrated TDCs with high linearity.

The performance of our SPADs in terms of PDE and DCR density is comparable with the best arrays of SPAD in custom technologies. Better timing performance could be achieved with expensive and bulky multi-channel timing electronics, but since this array integrates both sensor and electronics in a single chip it can be successfully employed in compact Raman spectrometer, in which high fill-factor and low DCR are fundamental requirements, and timing information is used just to distinguish Raman scatters from fluorescence (nanosecond resolution is enough), or in portable FLIM systems, which requires hundreds of picosecond resolution and multispots with high collection area in order to increase the throughput of the measurement.

TABLE I. Comparison of different linear SPAD arrays.

Ref.	*number of pixels*	*fill-factor (%)*	*pitch (µm)*	*DCR (cps)*	*peak PDE (%)*	*integrated electronics*
this work	**60×1**	**52**	**150**	**2,500**	**50**	**TDC (250 ps resolution 5.3% LSB DNL)**
[6]	32×1	15.7	250	7,300	44	external processing
[7]	4×112	-	25	6	5.3	external processing
[8] type I	1024×8	4.9	24	80	6	time gated counters
[8] type II	1024×8	44.3	24	5,700	23	time gated counters
[9]	64×1	34	26	1,000	32	time gated counters
[10]	32×2	20	100	150	50	external processing

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