A Simple Technique for Signal Compression in High Dynamic Range, High Speed X-ray Pixel Detectors

C. Fiorini, B. Nasri, S. Facchinetti, L. Bombelli, P. Fischer, and M. Porro

I. Introduction

THE availability of high-intensity and high repetition rate X-ray sources, like XFEL (X-ray Free Electron Laser) facilities, imposes severe constraints for the detectors to be developed, in terms of high speed and high dynamic range. For the European XFEL in Hamburg (Germany), different detection systems are under development to operate with X-ray flashes with a repetition rate of 4.5 MHz with a dynamic range up to 10^4 photons and beyond [1]. These systems have to provide, on the one hand, a sufficiently low electronics noise to allow single photon detection at low signal intensities. On the other hand, they have to provide a compression of the signal at high photon fluxes, when single-photon resolution is no more necessary, in order to cope with the available dynamic range of the processing circuit and of the analog-to-digital converter. In this framework, different compression techniques may be adopted to cope with the high dynamic range. Among different solutions that have been proposed, we recall here three examples, implemented in X-ray detection systems under development for the European XFEL. In the first one, adopted in the DSSC system [2], when the incoming charge increases, it is stored in different regions of an internal gate of the DEPFET detector, characterized by lower gains of the device. In the second one, adopted in the AGIPD circuit [3], the gain of the preamplifier is dynamical switched to lower values when the input charge increases. In the third one, adopted in the LPD detector [4], a series of parallel gain stages ($1\times, 10\times, 100\times$) follows the preamplifier to guarantee the appropriate gain value.

In this work, we explore the feasibility of an alternative solution which provides compression of the signal at high intensities, still keeping the low noise necessary to provide single photon identification at low intensities. The peculiarity of this solution is its simple implementation, as it regards only the first transistor of the front-end (FE) electronics and does not involve the next stages of the filter. Moreover, it is compatible with the use of detectors without the FE transistor integrated in the detector chip. The solution has been designed to be compatible with the ASIC already designed to readout the DEPFET in the DSSC detector, but its use can be more generally extended to other readout circuits. A first prototype of the proposed FE has been realized in 130 nm IBM technology and the results of the experimental characterization, including first X-ray measurements of the chip connected to a detector, are reported in the work. Finally, possible improvements of the design to allow the response of the circuit to match a desired compression shape are discussed.

II. The Compression Principle

The FE circuit here proposed is based on an input PMOSFET transistor placed on the readout chip connected to the pixel detector by bump bonding (Fig. 1). The signal charge is directly converted into voltage on the total capacitance at the detector output. The PMOSFET reads this voltage and delivers a current signal which is fed into the virtual ground at the input of the filter, as proposed in previous current-readout circuits [5]. The PMOSFET is optimized for low-noise readout of single X-ray photons at low intensities. This is achieved by the operation of the transistor in saturation regime and with a value of trasconductance (gm) sufficiently large to overcome the relatively large value of total capacitance Cd due to the external connection of the detector with the FE stage. The compression

Manuscript received March 28, 2014; revised July 07, 2014; accepted July 16, 2014. Date of publication August 21, 2014; date of current version October 09, 2014. This work was supported by XFEL GmbH in the framework of the DSSC project.

C. Fiorini, B. Nasri, and S. Facchinetti are with Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria, 20133 Milano, Italy, and also with INFN Sezione di Milano, 20133 Milano, Italy (e-mail: carlo.fiorini@polimi.it).

L. Bombelli is with XGLab s.r.l., 20133 Milano, Italy.

P. Fischer is with the Institut für Technische Informatik der Universität Heidelberg, 69117 Heidelberg,Germany.

M. Porro is with Max-Planck-Institut für Extraterrestrische Physik, Giessenbachstrasse 1, 85748 Garching, Germany.

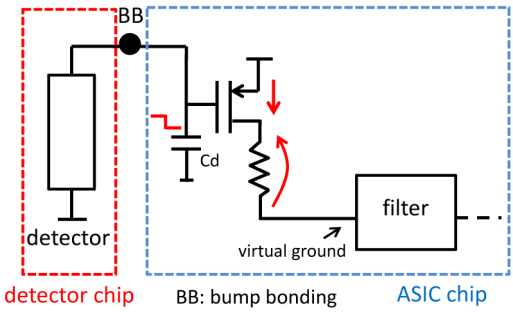

Fig. 1. Principle of the proposed compression mechanism, based on an input PMOSFET driven toward triode region by the voltage drop on a resistor connected between its drain and the filter.

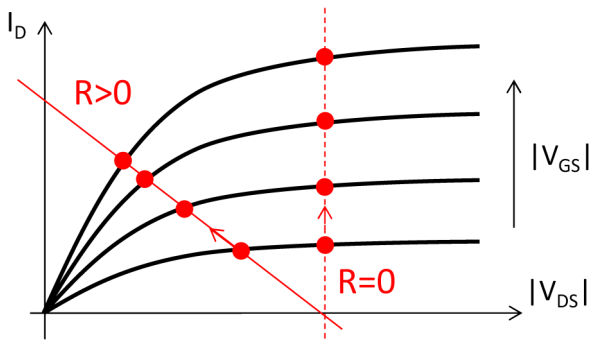

Fig. 2. Characteristics of the PMOSFET showing the operating points in the triode region when increasing the gate voltage ($R > 0$). For comparison, the situation with the transistor operating in saturation ($R = 0$) is also reported. All voltages are represented in absolute value.

of the PMOSFET gain when the signal intensity increases is obtained by pushing the transistor to operate in the triode (ohmic) regime through a resistor connected between the transistor drain and the virtual ground of the filter. When the signal at the gate of the PMOSFET increases (larger $|V_{GS}|$ in the characteristics curves of Fig. 2), the voltage drop on the resistor becomes larger and this pushes the transistor to operate deeper in triode regime with a reduced $|V_{DS}|$. Thus, the transistor current still increases (following the straight line in Fig. 2 for $R > 0$) but with a decreasing gain, lower than in the case of the transistor operated in saturation region ($R = 0$ in Fig. 2), for the same variation of $|V_{GS}|$. This produces a compression in the FE current response.

III. Implementation with the Flip-Capacitor-Filter

The proposed FE is connected to the same filtering amplifier designed for the readout of the DEPFET detector in the DSSC project (Fig. 3). The filter is based on the flip-capacitor concept [6], where a double integration is performed using a single amplifier and flipping the capacitor between the two integrations, leaving at the end the subtraction of the results of the two integrations. A programmable current source subtracts the PMOSFET bias current before filtering operation to exploit the maximum dynamic range of the filter. A reset of the gate of the input PMOSFET has been added to restore the nominal bias voltage after signal processing.

A prototype of the circuit, shown in Fig. 4, has been designed and produced in the 130 nm IBM technology (1.2 V power

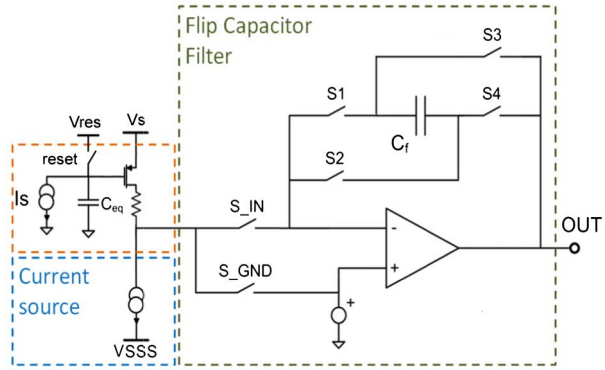

Fig. 3. The proposed PMOSFET-resistor FE coupled to the flip-chip filter. The bottom side of the resistor is kept to fixed voltage during the operations of the filter (I integration, capacitor flip, II integration). The current generator connected to VSSS is used to subtract the bias current of the PMOSFET and fed the filter with the signal current only.

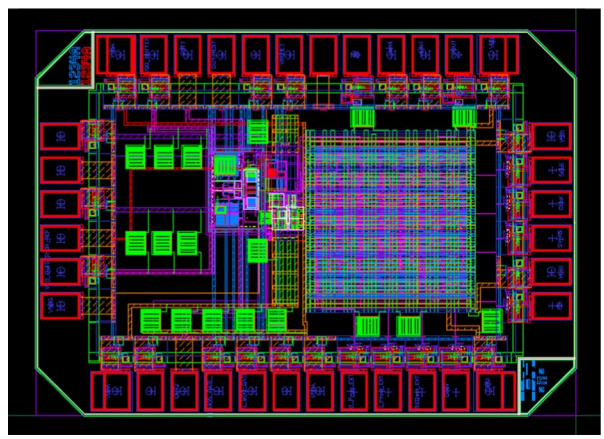

Fig. 4. Layout of the chip produced in the IBM 130 nm technology.

supply). The goal of this prototype was to verify the proof of principle of the proposed solution and also to make a preliminary noise evaluation by connecting the chip with a test detector to perform X-ray measurements.

IV. Experimental Results

Fig. 5 shows the measured characteristics of the PMOSFET-resistor stage in the produced chip. The current response at various gate voltages is reported in figure, showing the compression behavior. The corresponding transconductance *gm* is also shown in the graph. The transconductance rises at the beginning for an increase of $|V_{GS}|$, when the transistor is still in saturation region of operation. Then it starts to decrease at larger $|V_{GS}|$ because the transistor enters in the triode regime of operation and further current increments are smaller, as also qualitatively shown in Fig. 2 for $R > 0$. The transistor has to be operated at the 'optimum' gate bias point which provides the maximum of *gm*. This condition provides the lowest possible electronics noise which is necessary for single-photon detection. The transistor gate voltage is restored at this nominal bias point by activating the reset (Fig. 3) after the completion of the signal processing. In the measurements shown in Fig. 5, the PMOSFET drain is kept to 0 V while the voltage *Vref* at the bottom end

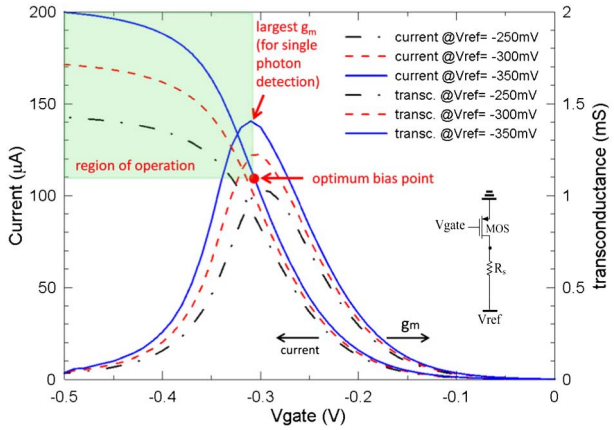

Fig. 5. Measured characteristics curves of the PMOSFET-resistor stage at various gate voltages. The current and the corresponding transconductance are reported in the graphs. The measurements are performed for various voltages differences between PMOSFET drain (kept to 0) and the resistor bottom electrode.

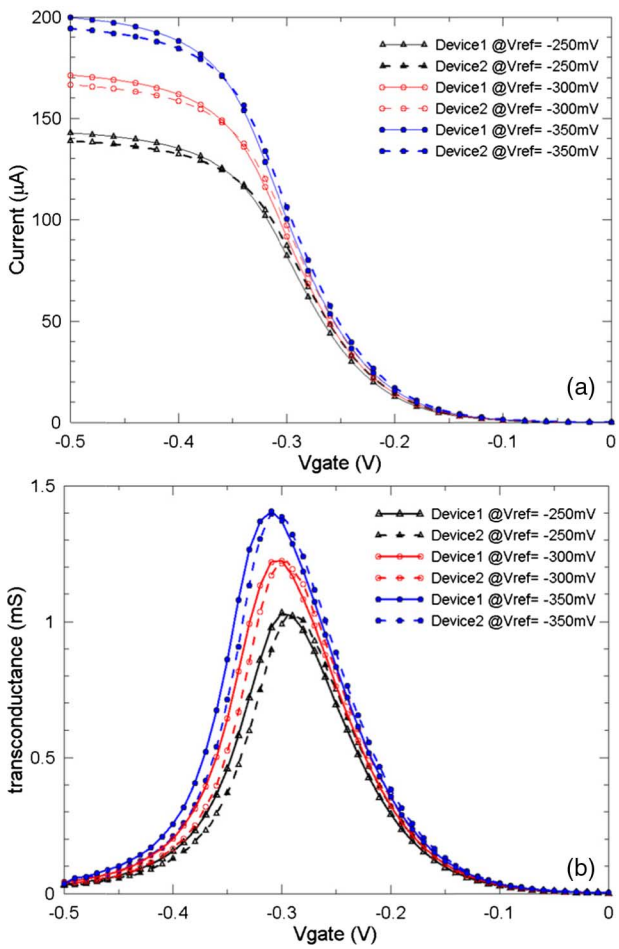

Fig. 6. (a) I/V characteristics measured for two devices, at different reference voltages. (b) Corresponding trasconductances.

of the resistor (see inset in Fig. 5) is varied at three different values to tune the characteristics response of the device, and correspondingly its *gm*. The value of the resistor R_s is 1.7 kΩ.

Although an extended characterization of several samples has not been made in this work, in Fig. 6 the characteristics measured on two devices are reported and compared. The

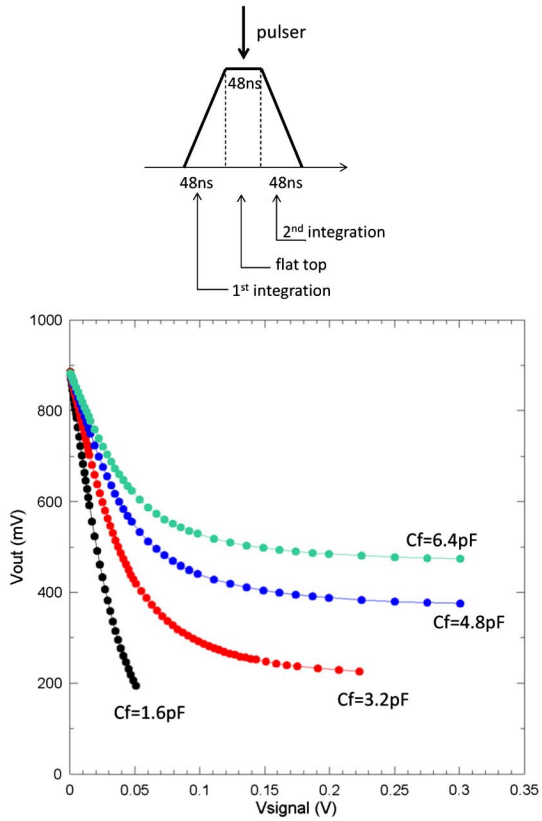

Fig. 7. Output response of the filter for various amplitudes of the voltage pulses given at the gate of the input PMOSFET. Amplitudes are represented in absolute values. In the upper side of the figure, the timing diagram used for the filter in the measurements is reported.

differences in the measured characteristics are rather small, confirming the Monte Carlo simulations previously carried out for the chosen technology, considering mismatch of the devices only. We consider the mismatch-only condition quite representative for pixels inside the same detector array, while process variations may have impact on devices belonging to different wafers. Process variations may be compensated globally for all pixels in an array by properly adjusting the bias point of the gate voltage, which is common to all pixels. Beside these preliminary considerations, we are conscious that the statistical variation of the devices parameters in the proposed solution is a key aspect to be evaluated and this will be specifically investigated in future work.

Fig. 7 shows the output of the circuit of Fig. 3 when a test signal of different amplitudes is applied at the PMOSFET gate. The gain of the filter can be modified by changing the value of the feedback capacitor C_f. The timing of the operation of the filter is performed in order to implement the weighting function reported in the upper side of Fig. 7. The input pulse is applied during the flat-top of the weighting function. The duration of the two integrations as well as of the flat-top is 48 ns. The flat-top value is considered sufficient to cope with the duration of signal generation in the detector and in the FE. The output of the filter shows again the expected compressing behavior. The appropriate setting of the feedback capacitance allows to better exploit the output range of the filter for a given dynamic range at the input.

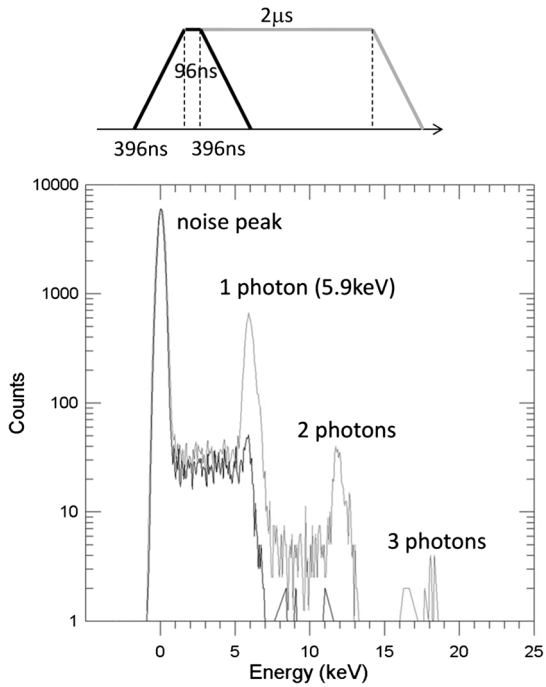

Fig. 8. Spectra of ^{55}Fe source measured with the chip connected to a SDD. The timing of the filter used in the measurements is reported in the upper side of the figure. The spectrum in gray is measured with 2µs flat top, while the spectrum in black is measured with 96 ns flat top.

X-ray measurements with the prototype have been carried out connecting the circuit to a Silicon Drift Detector (SDD) as test detector. The small anode capacitance of the SDD can be considered representative of the output capacitance of a pixel detector. In addition, the relative large area of the SDD (10 mm^2 in our prototype) made X-ray detection rather effective during the tests. The SDD has been cooled to $-20°$C to make negligible the contribution to the noise due to the leakage current. The anode of the SDD has been connected to the input pad of the circuit by wedge bonding. This setup was not optimal to minimize the capacitance seen by the detector and the main contribution was the input pad of the ASIC. We have estimated a total capacitance of about 1.1 pF, including: detector, bonding, pad and PMOSFET gate. This value is expected to be significantly reduced in the future by connecting the circuit to a pixel detector by bump bonding (0.3 pF - 0.5 pF total capacitance).

Fig. 8 reports the measured spectra of a ^{55}Fe source irradiating the SDD. To increase the probability of full-amplitude measurements of the X-rays events, whose occurrence is asynchronous with respect to the timing of the filter, the flat-top of the weighting function has been purposely extended to 2 μs, as shown in the filter timing diagram in the upper section of Fig. 8 (gray line). The duration of the two integrations was set to 396 ns, to first evaluate the best electronics noise before using shorter values. In the spectrum (gray line), detection of single 5.9 keV photons is visible, as well as detection of two and three photons which sum occasionally during the flat-top. The electronics noise estimated from the noise peak is of 65 e- rms.

Fig. 8 also reports the spectrum of the ^{55}Fe source with the filter timing shown in black in the upper side of the figure. Here the flat-top has been shortened to 96 ns, a condition much closer

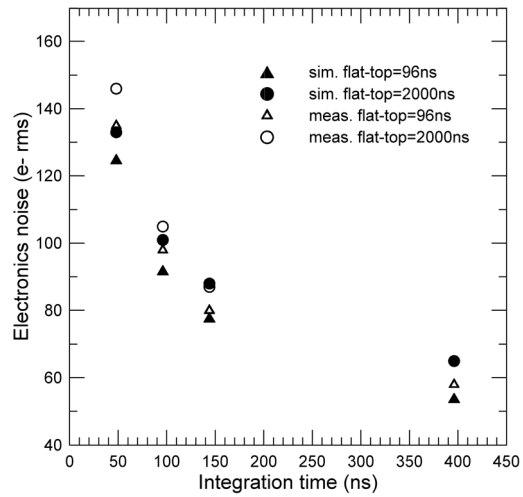

Fig. 9. Comparison of measured ENC with values calculated from (1) using the parameters listed in the text. The ENC is reported for different values of integration time and flat-top of the filter.

to the real operation with XFEL where the filter timing can be synchronized with the occurrence of the X-ray events. In this case, the ^{55}Fe spectrum results obviously smeared (black line) because only a minority of events can be detected with full amplitude, i.e. within the flat-top duration. However, the measurement can still be used to quote again the noise with this filtering timing. The noise is 58 e- rms. The slight improvement with respect to the previous measurement can be justified by the better performance of the filter with the shorter flat top with respect to the 1/f noise contribution [7].

Spectra of ^{55}Fe source have been measured also using shorter filtering time, which is of interest for a faster processing in XFEL applications. With the shortest filtering time using 48 ns for each integration and 48 ns for the flat top, the measured electronics noise is of 135 e- rms.

We have compared the noise value measured for different processing time with a theoretical estimation that can be made according to the well-known ENC (Equivalent Noise Charge) formula [8] which is reported as follow (neglecting the contribution of the parallel noise due to the leakage current):

$$ENC^2 = C_T^2 \alpha \frac{4kT}{gm} A_1 \frac{1}{\tau} + 2\pi C_T^2 a_f A_2 \qquad (1)$$

where: C_T is the total capacitance, α is a factor ~ 1 for short channel MOSFETs, *gm* is the transconductance, a_f is the 1/f noise coefficient, A_1 and A_2 are the filter noise coefficients and τ is the shaping time (the integration time in our case). In Fig. 9, the measured ENC at various integration times and flat-top durations is compared with the theoretical value calculated from (1) using the following parameters: $gm = 1.0$ mS, $C_T = 1.1$ pF, $\mathrm{a_f} = 4 \cdot 10^{-12}$ V^2, which are in satisfactory agreement with measurements and technology data.

Eq. (1), where the noise contribution of the leakage current has been neglected, shows that the main noise components of the ENC are all proportional to the value of the input capacitance. Therefore, a lower value of C_T foreseen in future using bump bonding would correspond to a lower noise. It has to be

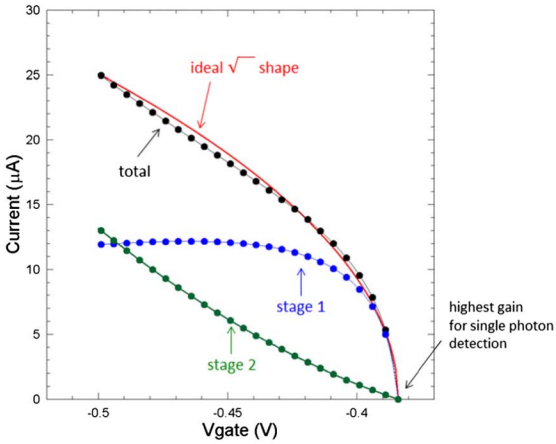

Fig. 10. Example of the use of two stages in parallel in order to better approximate the desired shape of the compression, a 'sqrt' shape in this example. Current and voltage values in the graph are indicative, as obtained from basic device models calculations and not from technology simulations. The current is reported as signal current only, i.e. the value zero in the graph correspond to the PMOSFETs biased only with the nominal bias current ('optimum bias point' in Fig. 5).

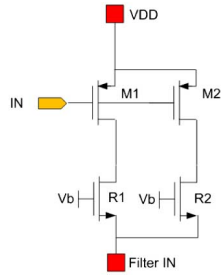

Fig. 11. Principle schematic of the implementation of the two stages considered in Fig. 10. Two PMOSFETs are used in parallel, one with higher gain (M1) and one with lower gain (M2). The fixed-value resistor in each branch is replaced by a NMOSFET which exhibits low resistance for low signals and high resistance for large signals.

pointed out, however, that a reduction of the capacitance at the input node of the circuit reduces the noise but also increases the voltage swing at this node for the same signal charge. A compromise between noise and voltage dynamic range at the input node has therefore to be found.

V. Shaping the Compression Response

In this section, we introduce some ideas on how to improve the compression behavior of the FE response. In potential applications of the proposed technique, a suitable 'shape' of the compression curve may be in fact required. A custom shape may be obtained by adding more stages in parallel of the PMOS + resistor unit and optimizing the behavior of each stage. An example of optimization of the FE response is schematically reported in Fig. 10. In this example, a 'square root' shape of the compression is desired, in order to make the best use of the quantization of the ADC for the given dynamic range of the signal and with respect to its statistical fluctuation [9]. The desired shape can be obtained by using two stages in parallel: the two stages are implemented as shown in Fig. 11. Here a further modification with respect to the basic scheme of Fig. 1 is introduced: in each stage, a NMOSFET replaces the resistor to change the resistance with the signal intensity. The NMOSFET is biased at a suitable bias Vb. Considering stage 1 composed by M1 and R1, when the signal current is zero, the NMOSFET operates in the triode regime, so with a value of R1 very small. In this condition, the PMOSFET M1 works in saturation with high *gm* for noise minimization. When the signal increases, the NMOSFET moves from triode to saturation regime, increasing the value of R1. This brings M1 into triode regime, reducing its gain. The result is the response for stage 1 reported in Fig. 10. In stage 2, composed by M2 and R2 in Fig. 11, the PMOSFET has a lower W/L with respect to M1 (W and L are, respectively, the width and the length of the transistor channel). This second stage does not contribute to the overall response for small signals, which is dominated by stage 1. However, its smoother response, reported in Fig. 10, adds to the main one and dominates the response of the FE for larger signals. The overall I/V characteristic resulting from the sum of the two stages can be tailored to be a good approximation of the desired 'sqrt' curve, as reported in Fig. 10. The proposed approach can be further extended by using more than two stages in parallel, with different choices of PMOSFETs and NMOSFETs. In the additional stages, the NMOSFET can be even eliminated if the I/V characteristic of the PMOSFET alone is already suitable.

Finally, for what concerns noise evaluation, considering stage 1 only which is dominating for single photon detection, we point out that the noise contribution of the NMOSFET R1 is negligible with respect to the main noise contribution due to M1, as R1 is operating in triode regime and its noise current is circulating mainly into R1 itself, almost cancelling its contribution to the output current (which is fed at the input of the filter). This cancellation is similar to the cancellation of the current noise contribution of a 'cascode' transistor in a conventional 'cascode' amplifier.

VI. Conclusions

In this work we have presented a compression technique which could be adopted in pixel detectors for XFEL applications characterized by single-photon detection capability at low intensity and by high dynamic range for high intensity of photon fluxes. The technique is rather simple as it is based on an input PMOSFET which is pushed to work in the triode region, therefore with a lower gain, when the signal increases. The charge to voltage conversion is obtained directly through the gate of the transistor while the voltage signal is amplified by the transistor trasconductance. This voltage-amplification strategy is, of course, not optimal compared to a charge preamplifier because the conversion depends on the total capacitance at the anode of the detector. This includes the contribution of the bonding capacitance which may depend from channel to channel. Our choice was, however, mainly dictated by keeping the same voltage-amplification strategy already adopted for the DEPFET detector and it maintains compatibility with the following stages of the FE electronics. The proposed solution is foreseen to be implemented in a pixel detector where each pixel is bump-bonded to a corresponding channel of the readout ASIC. In the first implementation of the detector, we will evaluate carefully the channel-to-channel gain uniformity

in relation to possible differences of input capacitance and to statistical variations of devices parameters.

The proof-of-principle of the technique has been verified in a first prototype. Using the prototype with a SDD test detector, X-ray measurements have been carried out to assess the electronics noise performances which are in line with theoretical evaluations. To optimize the compression profile of the response of the FE, more stages can be used in parallel, each one implementing a NMOSFETs instead of the resistor, to have a variable resistance in the signal range. An optimized design will be implemented in a next prototype.

Acknowledgment

The authors would like to thank S. Masci for the mounting and bonding of the detectors and F. Erdinger and K. Hansten for discussions.

References

[1] [Online]. Available: http://www.xfel.eu/research/detectors/

[2] M. Porro *et al.*, "Development of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame readout capability for the european XFEL," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pt. 2, pp. 3339–3351, Dec. 2012.

[3] S. Xintian *et al.*, "A low noise high dynamic range analog front-end ASIC for the AGIPD XFEL detector," in *Proc. 19th IEEE Int. Conf. Electronics, Circuits and Systems (ICECS)*, 2012, pp. 933–936.

[4] M. Hart *et al.*, "Development of the LPD, a high dynamic range pixel detector for the European XFEL," in *Proc. Nuclear Science Symp. and Medical Imaging Conf. (NSS/MIC)*, 2012, pp. 534–537.

[5] L. Bombelli, C. Fiorini, M. Porro, S. Herrmann, and S. Wölfel, "VELA: The CMOS circuit based on fast current read-out for X-Ray spectroscopy with DEPFET," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 1359–1366, Aug. 2007.

[6] S. Facchinetti *et al.*, "Characterization of the flip capacitor filter for the XFEL-DSSC project," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 4, pt. 2, pp. 2032–2038, Aug. 2011.

[7] M. Porro, C. Fiorini, and L. Strüder, "Theoretical comparison between two different filtering techniques suitable for the VLSI spectroscopic amplifier ROTOR," *Nucl. Instrum. Methods Phys. Res. A*, vol. 512, pp. 179–190, 2003.

[8] E. Gatti, P. F. Manfredi, M. Sampietro, and V. Speziali, "Suboptimal filtering of $1/f$-noise in detector charge measurements," *Nucl. Instrum. Methods*, vol. 297, no. 3, pp. 467–478, Dec. 10, 1990.

[9] M. Porro *et al.*, "Expected performance of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame readout capability for the European XFEL," *Nucl. Instrum. Methods Phys. Res. A*, vol. 624, no. 2, pp. 509–519, 2010.