A 1.7 GHz Fractional-N Frequency Synthesizer Based on a Multiplying Delay-Locked Loop

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I. Introduction

FREQUENCY synthesizers based on the phase-locked loop (PLL) have a stringent tradeoff between integrated phase noise and dissipated power. Furthermore, this compromise is directly affected by the typical noise/power tradeoff of voltage-controlled oscillators (VCOs) [1]. For this reason, high-performance applications such as wireless frequency generation still rely on PLLs based on LC oscillators [2]–[5], which have better noise/power compromise than ring oscillators. Unfortunately, monolithic inductors do not benefit from technology scaling.

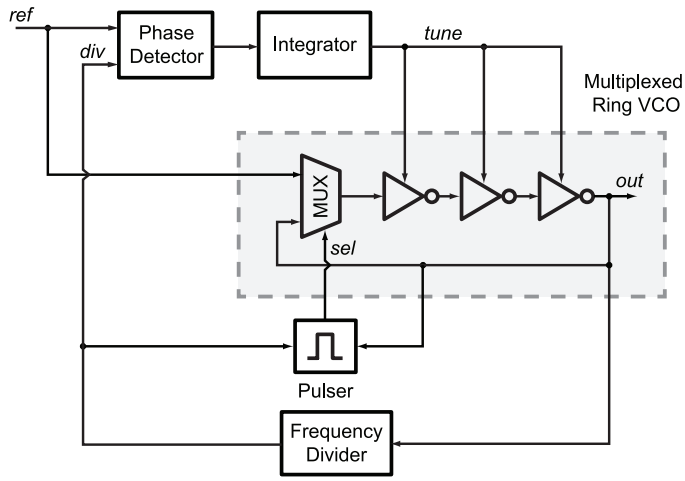

Fig. 1. Block diagram of a conventional multiplying DLL (MDLL).

Additionally, when more synthesizers on the same die must operate simultaneously in nearby bands (e.g., in carrier aggregation), the electromagnetic coupling among VCO coils causes unwanted spurious tones in the spectra. This impairment has been recently counteracted by means of both elaborated calibration techniques [6], and suitable shapes of inductor coils [7] that reduce coupling but compromise quality factor.

For all these reasons, ring oscillators would be more desirable than LC ones for radio transceiver design in scaled CMOS technologies. Thus, methods and schemes to aggressively filter or cancel out the phase noise of ring oscillators are being investigated. Remarkable steps in this direction are the feed-forward cancellation schemes introduced in [8] and [9]. Most likely, LC oscillators will continue to be needed in integrated transceivers for wireless cellular standards. However, ring oscillators combined along with those techniques will be potentially employed as local oscillators in systems requiring moderate spot noise levels but tight integrated noise (e.g., high-bit-rate WLANs, or clocking of high-resolution data converters).

An effective way to significantly reduce the phase noise of a ring oscillator without appreciably increasing its power consumption is to rely on the so-called recirculating or multiplying delay-locked loop (MDLL) [10]–[17]. This architecture schematically shown in Fig. 1 overcomes the typical limitations of PLLs in terms of noise-filtering bandwidth. In an MDLL, a multiplexed ring VCO let in the clean edges of the low-frequency reference signal (*ref*) and discards periodically the noisy edge of the oscillator. The reference edge is typically selected by means of a pulsed *sel* signal. While the phase noise

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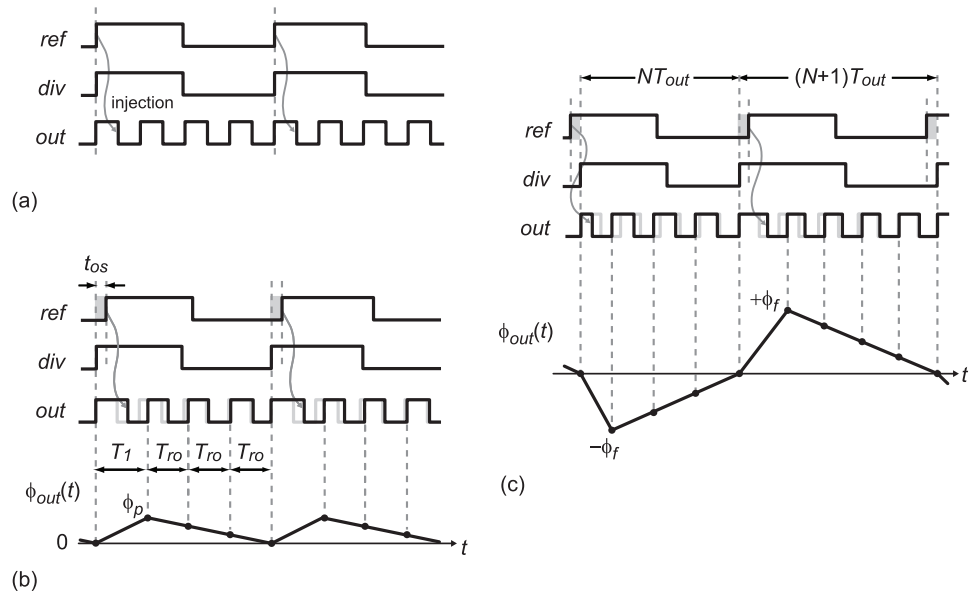


Fig. 2. Signal waveforms for the MDLL in Fig. 1: (a) ideal case, (b) case of PD time offset t_{os}, (c) case of dithering the divider modulus from N to $N+1$.

of a free-running oscillator integrates indefinitely [18], [19] and the phase noise of a VCO closed into a PLL is filtered out within its bandwidth (inevitably set well below the reference frequency [20]), the periodic refreshing of the signal edge in the MDLL substantially limits jitter accumulation. As rigorously demonstrated in [14], [21], [22] (using alternative approaches) and intuitively described in [23], the output phase noise of the MDLL is given by the (discrete-time) first difference of the phase noise of the free-running VCO, sampled at the reference rate f_{ref}. Thus, the output phase spectrum is given by filtering the spectrum of the free-running VCO via a first-order high-pass-shaped transfer function, with pole located at about $f_{ref}/2$ and high-frequency gain equal to 3 dB.

As a result, the phase noise of the free-running VCO in an MDLL is filtered out within a bandwidth much wider than in a typical PLL. This difference leads to the superior performance of MDLLs in terms of integrated jitter and dissipated power. Note that the same effect of wideband filtering of VCO phase noise is obtained by using the so-called injection locking PLL (IL-PLL), where a sub-harmonically injection-locked oscillator is enclosed in a PLL loop [24]–[31]. Unfortunately, MDLLs (as well as IL-PLLs) have two well-known limitations. First, the output frequency can only be changed by integer multiples of the reference frequency. The few attempts to extend MDLLs and IL-PLLs to fractional-N synthesis have achieved just coarse frequency resolution [32], [33], preventing their use in practical RF systems. The second problem is the large deterministic jitter, or equivalently the large reference spur, which is mainly caused by the phase offset of the phase detector. Known solutions to the latter issue typically require additional hardware, increasing power consumption and silicon area. They entail either the realization of an additional feedback loop detecting the time offset and retiming the injected pulse [13], [24], [26]–[28], or the adoption of techniques aiming to decouple the feedback of the PLL loop from the reference injection (such as the dual-pulse oscillator in [14], [34], or the dual loop in [29]).

This paper describes the first published fractional-N MDLL, achieving low jitter and power. Fractional-N operation is obtained by inserting an automatically calibrated digital-to-time converter on the reference path. Deterministic jitter is minimized by adopting an automatic cancellation of the time offset that eliminates the main source of reference spur with little extra hardware. The paper is organized as follows: In Section II, the operating principle and the key issues of the classical MDLL are briefly recalled. Section III illustrates the proposed fractional-N MDLL. Section IV describes the technique to automatically calibrate the time offset. The overall implementation and the key building blocks are described in Section V. Section VI presents the measured results and, finally, the conclusions are drawn in Section VII.

II. Multiplying DLL Background

The system in Fig. 1 without phase detector and integrator block is essentially a free-running ring oscillator periodically "realigned" by the signal *ref*. In fact, the pulser generates a pulse signal *sel* once every N rising edges of the *out* signal (being N an integer number), which allows the multiplexer to inject the *ref* edges into the ring VCO. Since, in general, the free-running frequency of the ring VCO, f_{fr}, differs from Nf_{ref}, the injection of *ref* causes a periodic phase error in the signal *out*, with period $T_{ref} = 1/f_{ref}$. The larger the offset of Nf_{ref} from f_{fr}, the larger is the phase error, and the more powerful is the spurious tone in the output spectrum at offset f_{ref} from the carrier. This issue is in principle solved by the tuning loop in Fig. 1 [10], [11]. A phase detector (PD) senses the phase error between the reference signal and the frequency-divided output, and drives an integrator that provides the VCO tuning voltage. Thus, at steady state, the loop tunes the VCO, so that the output frequency is N times the reference frequency ($f_{out} = Nf_{ref}$), and aligns the positive edges of *ref* and *out*, as shown in Fig. 2(a). We are assuming, for the sake of clarity, zero time delay in the frequency divider. On the other hand, the periodic injection of *ref* causes a

falling edge of *out* after $T_{out}/2$ (being $T_{out} = 1/f_{out}$ the output period), because of the odd number of inverting delay stages in the ring VCO. The resulting *out* in Fig. 2(a) is an ideal periodic waveform with no phase modulation, and, thus, no unwanted spurs in the spectrum. In contrast to a conventional PLL, the filter of the tuning loop is a simple integrator, and does not require a stabilizing zero [10], [17]. This comes from the fact that the periodic injection of the reference signal into the ring VCO eliminates the intrinsic integration from the tuning voltage to the output phase. In other words, if a step signal is applied at the *tune* node, the excess output phase of the VCO will not diverge, being periodically realigned by *ref*. Nevertheless, thanks to the integrator after the PD, the phase error between *ref* and *div* is always zero, even when Nf_{ref} differs from the free-running frequency f_{fr} of the VCO. In practice, like in a type-II PLL, there is no static phase error.

However, in contrast to a PLL, the time (or phase) offset at the input of the PD causes a spurious tone in the MDLL output spectrum at f_{ref} from the carrier, or, equivalently, a *deterministic* component of jitter [13], [14], [17]. The time offset t_{os} is induced by both systematic and statistical mismatches between the two inputs of the PD, as well as by delay mismatches between the two gates of the multiplexer in Fig. 1. The time offset causes a time shift equal to t_{os} between *ref* and *div*, at steady state [see Fig. 2(b)]. In this case, the output period T_{out} cannot be constant: the first period, T_1, is longer than the average period T_{ref}/N, while the following $(N-1)$ ones, T_{ro}, must be shorter to get the correct average. The tuning loop sets the period of the ring oscillator, T_{ro}, such that $T_1+(N-1)\cdot T_{ro} = T_{ref}$. The first rising edge of *out* will be aligned to *div*, while the subsequent falling edge of *out* will occur $T_{ro}/2$ seconds after the *ref* edge. Thus, $T_1 = T_{ro} + t_{os}$. Combining the two previous equations, we get $T_1 = T_{ref}/N + t_{os} \cdot (N-1)/N$. As a consequence, the output excess phase $\phi_{out}(t)$ [that can be seen as the phase error between *out* and the ideal *out* without offset, shown in gray in Fig. 2(b)] goes from zero to about $\phi_p \approx 2\pi \cdot N \cdot t_{os}/T_{ref}$ (for large N values) and, then, decreases linearly reaching again zero after T_{ref}. This sawtooth shape of $\phi_{out}(t)$ gives rise to a reference spur in the output spectrum.

Beside the offset problem, the use of the classical MDLL is bounded to integer-N clock multiplication only. To explain this fact, we can analyze the signal waveforms in Fig. 2(c), where the modulus of the frequency divider in Fig. 1 is varied from N to $(N+1)$ at every second reference cycle, and, for the sake of simplicity, the PD has zero phase offset. Thus, the average output period is $T_{ref}/(N+0.5) = T_{ref}/4.5$ (being $N = 4$). Similarly to a fractional-N PLL, the *div* signal is not aligned to the *ref* signal, but it exhibits a periodic phase error. However, in contrast to a fractional-N PLL, the periodic injection of the *ref* edge into the ring VCO causes the subsequent falling edge of *out* to occur after $T_{ro}/2$. As sketched in the diagram in Fig. 2(c), this time shift induces $+\phi_f$ and $-\phi_f$ phase errors in the *out* signal, whose values can be as large as $+\pi$ and $-\pi$. As a result, the output spectrum would be totally degraded by fractional spurs.

III. Fractional-N Multiplying DLL

Fig. 3 shows a simplified block schematic of the proposed fractional-N MDLL. The synthesizer has a mostly-digital architecture, where the phase error is detected and digitized by a time-to-digital converter (TDC), processed by a digital accumulator, and applied to the digital tuning input of a multiplexed ring-type digitally-controlled oscillator (DCO). With respect to the analog MDLL, this digital architecture offers lower area occupation and power consumption [17], as well as easy and accurate implementation of calibration schemes.

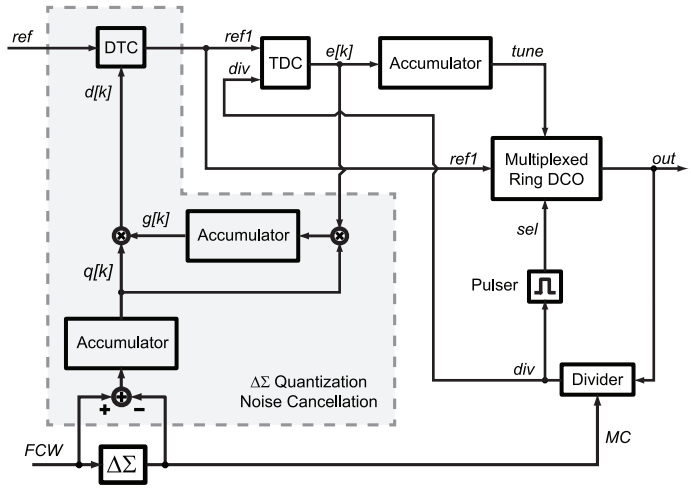


Fig. 3. Block diagram illustrating the operating principle of the proposed fractional-N MDLL.

Besides, a digital $\Delta\Sigma$ modulator dithers the modulus control of the frequency divider, to achieve on average fractional-N frequency division. As highlighted above, the periodic injection of the reference signal into the ring DCO produces an extremely large modulation of the output phase $\phi_{out}(t)$, giving rise to very high fractional-spur levels. Assuming a first-order $\Delta\Sigma$, the phase modulation is within $\pm\pi$ rad, and it would be even larger for higher order $\Delta\Sigma$'s. This problem that is inherent to fractional-N synthesis is caused by the induced phase delay between *ref* and *div*, whose value is proportional to the $\Delta\Sigma$ accumulated quantization noise $q[k]$.

To eliminate this unwanted modulation, we introduce a digital-to-time converter (DTC) in the reference path, which adds a delay to the *ref* signal, according to the input digital word $d[k]$, and generates a delayed version of the reference signal, *ref1*. The sequence $d[k]$ is obtained as the accumulated quantization noise $q[k]$ times a gain $g[k]$. In this way, if $g[k]$ has a proper value, the phase delay between *ref* and *div*, induced by $\Delta\Sigma$ dithering, is removed from the reference signal. In practice, *ref1* is realigned to *div*. The gain $g[k]$ is regulated by an accumulator driven by the product between the error detected by the TDC, $e[k]$, and $q[k]$. This feedback loop sets $g[k]$, such that $e[k]$ is uncorrelated with $q[k]$, or, in other words, such that the component of $e[k]$ induced by $\Delta\Sigma$ quantization is cancelled out.

The resulting signal waveforms are shown in Fig. 4. Since the new reference signal injected into the ring DCO, *ref1*, is perfectly aligned to *div*, no phase modulation of the *out* signal is produced, and no fractional spur is ideally generated in the output spectrum. As the $\Delta\Sigma$ quantization error is cancelled out via the DTC, it does not need to be converted by the TDC of the MDLL. Hence, a single-bit TDC can be employed to reduce

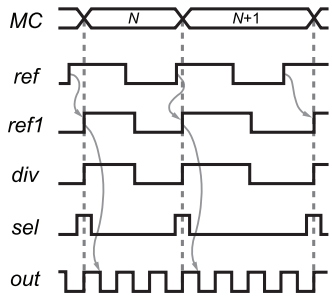


Fig. 4. Signal waveforms for the MDLL in Fig. 3.

power consumption and improve the jitter/power efficiency of the synthesizer [3].

In practice, the DTC has finite time resolution and, in general, nonlinear relationship between its control word and the time delay introduced. As a result, the cancellation of $\Delta\Sigma$ quantization error will be imperfect, giving rise to a residual modulation $\phi_{out}(t)$. An ideally linear M-bit DTC would scale down the output excess phase $\phi_{out}(t)$ shown in Fig. 2(c) by a factor of 2^{-M}, leading to a residual $\phi_{out}(t)$ within $\pm\phi_f/2^{-M}$ rad (i.e., $\pm\pi/2^{-M}$ for a first-order $\Delta\Sigma$ modulator). Nonlinearity in the DTC has the same impact of TDC nonlinearity in a digital PLL. In both cases, nonlinearity affects the reference signal path, and ultimately produces output spurs. Simulations and simple intuitive models, [35], suggest that the integral nonlinearity (INL) has to be lower than one LSB, to keep the spurs induced by nonlinearity below those induced by finite resolution.

IV. Time-Offset Cancellation Method

The second typical impairment of an MDLL is the time offset of the PD, and in general any time mismatch between the two reference paths. As we have already highlighted in Section II, this offset gives rise to significant reference-spur levels. To substantially mitigate this problem, two modifications to the original MDLL in Fig. 1 are made, and the resulting block diagram is shown in Fig. 5. First, an additional DTC is introduced which adds a delay between *ref1* and the input of the multiplexed ring DCO, *ref2*. Besides, a digital de-multiplexer is inserted at the output of the TDC, that allows diverting $e[k]$ either to the loop filter or to an accumulator controlling the second DTC input word. If $e[k]$ always feeds the loop filter, the second DTC just adds a fixed delay between *ref1* and *ref2*, that, with no loss of generality, we can assume to be zero. In this case, the input-referred TDC time offset t_{os} generates a static time error t_{os} between *ref1* and *div*, producing the output phase modulation $\phi_{out}(t)$ already sketched in Fig. 2(b). Unfortunately, the TDC that measures $\phi_{out}(t)$ at each reference edge produces a sequence $e[k]$ with all the samples equal to zero (if we neglect noise). So, to cancel this offset t_{os}, we need to first find a way to detect it.

To this purpose, we halve the rate of the *sel* signal, which gets close to $f_{ref}/2$. The resulting signal diagrams are shown in Fig. 6(a). Since the reference signal, *ref2*, is not injected into the ring DCO at every second cycle and the phase of *out* is not reset, the TDC is now able to detect the offset t_{os} at every second sample. So, we divert the TDC output $e[k]$ with odd

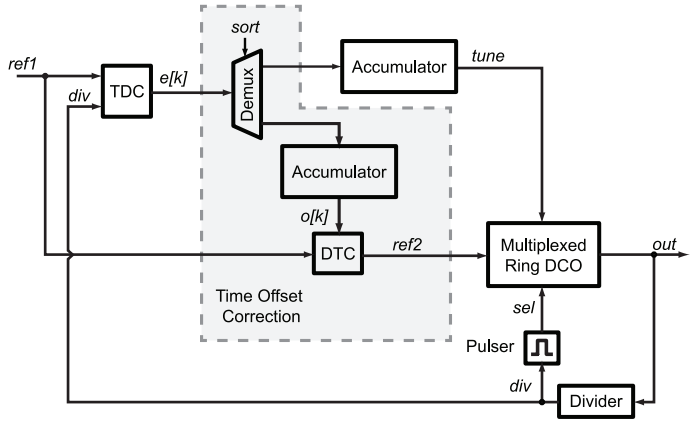


Fig. 5. Block diagram of the automatic correction of the time offset in the MDLL.

k to the tuning loop, and the sequence $e[k]$ with even k to an accumulator. The output, $o[k]$, of such accumulator is then used to control the delay of the second DTC. As a result, when $o[k]$ converges, the signal *ref2* is automatically delayed by a time that nulls $e[k]$ with even k, or, in other words, the offset-induced time error. In this way, the reference spur is removed [36]. The signals after the convergence of the offset-cancellation loop are shown in Fig. 6(b).

The offset-cancellation loop continuously runs in the background of the MDLL, so it is able to track any variation of the PD time offset. Note that, in this mode of operation (that can be denoted as *half-rate mode*), the reference edges are injected into the ring DCO at $f_{ref}/2$ rate, so the filtering bandwidth of DCO phase noise is halved. It is still possible to switch back to the full rate of injection of the reference edges. In this mode, which can be denoted as *full-rate mode*, the *sort* signal is kept constant and the steady-state value of $o[k]$ is frozen. The signal waveforms are shown in Fig. 6(c). In this mode, we recover the maximum filtering bandwidth of DCO phase noise, although we may need to periodically switch on the offset-cancellation loop, to track offset drifts.

In contrast to the offset-cancellation scheme in [13], which is based on a correlated double sampling technique, the proposed scheme does not require a precise multi-bit TDC that measures the time offset, but it can operate with a low-power single-bit TDC. In practice, the achieved offset cancellation is limited by DTC finite resolution. An M-bit DTC with resolution t_{LSB} leads to a residual amplitude of the phase error equal to $2\pi \cdot t_{LSB}/T_{out} = 2\pi \cdot 2^{-M}$ rad. Because of the single-bit TDC, the time needed to correct an offset t_{os} is in the order of t_{os}/t_{LSB} clock cycles, which typically does not represent a limitation.

V. Implementation

The overall synthesizer, embedding a single-bit (or bang-bang) TDC, is shown in Fig. 7. The MDLL is designed to synthesize an output frequency between 1.6 and 1.9 GHz, from a 50 MHz oscillator. To remove the phase-noise contribution of the multi-modulus frequency-divider, the output of the multiplexed ring oscillator is directly fed to the TDC input [17]. This choice saves power in the frequency divider, which is only used to derive the selection pulse *sel* for the ring DCO.

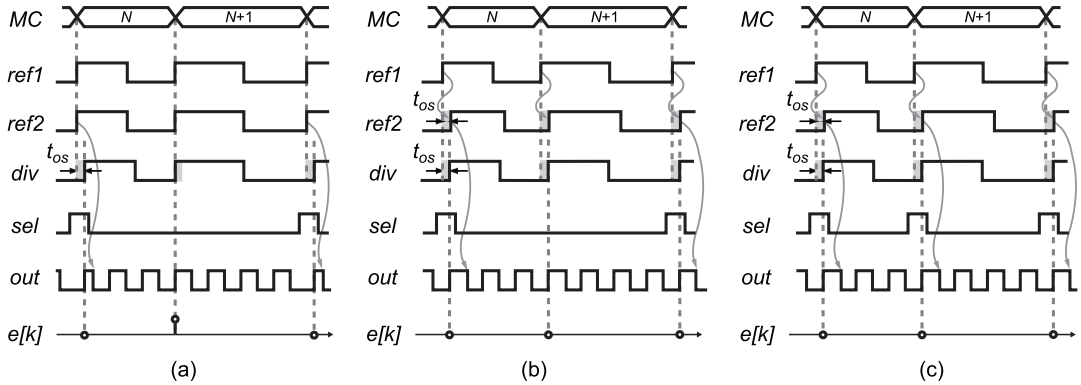


Fig. 6. Signal waveforms for the MDLL in Fig. 5: (a) *half-rate mode*, without offset cancellation, (b) *half-rate mode*, with offset cancellation, (c) *full-rate mode*, with offset cancellation.

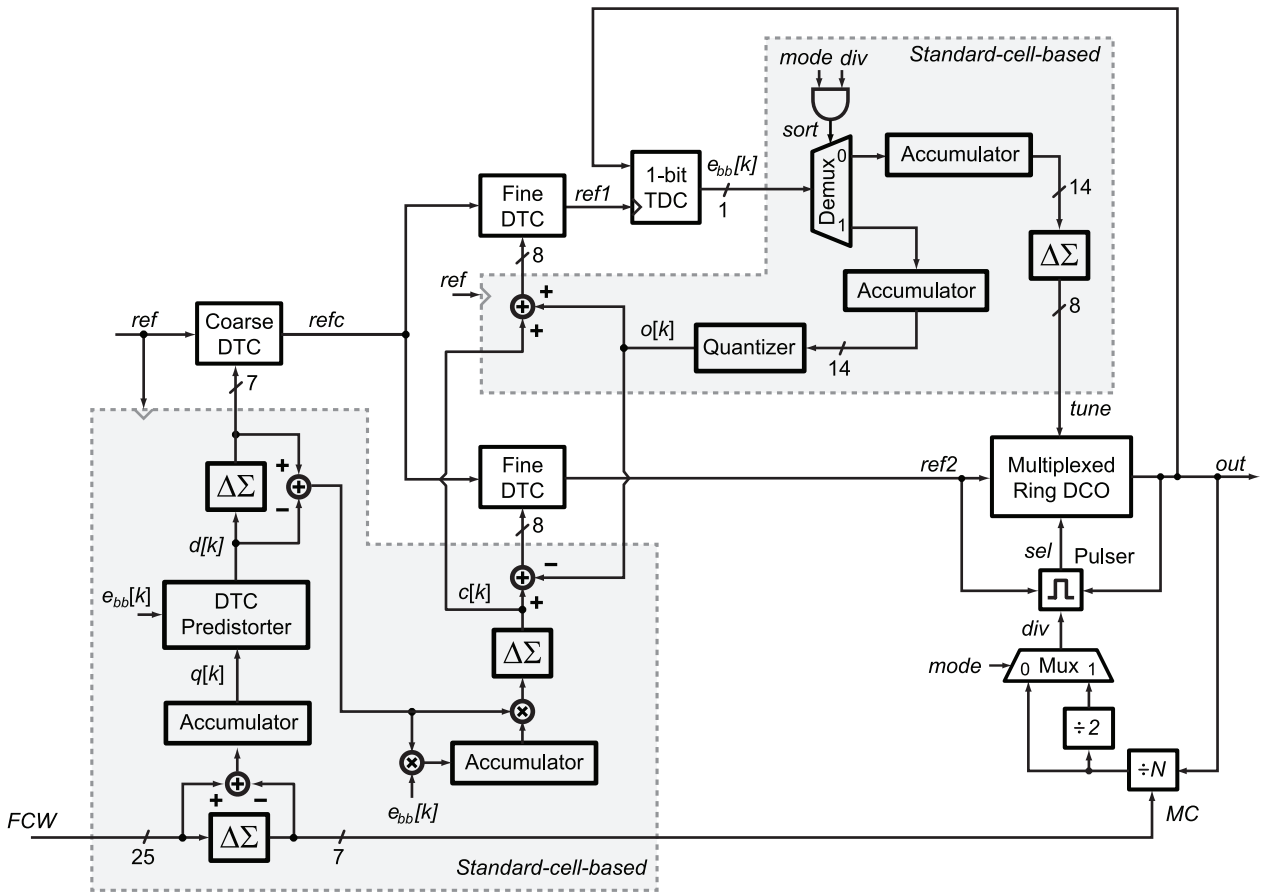


Fig. 7. Block diagram of the implemented fractional-N MDLL.

Both the automatic cancellation of the $\Delta\Sigma$ quantization error and the TDC offset, discussed in the previous sections, are implemented using digital standard cells and automatic synthesis tools. The first algorithm applies the same delay correction on the two paths via the coarse DTC (common to both paths) and the common mode signal $c[k]$ applied to the two fine DTC blocks. On the other hand, the TDC offset correction $o[k]$ is applied differentially at the input of the fine DTC of the two paths. This guarantees concurrent operation of the two calibration loops, similarly to what happens in a fully differential operational amplifier, where common mode and differential mode feedbacks operate concurrently. Note that any time mismatch between the two fine DTC blocks is not a concern, since it has the same impact as TDC time offset, and will be corrected by the offset cancellation loop as well.

The three control loops: (i) frequency tuning, (ii) offset cancellation, and (iii) quantization-error cancellation operate simultaneously and start up at the same time. Frequency tuning has a fast time constant (about 1.3 μs), while the two calibration loops have a time constant of about 30 μs, leading to an overall settling time from startup of about 150 μs. The MDLL can be switched from full-rate to half-rate mode by relying on the *mode* input. When *mode* is asserted, the MDLL is in half-rate mode: the *div* signal rate is halved, and *div* is used to control the demultiplexer

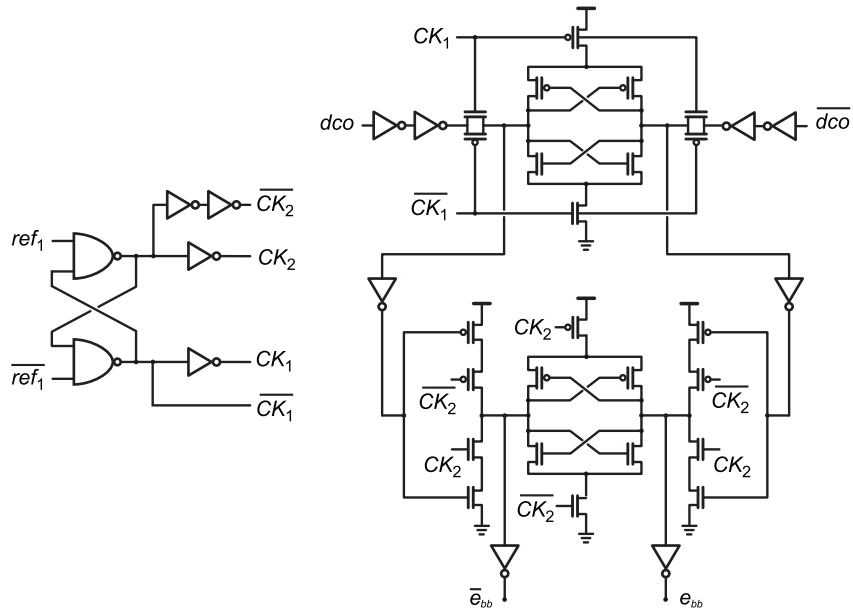


Fig. 8. Schematic of the single-bit time-to-digital converter [37].

following the TDC. Doing so, the demultiplexer diverts every second sample of $e_{bb}[k]$ to the accumulator of the offset-calibration loop. On the contrary, when the *mode* signal is zero, the MDLL is in full-rate mode: *div* has the reference rate and every sample of $e_{bb}[k]$ is delivered to the tuning loop.

A. Time/Digital Converter

As already mentioned, the TDC is implemented as a single-bit TDC, which saves considerable power and area with respect to a multi-bit converter. The circuit schematic shown in Fig. 8 consists of the cascade of two CMOS latches in master-slave configuration. A non-overlapping clock generator provides the clock phases to the two latches, to reduce kickback noise and limit flip-flop hysteresis [37]. The additional inverters between the latches increase isolation, so to further reduce hysteresis. The TDC drains about 62 μA from the 1.2-V supply, and it contributes to a flat phase noise of -117 dBc/Hz (referred to the MDLL output).

The asymmetry between the input paths of the TDC is the cause for a typical systematic time offset of about 9.6 ps, which is dominant over statistical mismatches. The time offset varies from 2.7 to 13.7 ps across the voltage supply range (1.1–1.3 V), and from 10.2 to 8.1 ps across the temperature range (0–125°C). Zero systematic offset (in typical conditions) can be achieved by employing a modified sense-amplifier flip-flop, as in [38]. However, in this case the power consumption would be much larger because of the static DC current. Moreover, the random offset and its variation over corners as well as the mismatches in the DCO multiplexer, would still force to employ an offset calibration circuit.

B. Multiplexed Ring DCO

The quantization introduced by the single-bit TDC, together with the DCO truncation error, may potentially generate limit cycles and, thus, spurs in the output spectrum [39]–[41]. To avoid them, the DCO resolution must be such that the power of the deterministic truncation noise is lower than the true-random phase noise. The circuit schematic of the multiplexed-ring DCO is illustrated in Fig. 9. Five delay cells are closed in a

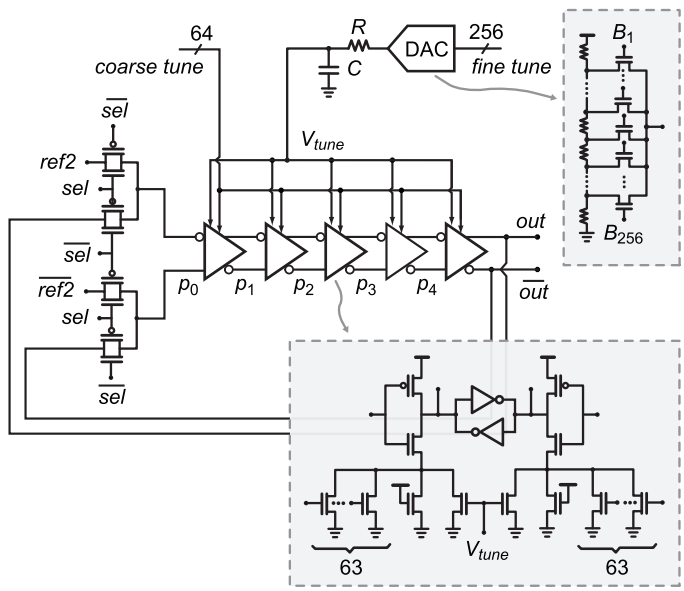


Fig. 9. Circuit schematic of the multiplexed ring DCO.

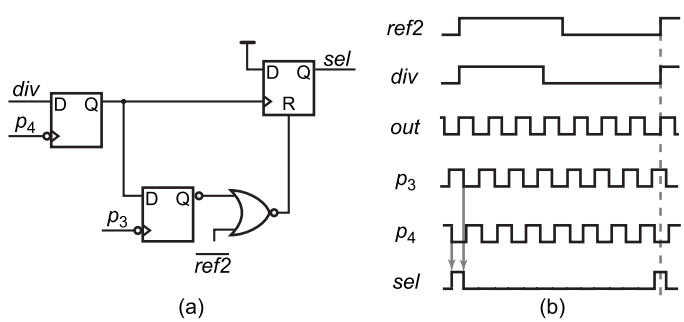


Fig. 10. Circuit schematic of the pulser and signal diagrams.

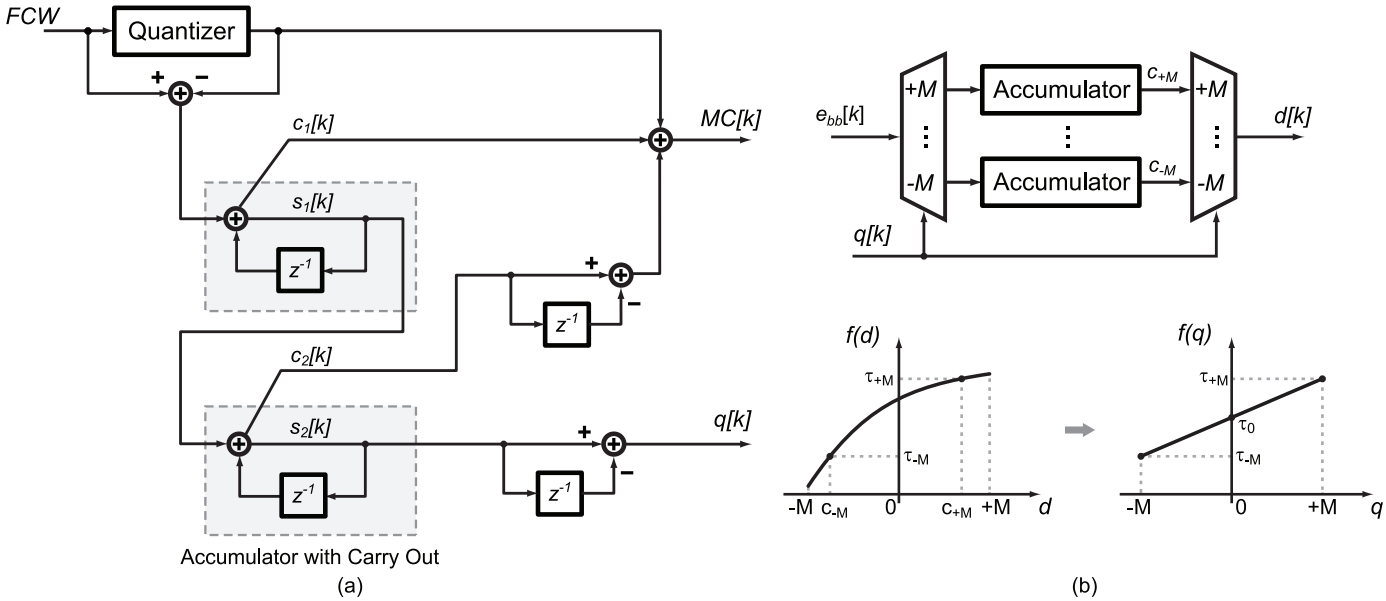


Fig. 11. Block diagram of circuits driving the frequency divider and the DTC converter: (a) Divider $\Delta\Sigma$ modulator, (b) Adaptive pre-distorter.

loop by means of a pass-transistor multiplexer. The delay cells employ a pseudo-differential topology [13], while frequency tuning is achieved by means of nMOS current starvers. A segmented tuning scheme is used to improve phase noise, increase maximum achievable frequency and reduce layout complexity. Coarse tune, which covers a frequency range between 1.3 and 2.4 GHz, is obtained by turning on and off 63 thermometer-coded nMOS transistors in each half of delay cell. A frequency-locked loop, not shown in figure, controls in the background the coarse tune, and helps speed up the locking transient of the MDLL. DCO fine tune is realized by means of an 8-bit DAC controlling the gate voltage V_{tune} of an nMOS transistor. The achieved resolution is about 500 kHz/bit. The DAC is implemented as a string of thermometer-coded poly-silicon resistors of about 90 Ω. To further refine frequency resolution, a first-order $\Delta\Sigma$ modulator, clocked by the *ref* signal, drives the DAC input, and a 1 MHz pole set by a first-order *RC* filter at the DAC output help suppress the $\Delta\Sigma$ quantization noise. The multiplexed ring DCO dissipates about 1.4 mA, and exhibits SSB phase noise of -123.5 dBc/Hz at 10 MHz offset from the carrier at 1.6 GHz.

Fig. 10 illustrates the pulser circuit along with the signal diagrams. The pulser generates a periodic pulse signal *sel* and drives the selection input of the DCO multiplexer, which replaces an edge of the signal travelling in the DCO with a reference edge, every N output periods. To work properly, the pulses of *sel* must be centered on the DCO signal edge to be replaced. Since the tuning of the delay stages acts just on the pull-down network, the time offset between positive and negative outputs of the delay cell varies over the synthesized channel frequencies. To avoid this dependence, the negative edges of two subsequent signals of the delay line, $p3$ and $p4$, both generated by the pull-down networks, are used as start/stop triggers for the rising/falling edges of *sel*. Two cascaded flip-flops sampling *div* guarantee the occurrence of the *sel* falling edge only after its rising edge. On the other hand, the NOR gate ensures that the falling transition of *sel* occurs only after the reference edge has been allowed to enter the delay line.

C. Digital/Time Converter

As described in the previous sections, the DTC needs to cancel both the time offset of the TDC and the quantization noise induced by the $\Delta\Sigma$ dithering the frequency-divider modulus. So, the DTC range must accommodate both components. The $\Delta\Sigma$ driving the divider is a MASH 1–1 modulator, whose schematic is shown in Fig. 11(a). Therefore, the induced quantization error at the output of the divider is as large as two output periods, $2T_{out}$ (i.e., 1.25 ns for the lowest output frequency, 1.6 GHz). The TDC offset and the statistical mismatches between the two inputs of the DCO multiplexer are lower than about 20 ps.

On the other hand, DTC resolution must be lower than about 500 fs (about 12 equivalent bits), and the INL lower than one LSB, to get residual level of reference and fractional spurs below -60 dBc. Moreover, being in a feedback loop, the DTC needs to have a monotonic characteristic. These linearity constraints over the wide dynamic range are combined with the requirement of sharp signal edges for low jitter. Thermometer coding guarantees monotonicity. However, the random mismatch of the unity delay t_{LSB} piles up along the DTC characteristic. So, the RMS value of the INL is $\sigma_{INL} = 2^{(M/2)-1} \cdot \sigma_{LSB}$, M being the number of bits and σ_{LSB} the RMS value of t_{LSB} [42]. Thus, σ_{LSB} should be kept below few percent of the LSB in a 12-bit DTC. This requirement would be tight, as the required LSB is in the order of hundreds of femtoseconds. A simple increase of the size of unity delay elements should be compensated by a proportional increase of current consumption, to maintain the same slope of the voltage waveforms.

To reduce power and area occupation, the DTC is instead split into a coarse and two fine blocks, and an adaptive pre-distortion of DTC input word, d, is adopted (Fig. 7). The adaptive pre-distortion relies on the technique described in [35] and shown

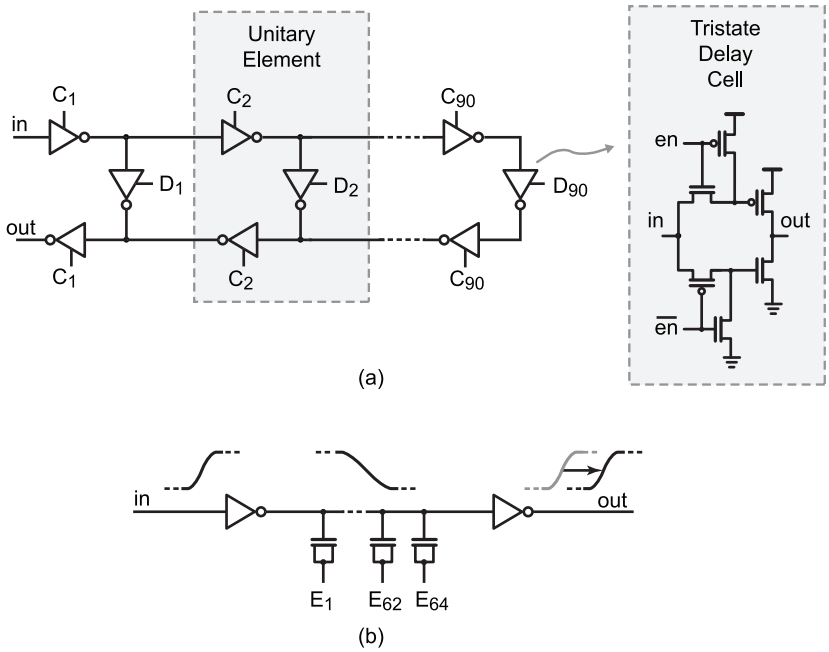


Fig. 12. Circuit schematic of the DTC converter: (a) coarse section, with tri-state delay element, and (b) fine section.

schematically in Fig. 11(b). Instead of simply multiplying $q[k]$ by one gain, $q[k]$ is mapped from the set of integer numbers $[-M, \ldots, M]$ into the set $C = [c_{-M}, \ldots, c_M]$. Thus, the nonlinear delay characteristic, $f(d)$, of the DTC is linearized from τ_{-M} to τ_{+M}, when the DTC is driven by the set of coefficients C. The resulting characteristic is the function $f(q)$ in Fig. 11(b). To automatically estimate the i-th coefficient c_i in the background, the error $e_{bb}[k]$, detected by the TDC when the signal $q[k] = i$, is integrated in the i-th accumulator. Meanwhile, the other $(2M - 1)$ accumulators integrate zero. In this fashion, every c_i will converge to a value that minimizes the error $e_{bb}[k]$ due to the nonlinearity of the DTC characteristic. To reduce hardware, the adaptive pre-distorter is implemented with 16 accumulators. In this way, the c_i will provide a piecewise linear approximation of the inverse function of the DTC characteristic.

Fig. 12 shows the transistor-level implementation of the DTCs. The coarse DTC is implemented as a digitally controllable delay line, which employs 93 unitary delay elements. Each delay element is made of tri-state inverters and allows to digitally shortening or lengthening the delay line. In simulations, the delay line covers a typical full-scale range from 320 to 2770 ps, with resolution of about 26 ps. This allows covering the required range of $2T_{out}$ with margin over process, temperature and voltage (PVT) variations. Current consumption and phase noise vary linearly across the delay range. In the middle of the range, DC current is 330 μA, flat phase noise is estimated to be equal to -123 dBc/Hz (referred to MDLL output), while the supply sensitivity, obtained from transistor-level simulations, is about 1.6 ns/V. The 8-bit fine DTC that is cascaded to the delay line is instead implemented as an inverter stage loaded by an array of thermometer-coded MOS varactors and a subsequent CMOS inverter stage restoring the sharpness of the voltage edges at the output. The full-scale range of the fine DTC covers with wide margin the LSB of the coarse one, while its resolution is equal to about 400 fs, in nominal conditions. The current consumption is 60 μA per each fine DTC, and their contribution to the output phase noise is -135 dBc/Hz.

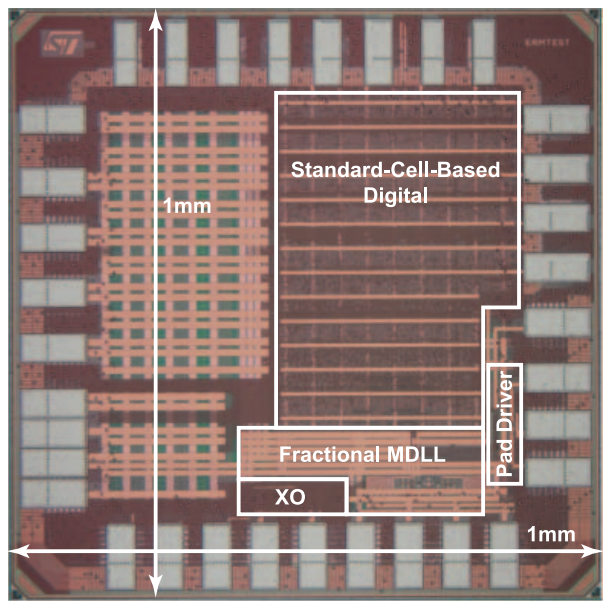
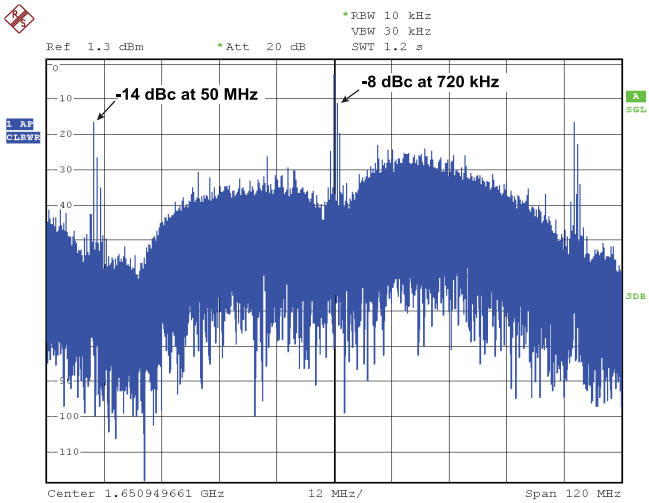


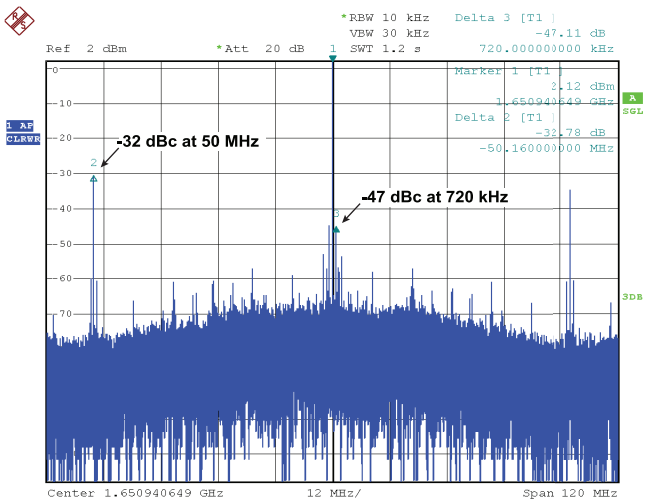
Fig. 13. Die photograph.

VI. Experimental Results

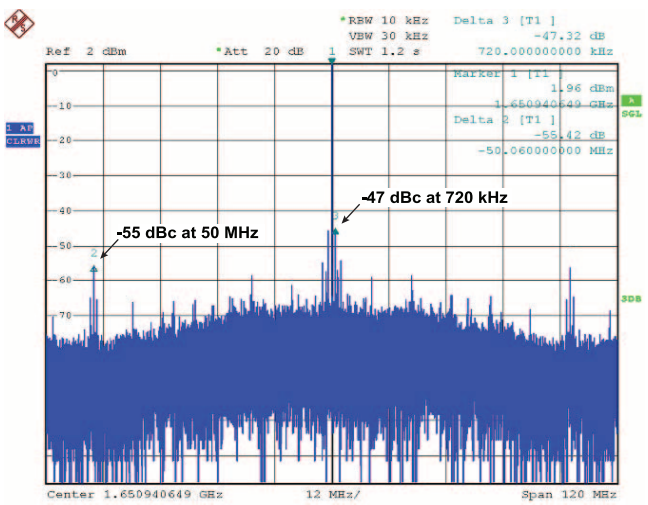
Fig. 13 shows the photograph of the chip, fabricated in a 65 nm CMOS process [43]. The size of the die is pad limited to 1 mm^2. For this reason, a decoupling capacitance of about 900-pF is included in the die (left side), and about 800 pF is spread over the standard-cell-based digital section (right side),



(a)



(b)



(c)

Fig. 14. Measured spectrum for a fractional-N channel: (a) disabling DTC correction, (b) enabling cancellation of $\Delta\Sigma$ noise and disabling offset correction, and (c) enabling both cancellation of $\Delta\Sigma$ noise and offset correction.

which is not optimized for density. When the circuit is embedded in a system on chip, a voltage regulator to avoid coupling

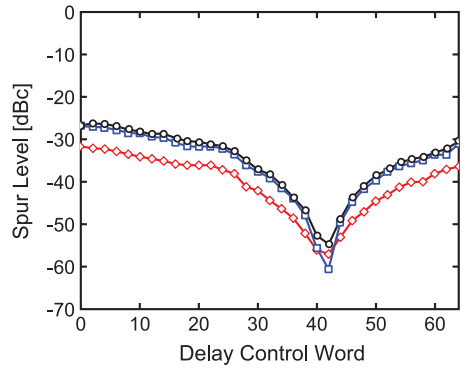


Fig. 15. Reference-spur level, measured hand-tuning the fine-DTC control word: 25 MHz (squares) and 50 MHz (diamonds) spur levels in *half-rate mode*; 50 MHz spur (circles) in *full-rate mode*.

among blocks can be used in place of most of the decoupling capacitance, with negligible area occupation [17]. The digital core area, excluding the capacitance, is only about 0.04 mm^2. The analog blocks occupy about 0.05 mm^2, whose main contributors are the DTC (25%) and the crystal reference oscillator (XO, 20%). Thus, the total core area of the synthesizer is 0.09 mm^2.

The synthesized frequency covers the 1.6–1.9 GHz range with a frequency resolution of about 190 Hz from the 50 MHz reference. The total power consumption (excluding pad drivers and XO) is 3.0 mW from a 1.2 V supply, when a fractional-N channel is synthesized. When the circuit synthesizes an integer-N channel, the coarse DTC is bypassed. So, its dissipation is reduced to a negligible value, and the overall power drops to about 2.4 mW.

The impact of both the cancellation of $\Delta\Sigma$ noise and TDC time offset via the DTC was experimentally assessed. Fig. 14(a) shows the output spectrum of the MDLL, when the $\Delta\Sigma$ dithers the divider modulus and the two algorithms are disabled. The large modulation visible in the spectrum is related to the mechanisms described in Fig. 2(c), which would prevent the use of a plain MDLL for fractional-N synthesis. The spectrum measured after enabling the cancellation of $\Delta\Sigma$ noise is shown in Fig. 14(b). The $\Delta\Sigma$ noise is substantially cancelled, but the reference spur level is still about -32 dBc, and a -47-dBc fractional spur at 720 kHz offset and its harmonics are visible in the spectrum. The fractional spurs, which are typically caused by the nonlinearity in the path from $\Delta\Sigma$ injection point to output, were not expected from simulations, and they may be ascribed to unwanted coupling between the harmonics of the input reference and the sensitive nodes of the ring DCO and of the DTC. As the offset cancellation is enabled in full-rate mode, the reference-spur level drops at -55 dBc, as shown in Fig. 14(c), while the level of fractional spurs is unaffected. This result further sustains the hypothesis of a parasitic coupling at the origin of the residual fractional spurs. Offset cancellation is verified also opening the calibration loop and manually sweeping the fine DTC input $o[k]$ in Fig. 5. The measured reference-spur level is reported in Fig. 15. In *half-rate mode*, the injection rate is halved to 25 MHz. So, the spur induced by the TDC offset lies at 25 MHz, and its level (squares in Fig. 15) goes from -27 to -61 dBc, sweeping the fine-DTC input word. In the same experimental conditions, the 50 MHz spur level (diamonds) is

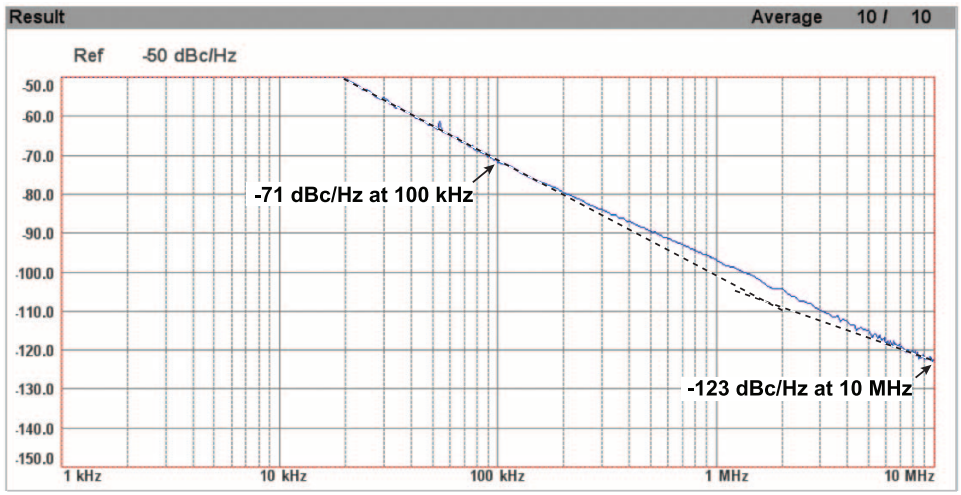


Fig. 16. Measured phase noise of the free-running multiplexed ring DCO.

TABLE I
PERFORMANCE COMPARISON WITH INDUCTOR-LESS FRACTIONAL-N FREQUENCY SYNTHESIZERS

	This Work ***Fractional-N mode***	[49] ISSCC'13	[52] VLSIC'14	[53] ISSCC'15	[54] ISSCC'15	[55] ISSCC'15
Architecture	**MDLL**	PLL	MDLL/PLL	PLL	PLL	IL-PLL
Reference Frequency (MHz)	**50**	26	50	50	26	380
Output Frequency (GHz)	**1.7**	1.9	4.5	2.0	2.0	1.5
Reference Spur (dBc)	**-55.4**	N/A	-60.1	N/A	-87	-63
Fractional Spur (dBc)	**-47**	-50.1	-50.1	-31.4	-70	N/A
Integrated RMS Jitter (ps)	**1.4**	3.4	1.5	3.5	2.4	N/A
Power Dissipation (mW)	**3.0**	10	11.6	3.9	9.1	3.0
Figure of Merit (dB)	**-232.3**	-219.4	-225.8	-223	-223	-224
Area occupation (mm^2)	**0.09**	0.055	0.48	0.029	0.228	0.048
CMOS Process (nm)	**65**	40	65	16	65	65

about 6 dB lower than the 25 MHz one (far from the minimum of the curve), which is consistent with level of the second harmonic of the sawtooth phase error described in Fig. 2(b). Instead, the minimum level of the 50 MHz spur saturates at about -56 dBc, revealing an unwanted coupling of the 50 MHz reference signal. In *full-rate mode*, the 50 MHz spur follows the level measured in half-rate mode and reaches a minimum of -55 dBc[1]. So, even in the full-rate mode, the minimum reference-spur level is not limited by the DTC resolution, but by unwanted coupling of the reference to the output signal. If the voltage supply is varied across the 1.1–1.3-V range, the minimum of the curves in Fig. 15 is shifted at different values of the DTC input word, but it shows the same behavior.

Fig. 16 displays the measured phase noise of the free-running multiplexed ring DCO. The $1/f^3$ phase noise extends up to about 1.2 MHz offset, the value at 100 kHz is about -71 dBc/Hz, while phase noise at 10 MHz offset is about -123 dBc/Hz. The MDLL phase noise plots measured for integer-N ($N = 32$) and fractional-N channel ($N = 33.014$) are shown in Fig. 17. Those measurements were compared against numerical simulations in Fig. 18. Perfect agreement is obtained for the integer-N case in Fig. 18(a). The phase noise of the free-running DCO, filtered up to about 25 MHz (i.e., $f_{ref}/2$), and that of the TDC at low frequency dominate MDLL noise. Instead, the phase noise of the reference path, mainly induced by the fine DTC (shown in the plot), is negligible. In the fractional-N case shown in Fig. 18(b), the reference noise introduced by the DTC is higher, as discussed above. However, even this component does not fully justify the measured spectrum. The peak measured at high offset frequency may be ascribed to an imperfect cancellation of the $\Delta\Sigma$ quantization noise. A residual $\Delta\Sigma$-quantization-noise component (shown in the same plot), 52-dB lower than the theoretical $\Delta\Sigma$ spectrum, may justify the measured spectrum.

The plot in Fig. 19 reports the RMS jitter integrated from 30 kHz to 30 MHz, as a function of the synthesized frequency. The jitter ranges between 0.47 and 0.55 ps for integer-N channels (main plot), and between 1.15 and 1.4 ps for fractional-N ones (inset). To compare this realization against other fractional-N, inductor-less, frequency synthesizers, we adopt the figure of merit (FoM) typically used for PLLs [1]. The FoM is

[1]The measured level of the reference spur is lower than the value reported in [43], and it was obtained improving the ground shielding of the die bonded on the test board.

TABLE II
PERFORMANCE COMPARISON WITH MDLLS OR INDUCTOR-LESS IL-PLLS

	This Work ***Integer-N mode***		[29] JSSC 14	[31] ISSCC 14	[17] JSSC 13	[15] ISSCC 11	[13] JSSC 08
Architecture	**MDLL**		IL-PLL	IL-PLL	MDLL	MDLL	MDLL
Reference Frequency (MHz)	**50**		300	1850	375	570	50
Output Frequency (GHz)	**1.6**	**1.9**	1.2	15	1.5	4.6	1.6
Division Factor	**32**	**38**	4	8	4	8	32
Reference Spur (dBc)	**-55.3**	**-55.1**	-57	N/A	-55.6	-46	-58.3
Integrated RMS Jitter (ps)	**0.47**	**0.53**	0.7	0.27	0.4	1	0.68
Power Dissipation (mW)	**2.4**	**2.6**	0.97	46.2	0.9	6.8	9.2*
Figure of Merit (dB)	**-242.7**	**-241.4**	-243.2	-234.7	-248.4	-231.7	-233.7
Area occupation (mm^2)	**0.09**		0.022	0.044	0.25	0.025	0.76*
CMOS Process (nm)	**65**		65	20	130	90	130

* including off-chip components (FPGA and DAC)

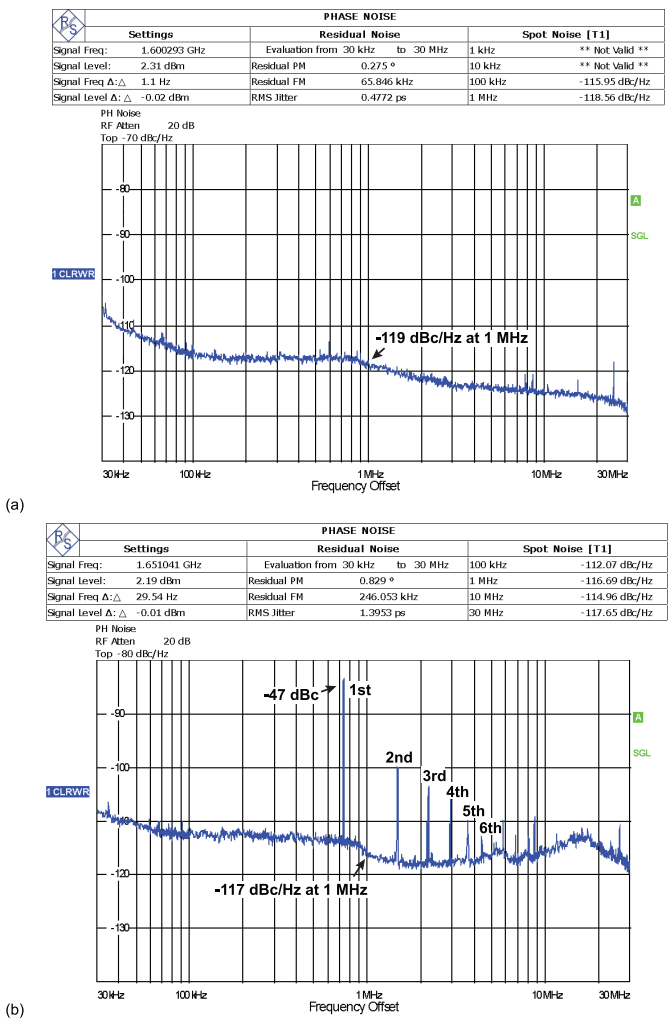


Fig. 17. Measured phase noise of the MDLL: (a) integer-N, (b) fractional-N channel.

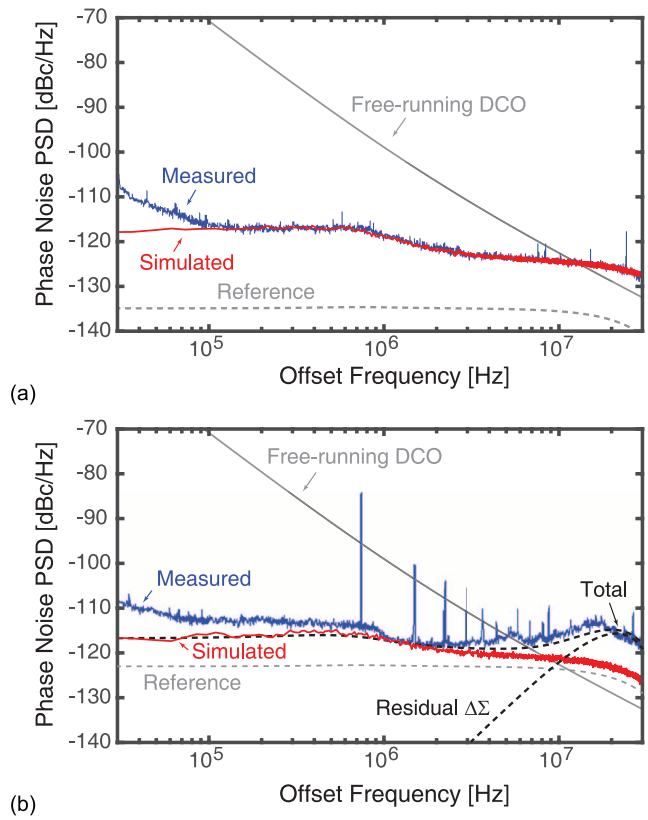


Fig. 18. Comparison of measured and simulated phase noise for (a) integer-N, and (b) fractional-N channel.

defined as $FoM = 10 \cdot \log_{10}\left(\sigma_t^2 \cdot P\right)$, being σ_t^2 the integrated jitter variance in squared seconds and P the dissipated power, expressed in milliwatts. The plot in in Fig. 20 reports σ_t^2 versus P, where the solid lines are obtained at constant FoM. The FoM achieved by the presented MDLL of about -232 dB (in the worst channel case) outperforms by several dBs the other published works. Table I summarizes and the main performance of the MDLL and compares it with the best published fractional-N inductor-less PLLs. Table II compares this work with other integer-N frequency synthesizers based on MDLLs or inductor-less IL-PLLs. The FoM of this work (ranging between -243 and -241 dB) outperforms previous works (excluding [17], [29] that benefit from a lower frequency-division factor)

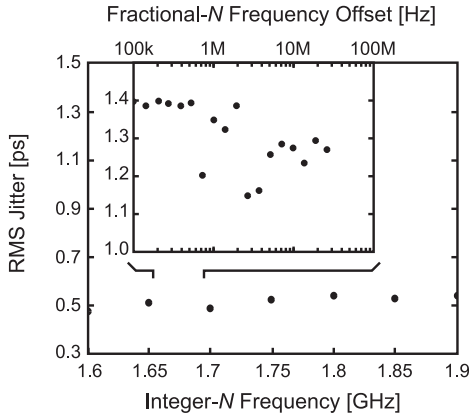


Fig. 19. Measured jitter over integer-N and fractional-N channels.

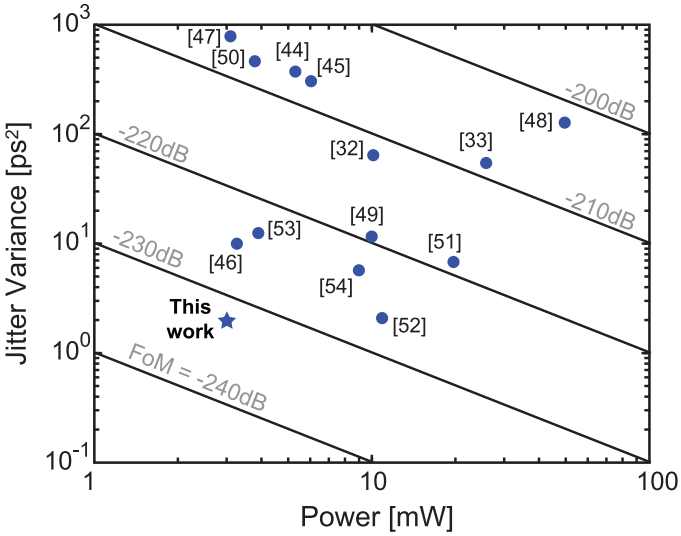


Fig. 20. Jitter-versus-power plot of inductor-less fractional-N frequency synthesizers.

at comparable level of reference spur, thanks to the low-power one-bit TDC and the offset cancellation scheme.

VII. Conclusion

This paper presented the design of the first $\Delta\Sigma$ fractional-N MDLL. Cancellation of $\Delta\Sigma$ noise and TDC time offset is obtained thanks to the insertion of a automatically-regulated DTC on the reference path. The prototype synthesizes frequencies between 1.6 and 1.9 GHz with 190 Hz resolution and achieves worst-case RMS integrated jitter of 1.4 ps at 3 mW power consumption and FoM of -232 dB. The measured RMS jitter with integer-N division is 0.47 ps at 2.4 mW power, which leads to a FoM of -243 dB. In both cases, the level of the reference spur is about -55 dBc. To the best of our knowledge, this circuit outperforms previously published, inductor-less fractional-N synthesizers in terms of both jitter and power dissipation.

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References

[1] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 117–121, 2009.

[2] X. Gao, E. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "A 2.2 GHz sub-sampling PLL with 0.16 psrms jitter and -125 dBc/Hz in-band phase noise at 700 μW loop-components power," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2010, pp. 139–140.

[3] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9-to-4.0 GHz fractional-N digital PLL with bang-bang phase detector and 560 $\mathrm{fs_{rms}}$ integrated jitter at 4.5 mW power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, Dec. 2011.

[4] S. Levantino, G. Marzin, C. Samori, and A. L. Lacaita, "A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, Oct. 2013.

[5] P.-C. Huang, W.-S. Chang, and T.-C. Lee, "A 2.3 GHz fractional-N dividerless phase-locked loop with -112 dBc/Hz In-band phase noise," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 362–363.

[6] A. Mirzaei and H. Darabi, "Pulling mitigation in wireless transmitters," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1958–1970, Dec. 2014.

[7] L. Fanori, T. Mattsson, and P. Andreani, "A 2.4-to-5.3 GHz dual-core CMOS VCO with concentric 8-shaped coils," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 370–371.

[8] S. Min, T. Copani, S. Kiaei, and B. Bakkaloglu, "A 90 nm CMOS 5-GHz ring-oscillator PLL with delay-discriminator-based active phase-noise cancellation," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1151–1160, May 2013.

[9] M. Mikhemar, D. Murphy, A. Mirzaei, and H. Darabi, "A cancellation technique for reciprocal-mixing caused by phase noise and spurs," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec. 2013.

[10] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[11] R. Farjad-Rad *et al.*, "A low-power multiplying DLL for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1804–1812, Dec. 2002.

[12] S. Ye and I. Galton, "Techniques for phase noise suppression in recirculating DLLs," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1222–1230, Aug. 2004.

[13] B. M. Helal, M. Z. Straayer, G.-Y. Wei, and M. H. Perrott, "A highly digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve subpicosecond jitter performance," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 855–863, Apr. 2008.

[14] S. Gierkink, "Low-spur, low-phase-noise clock multiplier based on a combination of PLL and recirculating DLL with dual-pulse ring oscillator and self-correcting charge pump," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2967–2976, Dec. 2008.

[15] T. Ali, A. Hafez, R. Drost, R. Ho, and C.-K. Yang, "A 4.6 GHz MDLL with -46 dBc reference spur and aperture position tuning," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 466–467.

[16] D.-W. Jee, D. Sylvester, D. Blaauw, and J.-Y. Sim, "A 0.45 V 423 nW 3.2 MHz multiplying DLL with leakage-based oscillator for ultra-low-power sensor platforms," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 188–189.

[17] A. Elshazly, R. Inti, B. Young, and P. Hanumolu, "Clock multiplication techniques using digital multiplying delay-locked loops," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1416–1428, Jun. 2013.

[18] J. A. McNeill, "Jitter in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 871–872, Jun. 1997.

[19] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[20] F. M. Gardner, "Charge-pump phase-lock loop," *IEEE Trans. Commun.*, vol. COM-28, no. 11, pp. 1849–1858, Nov. 1980.

[21] P. Maffezzoni and S. Levantino, "Phase noise of pulse injection-locked oscillators," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 10, pp. 2912–2919, Oct. 2014.

[22] N. Da Dalt, "Jitter an analysis of phase noise in religned VCOs," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 61, no. 3, pp. 143–146, Mar. 2014.

[23] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–79, Jan. 2015.

[24] B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, "A low jitter programmable clock multiplier based on a pulse injection-locked oscillator with a highly-digital tuning loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[25] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[26] C.-F. Liang and K.-J. Hsiao, "An injection-locked ring PLL with self-aligned injection window," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 90–91.

[27] Y.-C. Huang and S.-I. Liu, "A 2.4-GHz subharmonically injection-locked PLL with self-calibrated injection timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, 2013.

[28] I.-T. Lee, Y.-J. Chen, S.-I. Liu, C.-P. Jou, F.-L. Hsueh, and H.-H. Hsieh, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 414–415.

[29] A. Musa, W. Deng, T. Siriburanon, M. Miyahara, K. Okada, and A. Matsuzawa, "A compact, low-power and low-jitter dual-loop injection locked PLL using all-digital PVT calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[30] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, "A 0.0066 mm^2 780 μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using edge-injection technique," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 266–267.

[31] J.-C. Chien, P. Upadhyaya, H. Jung, S. Chen, W. Fang, A. M. Niknejad, J. Savoj, and K. Chang, "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16 GHz injection-locked ring oscillator in 20 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 52–53.

[32] P. Park, J. Park, H. Park, and S. Cho, "An all-digital clock generator using a fractionally injection-locked oscillator in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 336–337.

[33] S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara, and K. Masu, "An inductor-less injection-locked PLL with 1/2- and 1/4-integral sub-harmonic locking in 90 nm CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, Jun. 2012, pp. 189–192.

[34] D. Park and S. Cho, "A 14.2 mW 2.55-to-3 GHz cascaded PLL with reference injection and 800 MHz Delta-Sigma modulator in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2989–2998, Dec. 2012.

[35] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, Aug. 2014.

[36] G. Marzin, A. Fenaroli, G. Marucci, S. Levantino, C. Samori, and A. L. Lacaita, "Spur cancellation technique for MDLL-based frequency synthesizers," in *Proc. Int. Symp. Circuits and Systems (ISCAS)*, 2013, pp. 165–168.

[37] N. Da Dalt, "Theory and implementation of digital bang-bang frequency synthesizers for high speed serial data communications," Ph.D. dissertatiojn , Rheinisch-Westfâlischen Technischen Hochschule Aachen, Aachen, Germany, 2007.

[38] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita, "Time-to-digital converter for frequency synthesis based on a digital bang-bang," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 57, no. 3, pp. 548–555, Mar. 2010.

[39] N. Da Dalt, "Linearized analysis of a digital bang-bang PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3663–3675, Nov. 2008.

[40] M. Zanuso, D. Tasca, S. Levantino, A. Donadel, C. Samori, and A. L. Lacaita, "Noise analysis and minimization in bang-bang digital PLL," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 56, no. 11, pp. 835–839, Nov. 2009.

[41] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Analysis and design of low-jitter digital bang-bang phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 26–36, Jan. 2014.

[42] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, Dec. 1998.

[43] G. Marucci, A. Fenaroli, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 1.7 GHz MDLL-based fractional-N frequency synthesizer with 1.4 ps RMS integrated jitter and 3 mW power using a 1 b TDC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 360–361.

[44] T.-K. Jang, X. Nan, F. Liu, J. Shin, H. Ryu, J. Kim, T. Kim, J. Park, and H. Park, "A 0.026 mm^2 5.3 mW 32-to-2000 MHz digital fractional-N phase locked-loop using a phase-interpolating phase-to-digital converter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 254–255.

[45] X. Yu, Y. Sun, W. Rhee, and Z. Wang, "An FIR-embedded noise filtering method for fractional-N PLL clock generators," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2426–2436, Sep. 2009.

[46] A. Elkholy, A. Elshazly, S. Saxena, G. Shu, and P. K. Hanumolu, "A 20-to-1000 MHz $\pm$14 ps peak-to-peak jitter reconfigurable multi-output all-digital clock generator using open-loop fractional dividers in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 272–273.

[47] J. Liu, T.-K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, and H. Park, "A 0.012 mm^2 3.1 mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2014, pp. 268–269.

[48] Z. Shu, K. L. Lee, and B. H. Leung, "A 2.4-GHz ring-oscillator-based CMOS frequency synthesizer with a fractional divider dual-PLL architecture," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 452–462, Mar. 2004.

[49] T.-K. Kao, C.-F. Liang, H.-H. Chiu, and M. Ashburn, "A wideband fractional-N ring PLL with fractional-spur suppression using spectrally shaped segmentation," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 416–417.

[50] M. S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800 MHz fractional-N digital PLL with embedded TDC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 472–473.

[51] D.-W. Jee, Y. Suh, H.-J. Park, and J.-Y. Sim, "A 0.1-f_{ref} BW 1 GHz fractional-N PLL with FIR embedded phase-interpolator-based noise filtering," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 94–95.

[52] R. K. Nandwana, T. Anand, S. Saxena, S.-J. Kim, M. Talegaonkar, A. Elkholy, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 4.25 GHz–4.75 GHz calibration-free fractional-N ring PLL using hybrid phase/current-mode phase interpolator with 13.2 dB phase-noise improvement," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014.

[53] T.-H. Tsai, M.-S. Yuan, C.-H. Chang, C.-C. Liao, C.-C. Li, and R. B. Staszewski, "A 1.22 ps integrated-jitter 0.25-to-4 GHz fractional-N ADPLL in 16 nm FinFet CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 260–261.

[54] C.-F. Liang and P.-Y. Wang, "A wideband fractional-N ring PLL using a near-ground pre-distorted switched-capacitor loop filter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 190–191.

[55] W. Deng, Y. Dongsheng, A. T. Narayanan, K. Nakata, T. Siriburanon, K. Okada, and A. Matsuzawa, "A 0.048 mm^2 3 mW synthesizable fractional-N PLL with a soft injection-locking technique," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2015, pp. 252–253.