100 000 Frames/s 64 × 32 Single-Photon Detector Array for 2-D Imaging and 3-D Ranging

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I. Introduction

SINGLE-Photon Avalanche Diodes (SPADs) gradually emerged in the early 1990s as a solid-state solution to replace photomultiplier tubes and micro-channel plates in photon counting applications [1]. From the mid-1990s onwards, the use of dedicated CMOS-compatible processes fostered significant advances in building multichannel photon-counting modules, thus making SPAD devices a robust and competitive technology in many single-photon applications like confocal microscopy [2], biological essays [3], single-molecule spectroscopy [4], quantum cryptography [5], quantum key distribution [6], diffuse optical tomography [7], LIDAR [8] and adaptive optics in astrophysics [9].

The increasing demand of high-throughput single-photon detector arrays drove the research towards the development of SPAD imagers in conventional CMOS processes. To this aim, a major breakthrough was achieved in early 2000s, when SPAD structures were successfully demonstrated in standard high-voltage CMOS technologies [10]–[12]. Although there is still room for improvements regarding fill-factor, quantum efficiency and optical stack optimization, CMOS SPAD arrays represent, nowadays, a viable solution in high frame-rate single-photon imaging applications, where even the sensitivity of bulky intensified or expensive electron-multiplying charge-coupled devices is limited by read-out noise [13]. Typical examples are Förster Resonance Energy Transfer [14], Fluorescence Lifetime Imaging Microscopy (FLIM) [15]–[19], Fluorescence Correlation Spectroscopy (FCS) [20], [21] and Raman Spectroscopy [22], [23], as well as Positron Emission Tomography [24], and optical communication [25]–[27].

A major application which drives the development of SPAD arrays (not only in Silicon but also in III-V compounds) is optical 3D ranging, where picosecond timing resolution and single-photon sensitivity are required to achieve millimeter accuracy together with high-frame rate capability. SPAD-based multi-pixel rangefinders can extract distance information from either direct photons' time-of-flight (dTOF) measurements, through on-chip Time-to-Digital Converters (TDCs) [28]–[33] or Time-to-Amplitude Converters [34], or indirect time-of-flight (iTOF) measurement, where distance information is extracted from the phase-delay between a pulsed [35] or continuous-wave (CW) [36]–[39] modulated light source and its back-reflected echo (like in heterodyne or homodyne demodulation). Compared to CMOS/CCD [40] and CMOS [41] rangefinders, SPAD arrays have inherent better time resolution (limited by SPAD timing jitter, typically better than 100 ps), higher accuracy (just limited by photon shot-noise) and better linearity (since analog amplification and ADC quantization non-idealities are avoided) at the expense of fill-factor and pixel resolution [36]. In the literature reported so far, CMOS SPAD arrays were designed to target specific applications, by optimizing the trade-off among many parameters like SPAD area and geometry, number of pixels, complexity of in-pixel, on-chip and off-chip read-out electronics, etc., but limiting, conjointly, the exploitation in other fields.

In order to broaden the application fields of single-photon CMOS SPAD imagers, we conceived a multipurpose image sensor based on a cost-effective 0.35 μm CMOS 64×32 SPAD array, able to process at pixel-level both 2D (such as light

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intensity, reflectivity, luminescence or fluorescence) and 3D (such as distance, shape, velocity) information at a frame rate up to 100,000 fps. Although pixel density is limited due to the amount of in-pixel circuitry, fill-factor is comparable to other reported approaches; moreover, the flexible architecture and the featured best-in-class CMOS SPAD detectors employed enable high performance, in terms of high frame-rate and single-photon sensitivity, in most applications. The paper is organized as follows: Section II outlines the novel architecture; Section III presents and discusses preliminary results from 2D and 3D acquisitions; finally, Section IV concludes the paper.

II. Chip Design

SPAD array architectures usually integrate either counters or time converters. The former components are suited for time-gated single-photon counting (TGSPC) and iTOF; instead the latter ones allow to implement time-correlated single-photon counting (TCSPC) and direct time-of-flight (dTOF).

TCSPC typically outperforms TGSPC when complex waveforms are to be acquired, achieving higher accuracy in lifetime measurement [42], [43], whilst dTOF generally reaches better distance precision than iTOF, in light-starved condition [44]. Nonetheless, time converters produce a large amount of raw data (more than 1 byte per photon), which require high data throughput and complex off-chip computation. Therefore, TDC/TAC-based imager have an overall system frame-rate limited to less than few hundreds fps [18] and are suited only for very low photon rates.

TGSPC and iTOF architectures usually have one or more in-pixel counters, which allow to record the intensity of either slowly varying optical signals (in the microsecond range or slower) or high-repetition rate pulsed signals in fixed time windows to suppress unwanted background pulses (thus increasing dynamic range) or to discriminate between fast and slow events (e.g. between Raman scattering and fluorescence, or between fluorescence and phosphorescence) [42]. TGSPC can be also used to reconstruct the waveform of very fast optical signals (in the nanosecond range) by using a sliding-time window scheme: many measurement cycles are performed and the waveform of the input signal is sampled by "sliding" the delay of the integration window [42]. Although this approach has a very poor photon collection efficiency for full waveform scanning, since most of the time the detector is gated off, it becomes advantageous when the waveform is known *a priori* (e.g. single/double exponential decays or CW-modulated light). Indeed, in this situation, the optical signal can be undersampled, with an almost unitary collection efficiency, in few time windows (typically two or four), thus dramatically reducing the output data stream. Then, waveform parameters (such as decay constants, phase shift, or signal intensity) can be easily determined with very low computational overhead.

Consequently, counter-based arrays reach higher frame-rates, tolerate higher count rates, and offer better flexibility. For this reason, we conceived and developed an array architecture based on counter-based pixels.

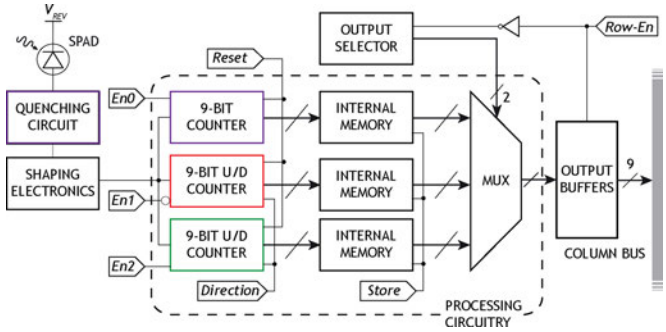

Fig. 1. Simplified pixel's block diagram. Note that *En1* is an active-low input.

A. Pixel Circuitry

The smart pixel (Fig. 1) is fabricated in a high-voltage 0.35 μm 2P-4M (two polysilicon and four metal interconnect levels) CMOS technology on 8" wafers [47]–[49]. The pixel comprises a round SPAD, with 30 μm active-area diameter, and includes an analog quenching circuit front-end to properly bias the SPAD above its breakdown voltage and to promptly sense its ignition [50]. Low area occupation (only 18 transistors), minimized stray capacitances, and fast mixed passive-active quenching [51] through positive feedback on the quenching transistor, considerably minimize the avalanche charge flowing through the detector [52], hence the deleterious afterpulsing issues [1], while boosting the maximum count rate up to 50 Mcps, with a hold-off time (T_{HO}) as short as 20 ns. The quenching circuit provides a digital pulse to the following electronics through a shaping circuitry, which adjusts the pulse width and manages the synchronization with external signals to avoid race hazards.

Three synchronous Fibonacci LFSR (Linear Feedback Shift Register) counters (two of which are bidirectional) are employed to grant high-speed operations and low area occupation. A 9-bit counting depth prevents overflow in typical working conditions, i.e. with hold-off time varying from 20 ns to 60 ns, and frame readout lasting 10 μs to 30 μs.

Three in-pixel memory registers store the content of the respective counter, simultaneously for the whole array, thus allowing *global shutter* operation and avoiding the well-known issues related to rolling shutter readout [37]. Each time the *Row-En* strobe is set, a 3:1 multiplexer connects the memory to be read out to the output buffers, which drive the capacitive load of the column bus.

The devised pixel has a pitch of 150 μm and a fill-factor of 3.14% (Fig. 2). For imaging applications, microlenses can get an expected 10x fill-factor improvement [53], even if this value greatly depends on the employed optical setup. Conversely, other applications exploiting each single pixel of the array as an independent single-photon counter (e. g. FCS) benefit from the low fill-factor [54].

B. Operating Modalities

The proposed pixel architecture has been devised to fulfil electronics requirements for high-frame-rate imaging, TGSPC and iTOF. In high-frame rate imaging only one counter is required

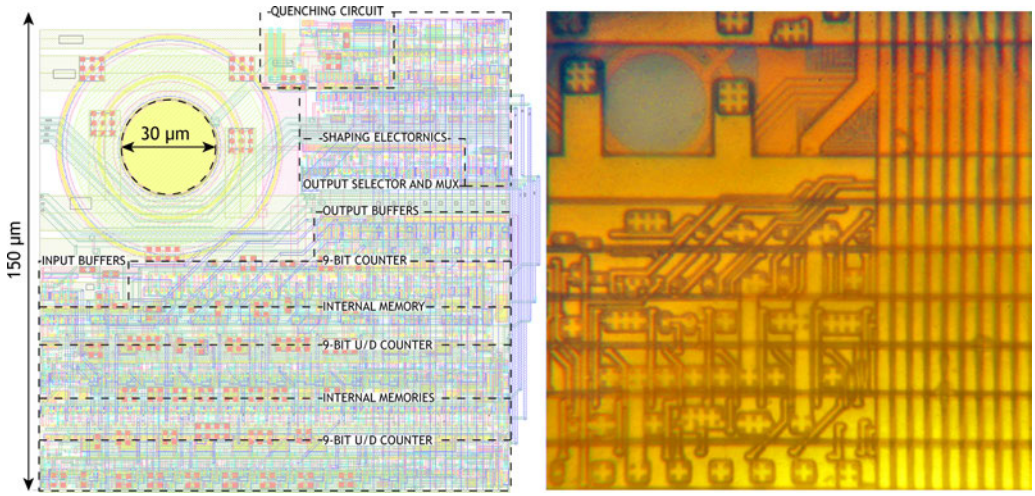

Fig. 2. Layout and main building blocks (left) and micrograph (right) of the pixel. The pitch (side) is 150 μm and the SPAD active area diameter is 30 μm.

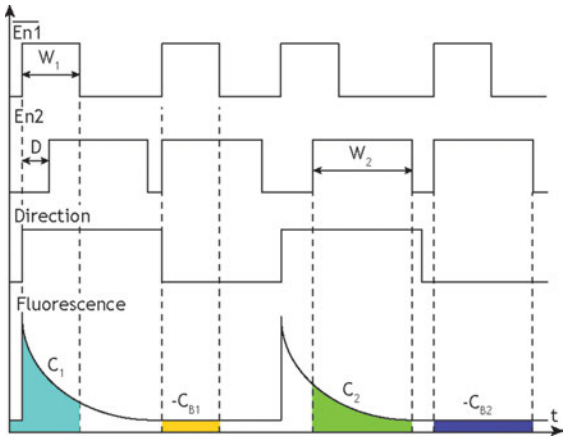

Fig. 3. Generalized 2-gate RLD timing diagram. *En1* and *En2* enable the two U/D counters (see Fig. 1). Counting direction is up when *Direction* is high, and viceversa. C_{B1} and C_{B2} are the background counts subtracted from C_1 and C_2, respectively.

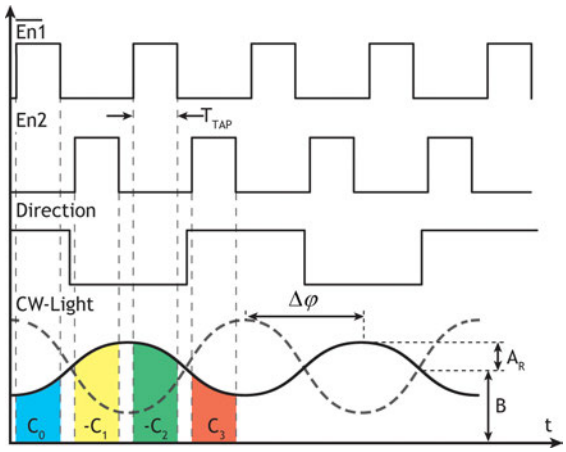

Fig. 4. Timing of the control signals (bottom) for implementing CW-iTOF 3D ranging. The dotted line represents the input light source, the received signal is depicted by a solid line. *En0* (not shown) is always high.

and the array can be employed in FCS [20], [21] or gun muzzle flash detection [55]. In time-gated FLIM, a widely used technique is rapid lifetime determination (RLD), where two or four time windows are used to evaluate respectively single or double exponential decays [56]. Better performance are achieved through generalized 2-gate RLD [57], easily implementable in the conceived pixel with the two up-down counters: if C_1 and C_2 are the counts accumulated in two windows with respective widths W_1 and W_2 and delayed from each other by a time *D*, the lifetime τ can be computed as [57]:

$$\frac{C_2}{C_1} = \frac{\exp[-(W_2 + D)/\tau] - \exp(-D/\tau)}{\exp(-W_1/\tau) - 1} \tag{1}$$

When the fluorescence decay is not triggered, background counts (C_B) can be subtracted directly in-pixel using the up-down counting scheme shown in Fig. 3. 4-, 8- or multi-gate RLD can also be performed, but with a lower collection efficiency and slower frame rate. Moreover, the third counter allows the co-registration of FCS-scale data (with microsecond resolution) and lifetime measurements (with nanosecond resolution). The different time scale information can be integrated to enhance the quality of FCS data by removing noise and distortion caused by scattered excitation light, detector noise, and afterpulsing [58].

Concerning iTOF measurements, two techniques are usually employed: pulsed light [45] and CW iTOF [40]. Although both methods can be implemented in the proposed architecture, we focus on CW-iTOF, being a more robust technique. Here, a sinusoidal-modulated light shines the scene; the received reflected signal is phase-shifted by an amount $\Delta\varphi$ proportional to the object's distance *d*:

$$d = \frac{cT_P}{2}\frac{\Delta\varphi}{2\pi} = d_{\mathrm{MAX}}\frac{\Delta\varphi}{2\pi} \tag{2}$$

To retrieve phase-shift information, the reflected wave is sampled by four integration windows of same duration (T_{TAP}), providing the counts C_0, C_1, C_2 and C_3 (Fig. 4). Then, through Discrete Fourier Transform, phase delay $\Delta\varphi$, reflected active-light

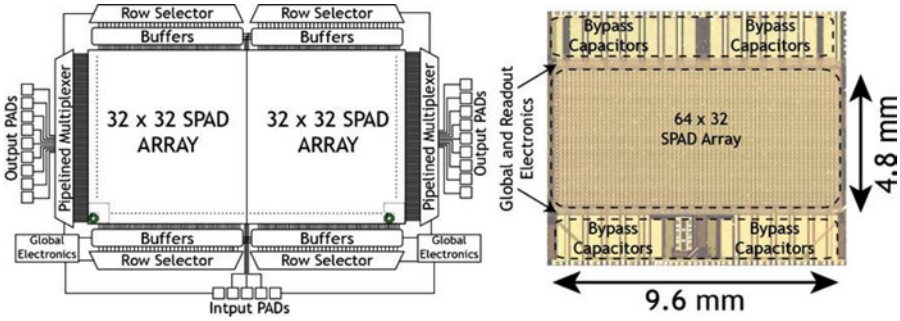

Fig. 5. Block diagram of the 64×32 SPAD imager with peripheral electronics (left) and micrograph (right) with relative dimensions. Global and Readout electronics are placed between the capacitors and the SPAD array.

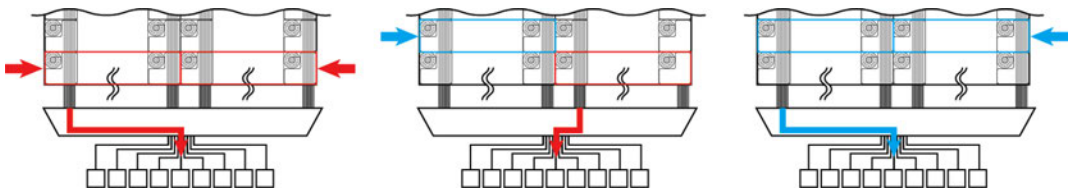

Fig. 6. Operations performed during the readout: row selectors are initialized to enable the first rows of both sub-arrays (left); after half of the pixels in the rows is scanned, the following left rows are connected to the data bus (center); when the first rows' readout is completed, the half rows on the right are selected (right).

intensity A_R and background B can be computed as [40]:

$$\Delta\varphi = \arctan \frac{C_3 - C_1}{C_0 - C_2} \tag{3}$$

$$A_R = \frac{\sqrt{(C_3 - C_1)^2 + (C_0 - C_2)^2}}{2T_{\mathrm{TAP}}\,\mathrm{sinc}(\pi T_{\mathrm{TAP}}/T_P)} \tag{4}$$

$$B = \frac{C_0 + C_1 + C_2 + C_3}{4T_{\mathrm{TAP}}} \tag{5}$$

As reported in Eqs. (3)–(5), to compute the phase shift $\Delta\varphi$ and the received signal A_R, it is not required to know the exact value of the four samples (C_0, C_1, C_2 and C_3), but only their differences ($C_3 - C_1$ and $C_0 - C_2$). Furthermore, the computation of the background intensity requires only the sum of the four different samples ($C_0 + C_1 + C_2 + C_3$). Hence, the two 9-bit bidirectional counters can be selected in turn by the enable signals (*En1*, *En2*) at twice the modulation frequency, thus acquiring respectively $C_0 - C_2$ and $C_3 - C_1$, while the counting *Direction* signal is switched synchronously with the modulation source, in order to perform homodyne (lock-in) demodulation. The remaining counter integrates light over the whole period, hence storing background intensity information. Incidentally, in frequency-domain FLIM, fluorescent samples are stimulated using a modulated light; in such conditions, the emitted fluorescence signal is a delayed and attenuated replica of the input waveform, whose phase-shift and amplitude attenuation strictly depend on the fluorescence lifetimes [59]. Consequently, with no changes, the homodyne detection scheme provided by the pixel can be employed also for frequency-domain FLIM.

C. Imager Architecture

The imager contains 2048 pixels, organized as an array of 64 columns by 32 rows, the row access circuitry, pipelined multiplexers, and global electronics (see Fig. 5). Row access circuitry consists of shift registers, for sequentially addressing data. The multiplexer scans the column bit-lines and the global electronics handles balanced clock distribution, read-out operations, and array initialization. The SPAD array is arranged in a split-frame architecture, so that the readout is performed in parallel on two 32×32 sub-arrays, halving both the minimum integration frame time (i.e. doubling the maximum frame-rate) and the column bus loading capacitance. Furthermore, in order to operate at higher clock rates, the row selection line is split and two row selectors drive only half of the line in an interlaced pattern. Fig. 5 shows the micrograph of the imager, whose dimensions are 9.6 mm $\times$ 4.8 mm. Integrated bypass capacitors and dedicated power-grids have been laid out for reducing ground bounce and voltage drop effects across the whole array.

Fig. 6 shows operations performed during the readout:

1) at the end of the integration time, the external electronics sets the *Frame* signal to trigger the global electronics;
2) global electronics generates a *Store* strobe, which accomplishes data transfer from counters to internal buffer memories, and a *Reset* strobe to initialize counters for the new integration frame (Fig. 1);
3) concurrently, the row access circuitry is initialized to select the first rows of both sub-arrays (Fig. 6, left);
4) when the memories of the first 16 pixels have been read out, the selectors are addressed to connect the following left rows to the data bus (Fig. 6, center);
5) when the first row readout is completed, also the right halves of the following rows are selected (Fig. 6, right).

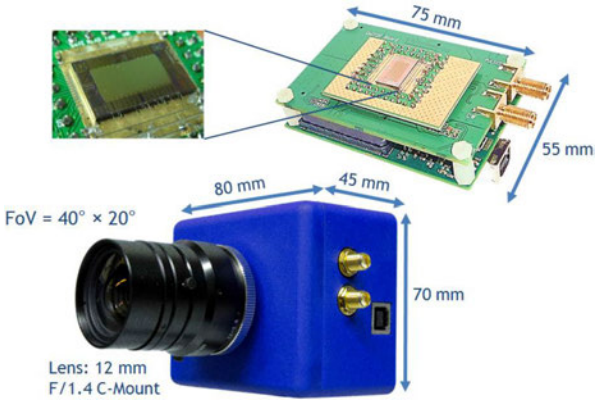

Fig. 7. Assembled system with actual dimensions (right).

Consequently, if T_{CK} is the readout clock period, the output buffers of the first column pixels, which otherwise would have one clock period to let data settle on the column bit-lines, have more time (namely $16{\cdot}T_{CK}$) to write the data on the column bus, thus avoiding erroneous data readout. This allows also relaxing requirements on in-pixel output buffers, hence reducing area occupation. Such an approach, combined with pipelined multiplexers, enables readout speed faster than 100 MHz, since the minimum clock period depends only on the hold and setup time of the multiplexer FFs ($<$1 ns), and on the time employed by the output drivers to charge pads and off-chip traces (some ns), which represents the bottleneck.

Currently, the readout circuit runs at 100 MHz, limited by the external FPGA that controls the array chip. Accordingly, a full readout of the whole imager requires 10.24 μs to access one counter in each pixel (thanks to the double output bus, as shown in Fig. 5). Therefore, 2D acquisitions, requiring only the first counter to be readout, can be acquired up to 100,000 fps. Instead, for time-gated FLIM, such value reduces to 50,000 fps and for 3D ranging frame-rate is limited to 33,000 fps (since three counters must be readout per pixel).

D. SPAD Camera

In order to operate the 64×32 SPAD imager, we developed a compact camera (Fig. 7), which includes a first board with the imager (bonded onto a 72-pin custom-made Pin Grid Array), I/O signal conditioning electronics, and power supply. A second board contains the FPGA (Xilinx Spartan-3) that manages timings of I/O signals, processes data read out from the chip and uploads processed data to a remote PC through a USB 2.0 link, which also provides $+5$ V bias (USB-powered system). The camera is housed in a case supporting a 12 mm F/1.4 C-mount imaging lens, with a $40° \times 20°$ ($H \times V$) field-of-view. The whole system is very rugged and compact (80 mm $\times$ 45 mm $\times$ 70 mm). A MATLAB interface is used for setting the measurement parameters (frame duration, integration time, etc . . .), the system clock frequency, and for data acquisition and post-processing. The power consumption is about 1 W, mostly dissipated by the FPGA board (240 mA), with negligible contribution from the SPAD imager (10 mA).

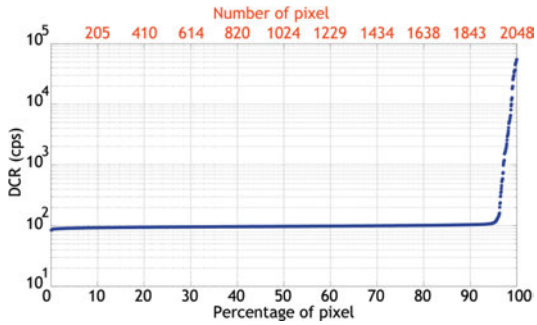

Fig. 8. DCR Inverse cumulative distribution function of the of a sample 64×32 SPAD array, measured at 5 V excess bias.

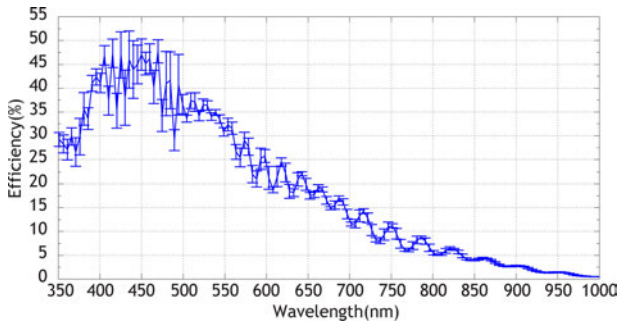

Fig. 9. PDE of all 2048 pixels measured at 5 V excess bias. Note the high PDE uniformity among pixels.

III. Experimental Results

A. Chip Characterization

We performed an in-depth characterization of the CMOS SPAD imager. The characterization of the SPAD performance is exhaustively reported in [46]–[49]. The breakdown voltage ($V_{\rm BD}$) at room temperature is 26.1 V, with a temperature coefficient of 38 mV/K [46]. The Dark Count Rate (DCR) was measured at room temperature with an excess bias voltage ($V_{\rm EX}$) of 5 V. In full working condition, the DCR distribution has a median value of about 100 cps and a mean value of about 425 cps, with 97% of pixels with less than 1 kcps (Fig. 8). The noisiest pixel shows a DCR still lower than 60 kcps. The DCR distribution is uniform across the whole array and the achieved yield of 97%, is the highest value reported in SPAD literature so far.

At 5 V excess bias, Photon Detection Efficiency (PDE) (Fig. 9) tops 45% at 410 nm, with an afterpulsing probability ($P_{\rm AP}$) of about 2.6% [48] at a very short hold-off time of just 20 ns (i.e. a maximum counting rate of about 50 Mcps), a timing resolution of 120 ps [46] at 520 nm wavelength, and negligible crosstalk [49].

Besides these figures of merit, another important one, usually not reported, is the Dynamic Range (DR) defined as the ratio between the maximum achievable count ($C_{\rm MAX}$) and the minimum detectable signal ($C_{\rm MIN}$), i.e. the photon count needed to reach a unitary Signal-to-Noise Ratio (SNR) as a function of the integration time [1].

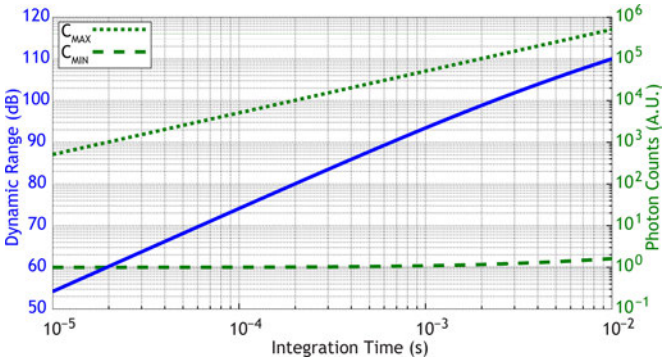

Fig. 10. Dynamic Range (solid line), minimum detectable signal (C_{MIN}, dashed line) and maximum achievable count (C_{MAX}, dotted line) as a function of the integration time. Thanks to the very low noise SPADs, DCR enters into play only at frame rate slower than 100 fps.

Thanks to the very low DCR, the array provides not only single-photon sensitivity (with high PDE) but also ideal shot-noise limited detection almost up to 10 ms integration time (roughly the inverse of the DCR). Therefore, a single signal photon can be discriminated even at 100 fps (Fig. 10). Such a performance is often underestimated in many other similar imagers. For our imager, the DR at 100,000 fps is:

$$\mathrm{DR_{IMAGER}} = 20\log_{10}\frac{C_{\mathrm{MAX}}}{C_{\mathrm{MIN}}} = 20\log_{10}\frac{512}{1} = 54\ \mathrm{dB} \quad (6)$$

At longer integration times (T_{INT}), it is possible to achieve higher DR—at system level—by summing *N* shorter frames, each lasting 10 μs (T_{FRAME}), inside the FPGA. Therefore, the maximum counts is not limited by the counter 9-bit depth, but it will be extend up to $C_{\mathrm{MAX}} = N \cdot 512$.

With this solution, the system-level dynamic rang at can be expressed as:

$$\mathrm{DR_{SYS}} = 20\log_{10}\frac{N\cdot 512}{C_{\mathrm{MIN}}} = 54\ \mathrm{dB} + 20\log_{10}\frac{N}{C_{\mathrm{MIN}}} \quad (7)$$

This enhances DR to 94 dB at 1,000 fps ($N = 100$, $C_{\mathrm{MIN}} = 1$) and to 110 dB at 100 fps ($N = 1000$, $C_{\mathrm{MIN}} < 2$), as shown in Fig. 10. This is the highest value achieved among different SPAD sensors reported in literature (Table I) and ensure a single-photon sensitivity almost over the whole frame rate range typical for SPAD cameras (>100 fps).

B. High Frame-Rate Imaging

An advantage of the SPAD imagers is their ability to act as optical "analog-to-digital" converters, thus removing readout noise, since each photon is converted in a 1-bit count. Correspondingly, no limitation on minimum integration time, due to SNR degradation, is set (contrary to CCD and CMOS imagers) and sampling broadband signals becomes feasible. An example of high-speed imaging application is optical muzzle flash detection [59], which requires fast sensing of transient events with characteristic times between few microseconds up to some milliseconds, and where only recently, single-pixel SPADs have been tested [54].

For security issues, instead of employing a gun and studying its muzzle flame, we acquired the flash from a commercial camera strobe light. Fig. 11 shows the light waveform acquired at 100 kfps: just before exposure begins, the lighting unit emits a pre-flash pulse, lasting 70 μs, which is used by the through-the-lens metering system to adjust the flash exposure. After 31 ms, during which the shutter is opened (first curtain sync), the flash tube is fully triggered. As the flash's capacitor discharges, the light intensity exponentially dims and fades out in about 2 ms. The acquired signal has a very similar shape (and bandwidth) compared to the muzzle response measured in [54], which exhibits a short 500 μs pulse followed by a longer 4 ms response.

C. Time-Gated Single-Photon Counting

In time-gated detection-based methods, the optical signal is detected sequentially in several gates, each shifted by a different delay time relative to the trigger pulse [42]. Given a certain trigger frequency, our system is able to generate up to 256 delays (each equal to 1/256 th of the trigger period) thanks to FPGA digital clock managers [61].

Here, we show how TGSPC can be used to implement an ultra-high speed system capable of capturing the motion of light. To this purpose, we used 1.75 ns gate windows and a 50 MHz trigger frequency, so each delay was equal to 80 ps. The trigger signal was sent to a 450 nm pulsed laser, which shone the scene depicted in Fig. 12. Sample frames (Fig. 13) from the acquired movie [60] show the light hitting different objects during its propagation. From the acquired waveforms it is also possible to compute the distance between the first and the second objects (2.6 ns $= 34$ cm) and between the second objects and the white panel (3.4 ns $= 51$ cm). Since each sequential interframe time is 80 ps, similarly to sequential equivalent-time sampling for oscilloscopes [62], we can define a sequential equivalent-frame rate, which is equal to 12.5 Gfps for the presented camera. Therefore, the imager can be used as a bidimensional streak camera or to perform nanosecond and picosecond transient absorption spectroscopy (e.g. pump-probe spectroscopy) [63]. With respect to the equivalent 100 Gfps imaging system described in [64], the current system is four time slower, but with respect to the effective acquisition time it is much more faster as the whole movie has been acquired in only 2.56 s, to be compared to 1 h acquisition in [64]. Moreover, the current system is very compact, not power-hungry, and cost-effective with the advantage of employing a bidimensional sensor and therefore the same pixel resolution—if more than 2048 pixels are needed—may be achieved faster.

D. 3D Ranging

In order to assess the 3D performance, the camera was equipped with a compact illuminator consisting of 36 LEDs, with emission peaks at 850 nm wavelength and a 40 nm wavelength variation measured as full-width at half maximum (FWHM), arranged in a daisy chain as shown in Fig. 14. The maximum optical power is about 800 mW.

We acquired 3D pictures of a reference scene (Fig. 15), at 100 fps, with a 20 MHz modulation frequency ($d_{\mathrm{MAX}} = 7.5$ m)

TABLE I
SUMMARY OF SYSTEM PERFORMANCES FOR VARIOUS SPADS ARRAYS AVAILABLE IN LITERATURE

Work	[29]	[32]	[35]	[36]	[37]	[41]	[45]	this work	Unit
Tech. Node	350	180	800	350	130	180	350	**350**	nm
Pixel Resolution	128×128	340×96	64×1	60×48	128×96	80×60	32×32	$\mathbf{64 \times 32}$	Pixels
SPAD Diameter	7	25	100	7	9	-	20	**30**	μm
SPAD $\mathbf{T_{HO}}$	100	40	n.a.	40	50	-	100	**20**	ns
Median DCR	694	2650*	<1000	245	100	-	4000	**100**	cps
Pixel Fill Factor	6	70	n.a.	0.5	3.17	24	3.14	**3.14**	%
Imaging Lens	1.4	n.a.	n.a.	1.4	1.4	1.4	1.4	**1.4**	-
Illumination Wavelength	635	870	905	850	850	850	808	**850**	nm
Narrowband Filter Width	11	n.a.	n.a.	40	40	n.a.	40	**40**	nm
Illumination Frequency	40	0.2	n.a.	30	3.33	20	6.67	**7.5**	MHz
Illumination Field-of-View	5	170×4.5	n.a.	50×40	40	n.a.	40	$\mathbf{40 \times 20}$	°
Illumination Average Power	1	40	250	800	50	80	750	**800**	mW
PDE at Illum. Wavelength	10	n.a.	0.62	3	5	n.a.	7	**5**	%
Unambiguous Range	3.75	128	5	5	45	7.5	22.5	**20**	m
Integration Time	50	100	n.a.	45	50	50	100	**10**	ms
Target Refelectivity	n.a.	100	n.a.	n.a.	100	100	70	**70**	%
Worst Accuracy	0.9	36.6	n.a.	11	0.5	4	n.a.	**80**	cm
Worst Precision @ D_{MEAS}	0.5	10	5	3.8	16	14	27	**85**	cm
D_{MEAS}	3.6	100	2	2.4	2.4	2.4	14	**20**	m
Background Light Condition	0.15	80	n.a.	0.15	0.11	n.a.	0.45	**0.45**	klux
Chip Power Dissipation	150	n.a.	1	35	40	18	20	**50**	mW
Max Readout Bandwidth	7.68	6.8	n.a.	2.13	10.24	2	0.8	**1.8**	Gbps
Max Frame Rate	39	n.a.	1	46.3	70	n.a.	100	**100**	kfps
Dynamic Range ($T_{\mathrm{INT}} = 10$ ms***)***	90	93	n.a.	101	102	51	83	**110**	dB
TOF Technique	Direct	Direct	PL	CW	CW	CW	PL	**CW**	-

*Mean Value

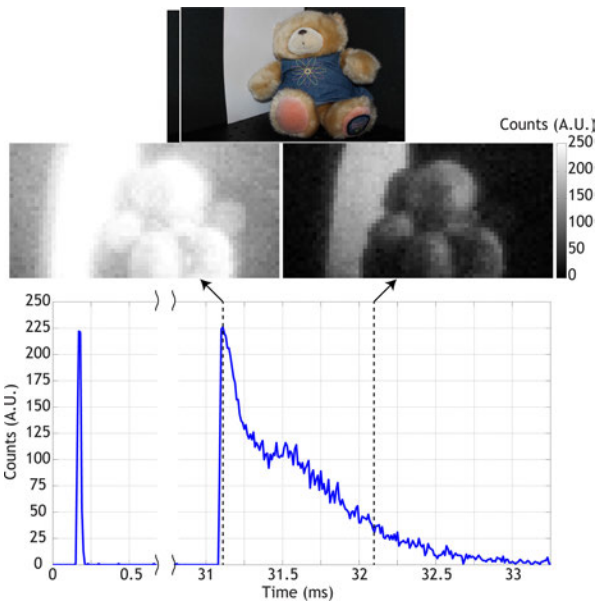

Fig. 11. Fast 2D movie [60] acquired at 100 kfps, of a reference scene (top) illuminated by a flash lamp. Two frames (center) and discharge waveform intensity (bottom) recorded by one pixel (position 17,32). The dashed lines indicates the time instants when the two frames were acquired.

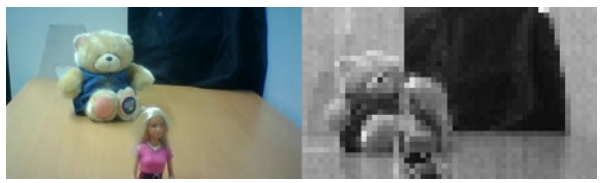

Fig. 12. Reference scene and 2D image acquired with the SPAD imager.

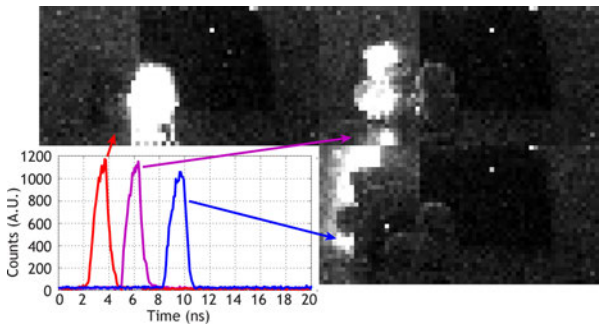

Fig. 13. Light propagation acquired at sequential equivalent-frame rate of 12.5 Gfps. Pictures show three different objects shined by light while propagating along its path.

and capturing 200 frames per acquisition. To decrease the background level and improve precision [36], a narrow bandpass (40 nm FWHM) filter was mounted on the camera lens.

The integration windows' width T_{TAP} (Fig. 4) was set equal to 1/4th of the modulation period T_P. This value represents a tradeoff between photon collection efficiency and distance precision: at longer integration times, more photons are collected and SNR increases, but concurrently the four samples are averaged and eventually overlap, so that phase information is gradually lost and the overall measurement precision reduces. With the chosen value, we are able to open four integration windows, within the same period, and to accumulate the four

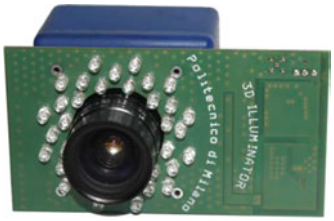

Fig. 14. Camera with optics and the illumination system.

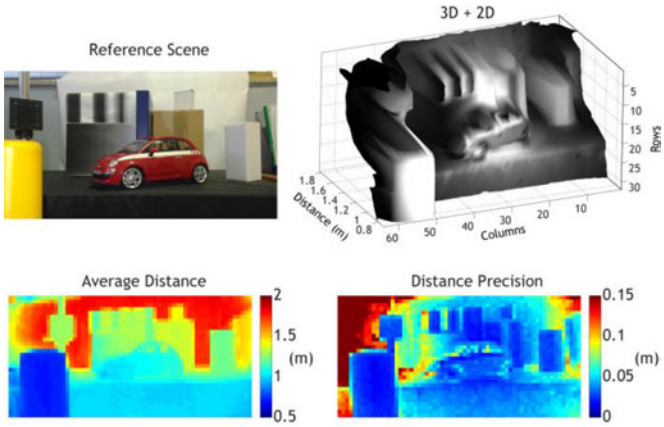

Fig. 15. Reference scene and combined 3D/2D image (top). 3D image acquired at 100 fps with corresponding precision computed over 200 frames.

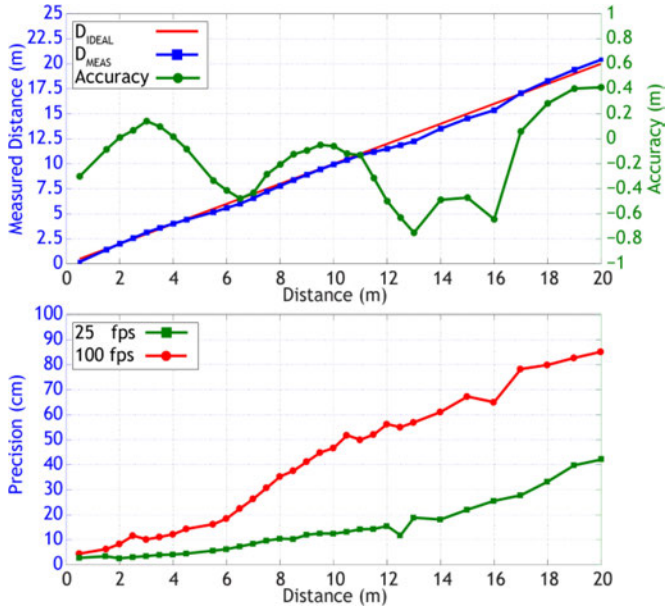

Fig. 16. Distance and accuracy (top) measured over a 20 m distance range. Accuracy shows typical oscillation caused by the third order harmonic in the modulated light source. Precision (bottom) is 90 cm at farthest distances and less than 10 cm at short distances with just 10 ms integration. At longer integration times (25 fps) the precision is almost halved.

samples in a single frame, without missing any photon and with no overlapping.

3D measurement of the reference scene and corresponding precision are shown in Fig. 15: a non-uniform illumination pattern causes a degradation of distance precision moving from the brighter center to the darker edges of the FOV.

The camera was also characterized using a non-cooperative target in a real scenario: an underground parking lot. The modulation frequency was set to reach a non-ambiguous range of 20 m ($f_{\mathrm{MOD}} = 7.5$ MHz). For each measured distance, we acquired 1000 frames at 100 fps and 25 fps. Accuracy and precision are shown in Fig. 16. Conceived as a sort of benchmark, Table I summarizes the performance of the camera and illuminator ensemble compared to other SPAD-based rangefinders reported in literature: dTOF sensors achieve better precision and accuracy with respect to iTOF arrays, at the expenses of higher dissipation and higher bandwidth, but with less illumination power. Compared to other iTOF systems, the reported structure presents some advantages: if compared to the results reported in [39], where four different frames were required (one for each tap), we achieve unitary photon collection per frame with a 4-fold higher acquisition speed. There are, also, some advantages in terms of speed and precision, if compared with the one reported in [36], whose in-pixel digital circuitry consists of a 2-to-1 multiplexer and two 8-bit counters operating in an interlaced counting scheme. That approach requires two readout frames and an integration window equal to 50% of T_P to collect all signal photon and rolling shutter readout. Moreover, thanks to the up-down counters, we attain in-pixel background suppression thus extending the intrinsic counting range. Finally, knowledge on background counts can be used to check saturation—i.e. if the SPAD is saturated distance information is no more correct, so the maximum tolerable background light is roughly $1/T_{\mathrm{HO}}$—and to correct pile-up distortion (which reduces distance precision, as well [36]). Concerning 3D ranging performance, the accuracy of the system is lower compared to other approach, due to a strong third order harmonic component ($f_{3d} = 22.5$ MHz, $d_{3d} = 6.7$ m), which impairs the overall linearity [40]. Concerning the distance precision, Fig. 16 shows that the camera provides a precision of 3.1 cm at 2.5 m, 7.5 MHz modulation and 25 fps, while a precision of 2.8 cm, at the same distance but at 30 MHz modulation and 45 ms integration time, was reported in [36]. The present sensor also shows a precision of 18 cm at 14 m thus improving the performance of our previous system [45], where a precision of 27 cm is reported. Even at higher frame rate (100 fps), distance precision is still less than 10 cm at 2 m and below 85 cm at 20 m.

IV. Conclusion

We presented the design and the characterization of a multipurpose 64×32 CMOS SPAD array, fabricated in a high-voltage 0.35 μm CMOS technology. The building block of the system is a pixel consisting of a SPAD detector and three individually selectable and fully independent counters able not only to measure light through photon-counting in either free-running or time-gated mode, and store 2D intensity map, but also to perform smart light demodulation with in-pixel background suppression. Pixel-level memories allow fully parallel imaging, thus preventing typical motion artefacts (skew, wobble, motion blur) and partial exposure effects, which otherwise

would hinder the use of the imager in those applications acquiring fast moving objects (e.g. automotive). The image sensor exhibits the best-in-class noise performance (100 cps at 5 V excess bias, for a 30 μm SPAD) and low afterpulsing probability (2.6% at 20 ns hold-off time and at room temperature), which results in fast (100 fps) depth measurement with a precision better than 90 cm over 20 m. Moreover high dynamic range (up to 110 dB at 100 fps) with peak PDE above 45% at 410 nm ensure true single-photon sensitivity jointly to high-frame rate acquisition (up to 100 kfps).

The amount of integrated electronics limits the pixel dimension and the resolution, but it provides flexibility to the overall imaging chip, which can be suited for molecular imaging applications in both time-domain, like FLIM and FCS, and frequency-domain FLIM as well as 3D ranging while maintaining good fill-factor, power consumption and photon detection efficiency.

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