Voltage Regulators Design Through Advanced Mixed-Mode Circuit Simulation

F. Bizzarri, Member, IEEE, A. Brambilla, and S. Saggini

I. INTRODUCTION

DESIGNERS of switching power suppliers typically approximate their behavior by subdividing one working cycle in various sequential phases/subtopologies and apply specific and simplified techniques to each phase to grasp the main features of the overall dynamics. This approach is justified by the fact that often MOSFETs and diodes are the unique nonlinear elements and the original nonlinear circuit reduces to a linear time varying one by modeling them as ideal switches. Subdivision is reasonable if the converter has a simple schematic/structure and the control strategy can be described by a limited number of combinatorial functions and state machines. Each linear subtopology is thus solved by pen and paper. In these cases, the entire system can be modeled by a differential algebraic equation (DAE) with switching vector field and/or algebraic constraints and with possibly discontinuous (digital) state variables. As shown in previous works (see for example [1]–[4] and references therein), this approach allows to describe a complete working cycle of the converter (and study its stability) by exploiting the product of constant fundamental matrices, one for each subtopology that the converter assumes.

We present here a general and fully automatic simulation method, based on an extension of the state transition matrix, allowing 1) to accurately and efficiently compute the periodic steady-state solution of switching power suppliers described by complex topologies (without substituting nonlinear elements with simplified linear ones) through the shooting (SH) method, 2) to study the stability of the steady state, 3) to determine time-varying transfer functions (e.g., the input/output one) through the periodic linear phasor (PAC) analysis, and 4) to evaluate the performances of the chosen controller.¹

To describe the proposed approach, the design of a voltage regulator module (VRM) supplying modern computers is used as a test vehicle. This peculiar choice is driven by the extremely large market of computers, and thus of VRMs, triggering a large interest in finding new solutions lowering cost.

The increasing integration of transistors in a chip directly impacts on the supply current that can be greater than 100 A with peaks above 150 A. In nowadays microprocessors, the extremely low value of supply voltage (about 1.0 V), makes very narrow (about 130 mV) the interval inside which this voltage is allowed to vary when there is a fast step in the requested power. The large supply current heavily burdens the transient response since load current swings of 100 A (with slew rates of 300 A/µs⁻¹) must be correctly handled [7]. These targets can be reached by using a very large output capacitance but this increases size and cost. Given a control strategy, our design target is to select the minimum capacitance value that ensures the desired performance and obviously the stability of the VRM. To achieve this goal, the adaptive voltage position (AVP) approach [8] is exploited. If the transient dynamics is characterized by the absence of spikes and oscillations, the AVP design is optimal. The AVP can be accomplished in a straightforward way when the VRM acts as an independent voltage source connected in series to a resistor. The constant resistive output impedance design for the VRM thus leads to an optimal solution for load transients [9]. PAC analysis is a promising tool to this kind of design and its extension to switching power supplies is extremely valuable.

¹In the following, we refer to the conventional shooting (SH) and periodic linear phasor (PAC) analyses providing no details on them since they are widely discussed in the literature (e.g., [5], [6]).
The switching frequency is 200 kHz.

The cutset can be removed by substituting, for example, a voltage-controlled voltage generator.

As a gross simplification helping in first dimensioning the elements of the VRM, the block schematic circuit reported in Fig. 2 implements the equivalent linear time-invariant model shown in Fig. 1. The controller includes also a current sharing block not shown in Fig. 2. The limit of the validity of this approximation will be verified by exploiting the proposed simulation approach. The analytical approach to obtain a purely real \( R_l \) impedance “seen” by the load considers the parallel connection of the impedances of the converter and of the output bank of capacitors. These capacitors are connected in parallel and are modeled for simplicity by \( C \) in Fig. 2; the corresponding overall equivalent series resistance (ESR) is modeled by \( R_c \) and the \( L_c \) parasitic equivalent inductance is neglected.

By choosing \( R_c = R_l \) (i.e., the desired impedance will match that of the capacitors bank), the relation governing the constant output impedance is

\[
\frac{sC}{1 + sC R_l G_c(s)} + \frac{I_l(s)}{V_o(s)} = \frac{1}{R_l} \frac{I_o(s)}{V_o(s)}
\]

where \( G_b(s) \) and \( G_c(s) \) represent the admittance of the board capacitors and of the converter, respectively. By exploiting the relations among the electrical variables involved in the linear time-invariant model shown in Fig. 2, we have

\[
I_l(s)(sL + R_p)N_{p1}^{-1} = V_o(s) - V_p(s)
\]

\[
V_p(s) = -H(s) (I_l(s)a + bV_o(s)) k_w
\]

and one can derive

\[
G_c(s) = \frac{1}{R_l} \frac{s}{s^2 + \frac{L}{k_w R_l k_b N_p b}} + \frac{1 + s + \frac{k_p k_w b}{k_l k_w b}}{N_p k_w R_l k_b - \frac{a}{R_l b}}.
\]

It is then possible to obtain a constant output impedance of the VRM by choosing

\[
a = -R_l, \quad b = 1, \quad k_p = \frac{L - C R_l^2 N_p}{k_w C R_l^2 N_p} k_l = R_p - R_l N_p
\]

determining thus the controller parameters yielding the AVP. It is worth noting that the controller admittance is far from (3) also because of sampling effect, limited slew rate of the inductor current, and possible nonlinearities of control block (such as for example saturations).

The design is completed by the schematic of the digital circuit generating the driving signals of a single phase of the VRM. The \( E_{ir} \) input terminal reads the signal at the output of the PI block shown in Fig. 2, i.e., across the CPU; the \( V_{saw} \) sawtooth waveform (dashed line) is compared with \( E_{ir} \) by the \( C_1 \) comparator that generates a square wave with a proper duty cycle. The \( V_o \) input reads the 50% duty-cycle square waveform (solid line) synchronous with the sawtooth one. The \( V_o \) gate signal is triggered when \( E_{ir} \) becomes lower than \( V_{saw} \) with \( V_o \) high and reset when both \( V_o \) and the comparator output are low. The FLIP-FLOP limits the generation of one and only one \( V_o \) gate triggering signal per working cycle of the VRM. The \( V_{saw} \) waveform and the corresponding square waveform are shifted by \( T_{saw}/3 \) among the three phases of the VRM.

Fig. 1. Schematic of the VRM and the lumped model of the motherboard. \( L_{f1} = L_{f2} = L_{f3} = 280 \text{ nH}, R_{f1} = R_{f2} = R_{f3} = 1 \Omega \). The equivalent \( C R_l L \) series circuit represents a bank of \( B \) identical capacitors connected in parallel (each capacitor of 470 \( \mu \text{F} \) has 5 m\( \Omega \) equivalent series resistance (ESR) and a series inductance of 2 nH). The values of the components enclosed in the motherboard block are reported in [7]. The switching frequency is 200 kHz.

Fig. 2. Simplified linear block schematic of the dc/dc converter. The PI controller is described by \( H(s) = k_1/s + k_2 \) being \( k_1 \) and \( k_2 \) real constant parameters. The \( a \), \( b \), and \( k_p \) blocks model the gain in sensing the \( I_l(s) \) current flowing in the \( L \) inductor, the \( V_o(s) \) output voltage across the load and the gain of the PWM modulator whose output voltage is \( V_p(s) \). The \( v_{ref} \) input voltage sets the value of the VRM output voltage.

Fig. 3. Schematic of the circuit generating the gate signal of the switching MOSFETs of a single phase of the VRM. The \( E_{ir} \) input terminal reads the signal at the output of the PI block shown in Fig. 2, i.e., across the CPU; the \( V_{saw} \) sawtooth waveform (dashed line) is compared with \( E_{ir} \) by the \( C_1 \) comparator that generates a square wave with a proper duty cycle. The \( V_o \) input reads the 50% duty-cycle square waveform (solid line) synchronous with the sawtooth one. The \( V_o \) gate signal is triggered when \( E_{ir} \) becomes lower than \( V_{saw} \) with \( V_o \) high and reset when both \( V_o \) and the comparator output are low. The FLIP-FLOP limits the generation of one and only one \( V_o \) gate triggering signal per working cycle of the VRM. The \( V_{saw} \) waveform and the corresponding square waveform are shifted by \( T_{saw}/3 \) among the three phases of the VRM.
III. PROPOSED METHOD

The general model of a converter can be written as

$$\begin{align*}
\dot{x} + f(x, y, r, w, t) &= 0 \\
\dot{r} &= 0 \\
g(x, y) &= 0 \\
c(w, r) &= 0
\end{align*}$$

(5)

where $x(t) : \mathbb{R} \to \mathbb{R}^N$ and $y(t) : \mathbb{R} \to \mathbb{R}^M$ represent the time evolution of differential and algebraic variables, respectively, linked by $g(x, y) : \mathbb{R}^{N+M} \to \mathbb{R}^r$, $r(t) : \mathbb{R} \to \{0, 1\}^R$ represent single bits stored in digital state variables ($R$ binary registers) linked to the $w(t) : \mathbb{R} \to \{0, 1\}^C$ combinatorial digital variables by $c(w, r) : \{0, 1\}^{R+C} \to \{0, 1\}^C$. $f(x, y, r, w, t) : \mathbb{R}^{N+M+R+C+1} \to \mathbb{R}^N$ is the vector field switching according to the values assumed by $r$, $w$, and possibly $y$.

From (5), the digital state variables seem to be static and this is in general true a part from a finite set of time instants where the $r$ variables abruptly change their values. These digital events can be monitored by a proper set of $H$ (say $H$) digital components $h(x, y, t) = 0$, where $h(x, y, t) : \mathbb{R}^{N+M+1} \to \mathbb{R}^H$. When a trajectory in the state space hits one of the $H$ manifolds [say $h_j(x, y, t) = 0$] at $t = t_j$, $r_0(t_j)$ (i.e., $r(t_j)$ immediately before the event) is instantaneously mapped in $r_+(t_j) = B_j(x(t_j), y(t_j), r_0(t_j), w_0(t_j))$, where $B_j$ (for $j = 1, \ldots, H$) are reset functions.

In our case, by referring to Fig. 3, we can identify three manifolds introduced by the three $C_1$ comparators (one per phase). These manifolds are automatically defined by considering the VERILOG-RTL description of the digital circuit and are selected according to the state of the FLIP-FLOP.

If we want to efficiently compute the steady-state solution of (5) by the SH method and then perform a PAC analysis to derive any periodic time varying transfer function of the VRM, the system fundamental matrix must be accurately computed [10]–[12]. This can be done in a conventional way between digital events, but it is not straightforward at discontinuities of the digital variables inducing switching in the $f$ vector field.

A. Variational Model

To evaluate the fundamental matrix of a hybrid dynamical system as (5), exhibiting discontinuities in the vector field and/or in the state variables, the saltation matrix operator must be used [13]. To understand how this linear operator is defined and how it must be used, in the following we assume that (5) reduces to an ordinary differential equation and that no combinatorial variables are involved.\(^5\)

\(^3\)In (5), the initial conditions are not specified.

\(^4\)One can adopt also more accurate descriptions of this class of analog/digital (A/D) circuits. We assumed that $V_{\text{wmax}}$, $E_{\text{j}}$, and $V_{\text{a}}$ are analog but one can resort to A/D converters to properly quantify these voltages. Of course this implies larger $H$. Nevertheless, even in this case, we have expanded the VERILOGA language and exploited the fact that the A/D converters linking the analog and digital parts of the circuit change their output codes any time the input voltages cross predefined thresholds which define the manifolds.

\(^5\)Complete description of the DAE case can be found in [10].
We compute the \( R_{Ao}(f) \) impedance “seen” by \( A_0 \) through the PAC analysis [6], [14] according to what reported in [7]. \( R_{Ao}(f) \) can be considered as the periodic time-varying transfer function between the current injected by \( A_0 \) and the variation of the \( V_{Ao} \) voltage (CPU land). This result is shown in Fig. 6; the real part of \( R_{Ao}(f) \) is almost perfectly equal to the sum of \( R_i \) and \( R_m \) till about 10 kHz; in this frequency range, the imaginary part of \( R_{Ao}(f) \) is almost null.

Since the target of our design is to minimize the capacitor bank ensuring stability, we removed one by one the capacitors till one of the Floquet multipliers exits the unit circle.\(^6\) For the considered values and number of capacitors constituting the bank, \( k_g \) and \( k_l \) are updated according to (4). This exit happens when the number of capacitors is reduced from \( B = 4 \) to \( B = 3 \) when \( \mu_1 \) is equal to 1.1925 [15], i.e., the \( T_o \)-periodic steady-state solution observed for \( B = 3 \) is unstable. This value, i.e., the stability border of the VRM, deeply depends on the implemented digital control schema. We computed the \( R_{Ao}(f) \) for \( B = 4 \) (see Fig. 6). We easily see that even though the VRM is stable, the quality of \( R_{Ao}(f) \) is unacceptable (too high value [7]). In other words, even before reaching the stability boundary, the performances of the VRM reduce in term of the controller capabilities to yield the AVP.

V. CONCLUSION

We exploited an extension to hybrid dynamical systems of both the conventional SH method and the PAC analysis to enhance the design of a VRM. We have shown that the main characteristics of the VRM such as its stability and periodic transfer functions can be directly and efficiently derived. This allowed to estimate the performances of the controller in yielding the AVP as a function of the circuit design parameters. The extended methods have general validity and in principle can be applied to any circuit modeled through a hybrid DAE.

REFERENCES


---

\(^6\)SH analyses were performed in tens of seconds on a DELL6600 computer running LINUX; the PAC ones were performed in \( \approx 2.5 \) s. The circuit simulator PAN, developed by the authors, has been used and it is available at the URL: http://brambilla.ws.dei.polimi.it.