Impact of the array background pattern on cycling-induced threshold-voltage instabilities in nanoscale NAND Flash memories

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1. Introduction

Cycling-induced threshold-voltage (V_T) instabilities represent one of the most relevant reliability issues for nanoscale NAND Flash memories. Instabilities are mainly the result of charge detrapping from the tunnel oxide of the memory cells, giving rise to unwanted displacements of their V_T during idle/bake periods [1–8]. Although the statistical nature of the detrapping process and, in turn, of the resulting V_T shift (ΔV_T) has been clearly recognized [3,6,9,10], an average reduction of V_T as time elapses is the typical feature of detrapping in Flash arrays, owing to a dominant neutralization of negative charge in the cell tunnel-oxide [3–5,7]. This negative ΔV_T is particularly detrimental for multi-level devices where the increase of storage density is traded off with the reduction of noise margins [11].

In this paper, extending what presented in [12], we provide experimental evidence showing that the average ΔV_T ($\langle \Delta V_T \rangle$) coming from detrapping in a nanoscale NAND Flash array does not depend only on the memory state of the cells being monitored (*victim cells*), but also on the state of their first neighboring cells (*aggressor cells*). In particular, experimental results show that the $\langle \Delta V_T \rangle$ of the victim cells increases when their aggressor cells are on a higher V_T level. This represents an additional interference effect among the cells of a state-of-the-art NAND Flash array, whose magnitude appears rather strong when victim cells are on a low V_T state. From the collected experimental results, a physical picture explaining the phenomenon is provided and validated with the help of 3-Dimensional (3-D) numerical simulations.

2. Experimental results

2.1. Test scheme

We investigated the $\langle \Delta V_T \rangle$ coming from charge detrapping during post-cycling bake experiments on our 20 nm multi-level NAND Flash technology [11]. To this aim, a total number of 10 k pro-gram/erase cycles were first performed on a memory block, ran-domly moving the cells from the erased (E) state to one of the three possible programmed levels of the device (namely, from lowest to highest, $L1$, $L2$ and $L3$). At the end of cycling, a random background pattern (BP) was created in the array and V_T instabilities were monitored during a bake test at $T_B = 125$ °C. In order to explore the BP sensitivity of $\langle \Delta V_T \rangle$, the entire array V_T map was periodically gathered by stopping the bake experiment, cooling the sample down to room temperature and accomplishing read operations on all of the array cells. From the array V_T maps, the ΔV_T of each cell was then extracted as a function of the bake time t_B and the $\langle \Delta V_T \rangle$ of cells in the same initial (pre-bake) state and with the same BP of aggressor cells was calculated. The definition of victim and aggressor cells in the NAND array is highlighted in Fig. 1: each cell in the array was considered a victim cell

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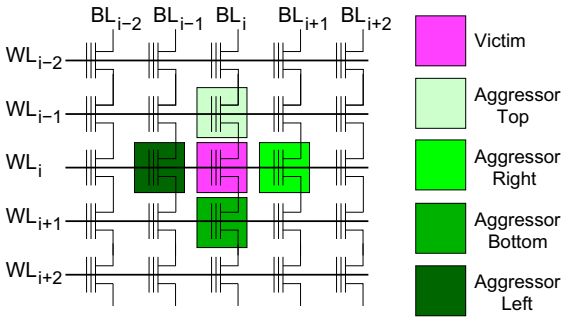

Fig. 1. Schematics for cell connection in the NAND array, highlighting a victim cell and its four neighboring aggressor cells. The BP given by the aggressor cells will be indicated in the following keeping the order: top, right, bottom, left.

surrounded by four aggressor cells placed at its top, right, bottom and left (the BP resulting from the state of the aggressor cells will be indicated keeping this order from now on).

2.2. Uniform background patterns

Fig. 2 shows the $\langle \Delta V_T \rangle$ transient of the victim cells on level $L1$ (a), $L2$ (b) and $L3$ (c) having a uniform BP of aggressor cells around them during the bake experiment. A relevant BP sensitivity of V_T instabilities during bake clearly appears for victim cells on $L1$, with an increase of $\langle \Delta V_T \rangle$ moving from the E,E,E,E to the $L3,L3,L3,L3$ BP. The pattern sensitivity, however, decreases for victim cells on level $L2$ and almost vanishes for victim cells on level $L3$.

In order to investigate more in detail the BP sensitivity of Fig. 2, we fit the $\langle \Delta V_T \rangle$ transients according to the following logarithmic trend [5]:

$$\langle \Delta V_T \rangle = -\alpha \cdot \ln\left(1 + \frac{t_B}{t_B^*}\right) \quad (1)$$

where t_B^* is the equivalent time elapsed between the end of cycling and the first read operation on the array [5]. From the fitting, the slope α of the logarithmic trend can be extracted as a function of the state of the victim and of the aggressor cells, as shown in Fig. 3. Results reveal, first of all, the typical increase of α with the initial V_T level of the victim cells [5], coming from a dependence of the detrapping rate on the electric field in the cell tunnel-oxide during bake. Besides, results clearly highlight that the value of α of the victim cells on level $L1$ increases by about a factor of 2.5 when moving from the E,E,E,E to the $L3,L3,L3,L3$ BP of the aggressor cells. This increase is, instead, only of about a factor of 1.5 and 1.2 for the victim cells on level $L2$ and $L3$, respectively.

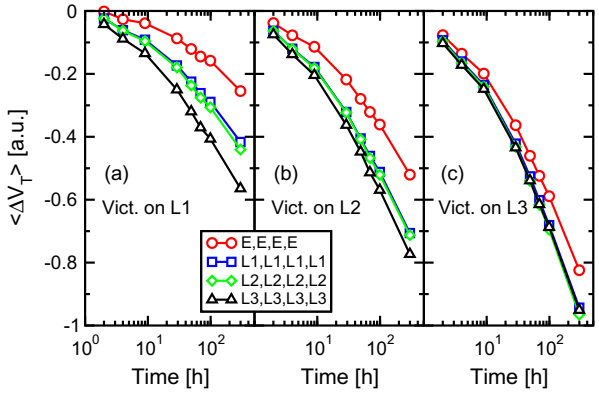

Fig. 2. $\langle \Delta V_T \rangle$ transient of the victim cells on level $L1$ (a), $L2$ (b) and $L3$ (c) when their aggressor cells are all on level E (red curve), $L1$ (blue curve), $L2$ (green curve) and $L3$ (black curve). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

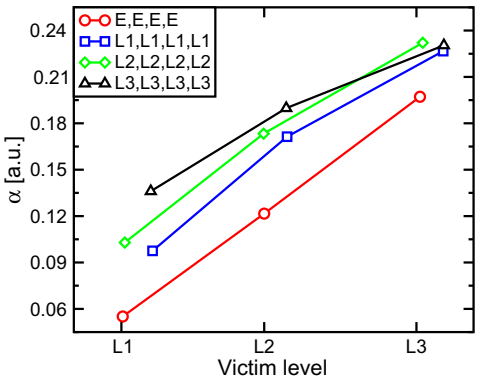

Fig. 3. Values of α resulting from the fitting of the $\langle \Delta V_T \rangle$ transient of the victim cells with (1), as a function of the state of the victim cells and for the four possible uniform patterns of the aggressor cells.

Results in Figs. 2 and 3 highlighted that the array BP has a non-negligible impact on the post-cycling data retention of the cells in a nanoscale NAND array. Note, to this regard, that the observed dependence of $\langle \Delta V_T \rangle$ on the BP is specific of the detrap-ping process, while different results have been reported in other working conditions for other competing mechanisms [13]. However, since the attempt to increase the number of bits per cell to improve the equivalent integration density of the memory array comes along with a reduction of its noise margins, making the differences in the $\langle \Delta V_T \rangle$ resulting from different BP in Figs. 2 and 3 largely relevant for array operation, these results confirm that a careful assessment of the reliability of nanoscale NAND Flash arrays cannot avoid, first of all, addressing different BP and, more-over, that the worst case BP may change during array lifetime. This sensitivity of cell reliability to the array BP can be considered, in general terms, a direct consequence of the closest and closest proximity of the cells in the NAND array as technology scaling proceeds, enhancing their electrostatic interaction during array operation.

2.3. Non-uniform background patterns

To gain a deeper insight on the basic phenomenology of the effect shown in Figs. 2 and 3, we investigated the $\langle \Delta V_T \rangle$ of the victim cells in the array having a non-uniform BP around them during data retention. The results obtained when only the two aggressor cells along either the bit-line or the word-line direction are on a programmed state are shown in Figs. 4 and 5, respectively. In both cases, the $\langle \Delta V_T \rangle$ transient qualitatively reveals the same BP sensitivity highlighted in Fig. 2. However, while the sensitivity remains clear and strong in the case only aggressor cells along the bit-line direction are programmed (Fig. 4), it appears largely reduced when aggressor cells along the word-line direction only are programmed (Fig. 5). This can be clearly observed also in Fig. 6, where the values of α extracted from the fitting of the transients of Figs. 4 and 5 according to (1) are reported. These results reveal that the observed cell-to-cell interference effect is mostly related to the aggressor cells in the bit-line direction. This is further confirmed by Fig. 7, showing the values of α in the case where only the aggressor cell at the bottom (a) or at the left (b) of the victim cell is programmed.

3. Physical origin of the new interference effect

3.1. Discussion

The experimental results presented in the previous section highlighted a new cell-to-cell interference effect occurring in nanoscale NAND Flash arrays and making the post-cycling V_T

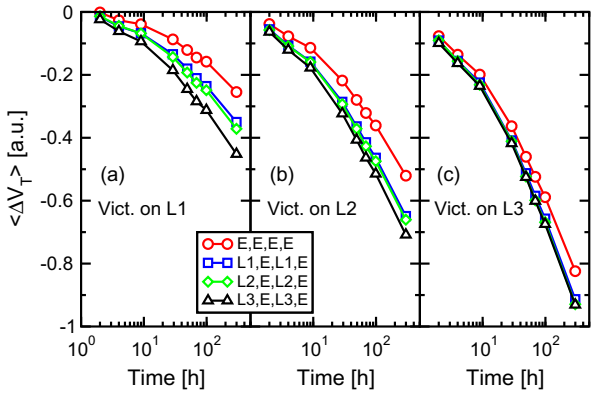

Fig. 4. Same as in Fig. 2, but for non-uniform BP with only the two aggressor cells along the bit-line direction on a programmed state.

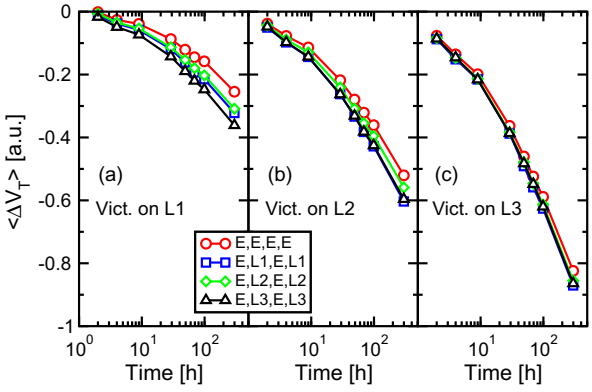

Fig. 5. Same as in Fig. 2, but for non-uniform BP with only the two aggressor cells along the word-line direction on a programmed state.

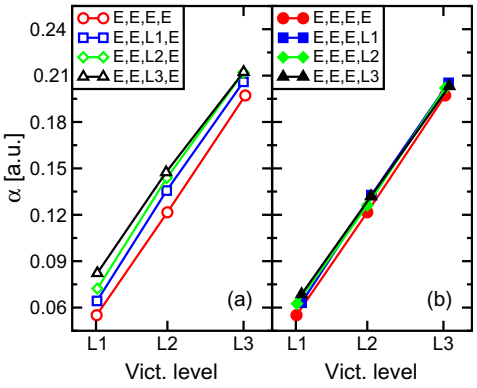

Fig. 7. Same as in Fig. 3, but when only one aggressor cell in the bit-line direction (a) or in the word-line direction (b) is on a programmed state.

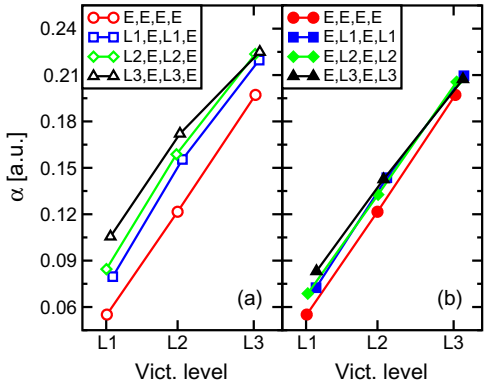

Fig. 6. Same as in Fig. 3, but when only the aggressor cells in the bit-line direction (a) or in the word-line direction (b) are on a programmed state.

instabilities of the victim cells dependent on the state of their adjacent aggressor cells. Note that this dependence cannot be the result of a different detrapping rate in the victim cells for different BP of their aggressor cells. Fig. 3 shows, in fact, that in order to achieve the same increase of α obtained when moving the aggressor cells from the E, E, E, E to the $L3, L3, L3, L3$ BP with the victim cells on level $L1$, the victim cells should be moved above the level $L2$ in the presence of an E, E, E, E state. This means that a relevant change of the electrostatics of the victim cells would be required to explain the BP sensitivity of their ΔV_T with a field dependence of their detrapping process. Considering that the initial V_T of the victim cells seeing a different BP are only slightly different, this relevant change of their electrostatics seems unlikely.

A strong change in the electrostatics of the aggressor cells occurs, instead, when these cells are moved from the E to the $L3$ level and results in a relevant increase of their detrapping rate. Starting from this point, the sensitivity of the ΔV_T of the victim cells to their BP can be explained in terms of a contribution given by charge detrapping in the aggressor cells to the V_T instabilities of their victim cells. Note, however, that this contribution cannot be just a conventional electrostatic interference in which charge detrapping in the aggressor cells modifies the floating-gate potential [14] or the channel potential [15] of the victim cell, as these effects should result in a ΔV_T contribution independent of the state of the victim cells. Figs. 2–5 reveal, in fact, that the BP sensitivity of the ΔV_T of the victim cells largely decreases moving these cells from level $L1$ to level $L3$. This effect can be explained only by saying that the same detrapped charge in the aggressor cells has a differ-ent impact on string current during read and, in turn, on the result-ing V_T of the victim cells depending on the memory state of the victim cells themselves. This means that the change of the memory state of the victim cells modifies the electron inversion and the current density profile along the NAND string during read.

3.2. TCAD simulations

In order to support the discussion of Section 3.1 with more quantitative analyses and to investigate in detail the role of detrapping in the victim and in the aggressor cells on the V_T instabilities of the victim cells, we performed 3-D numerical simulations of a template 20 nm NAND array. Fig. 8 shows the device structure simulated using a commercial device simulator [16] and consisting in a 3×3 NAND array with 20×20 nm^2 memory cells. For the sake of

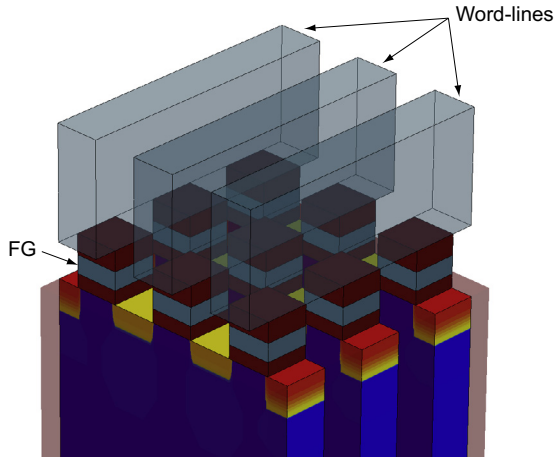

Fig. 8. Schematic structure of the 20 nm NAND array considered in Section 3.2 for numerical simulations of V_T instabilities as a function of the array BP.

simplicity and to give our results a more general validity, the simulated structure was not calibated on our 20 nm technology, being largely simplified with respect to it in terms of materials, geometry and doping profiles. With this in mind, SiO_2 was used for both the tunnel-oxide and the inter-gate dielectric, setting their thickness, respectively, to 6 and 9 nm. Aluminum was used for both the floating-gate and the word-line stripes, whose height was set to 8 and 50 nm. The current flowing through the central string was simulated by solving the coupled Poisson and drift–diffusion equations as a function of the bias applied to the central word-line, with the other word-lines biased at a pass voltage of 8 V and 0.3 V applied between the two lateral n^+ regions of the central string. The V_T of the cell in the center of the simulated array, considered as the victim cell in our analysis, was then defined as the bias of the central word-line allowing a string current of 100 nA. Simulations were performed with a different charge in the floating-gate of the victim and of the aggressor cells to reproduce their E, $L1$ and $L3$ state.

To investigate the ΔV_T coming from charge detrapping, the V_T of the victim cell was first calculated in the presence of electrons in the tunnel oxide of both the victim and the aggressor cells, aiming to reproduce a possible cell state after heavy program/erase cycling. Electrons were introduced as point charges in the simulated structure and distributed as shown in Fig. 9. In particular, 9 electrons were uniformly distributed over the channel area of the cells, with 3 additional electrons over the n junctions close to each

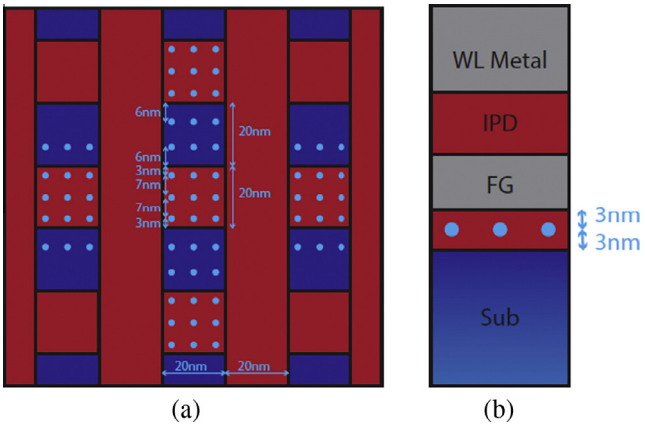

Fig. 9. Schematic drawing showing the position of the electrons put in the tunnel oxide of the victim and of the aggressor cells at the beginning of the detrapping simulations, on a planar (a) and vertical (b) cross section of the device.

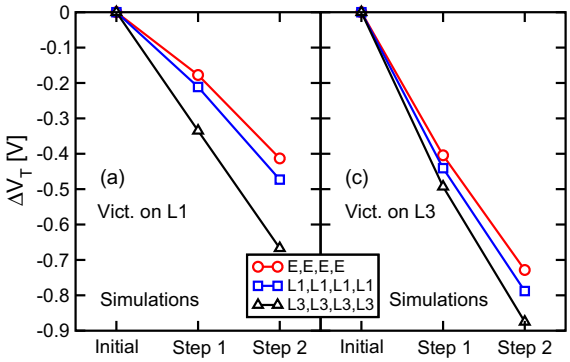

Fig. 10. Simulation results for ΔV_T as a function of the array BP, in the case where the victim cell is on level $L1$ (a) and on level $L3$ (b).

cell, as depicted in Fig. 9a. All the trapped electrons were placed halfway between the silicon substrate and the floating-gate (Fig. 9b), as typically reported from experimental analyses [3,2]. The V_T of the central cell was then simulated again after removing some of the trapped electrons to reproduce the detrapping process, calculating the resulting ΔV_T. To account for a field dependence of the detrapping process, a different number of electrons were removed from the tunnel oxide of the cells depending on their V_T level. In particular, at a first detrapping step (Step 1) we removed half of the electrons in the cells on level $L3$, one quarter of those in the cells on level $L1$ and none of those in the cells on the E level. At a second detrapping step (Step 2) we removed all the electrons in the cells on level $L3$, half of those on cells on level $L1$ and none of those in the cells on the E level.

Fig. 10 shows the simulation results obtained with the victim cell (a) on level $L1$ and (b) on level $L3$ and uniform patterns of the aggressor cells. Results appear in good qualitative agreement with the experimental data of Fig. 2, displaying a BP sensitivity that is relevant when the victim cell is on level $L1$ and smaller when the victim cell is on level $L3$. In addition, Figs. 11 and 12 show that numerical simulations correctly reproduce what experimentally observed in Figs. 4 and 5, *i.e.*, that the ΔV_T dependence on the array BP is mainly coming from a dependence of V_T instabilities in the victim cell on the state of its aggressor cells in the bit-line direction.

Given that our numerical simulations can correctly reproduce the qualitative trends of the experimental results of Section 2, we investigated more in detail the physical origin of the new cell-to-cell interference effect by looking at the electron concentration profile in the central string of the simulated array under read conditions, for different states of the victim and of the aggressor cells. Starting from the effect of the aggressor cells along the

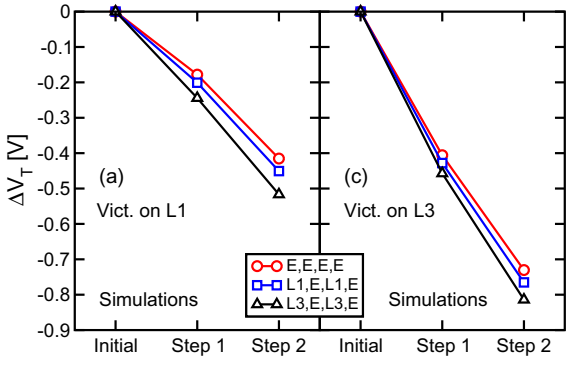

Fig. 11. Same as in Fig. 10, but for non-uniform BP with only the two aggressor cells along the bit-line direction on a programmed state.

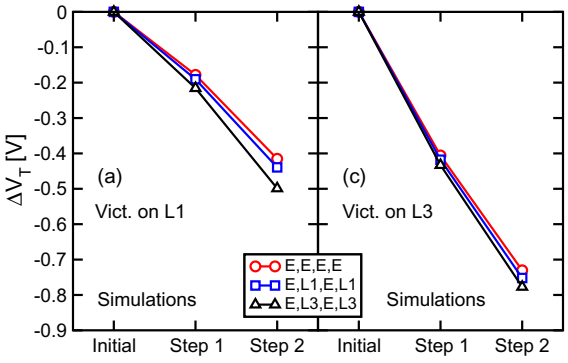

Fig. 12. Same as in Fig. 10, but for non-uniform BP with only the two aggressor cells along the word-line direction on a programmed state.

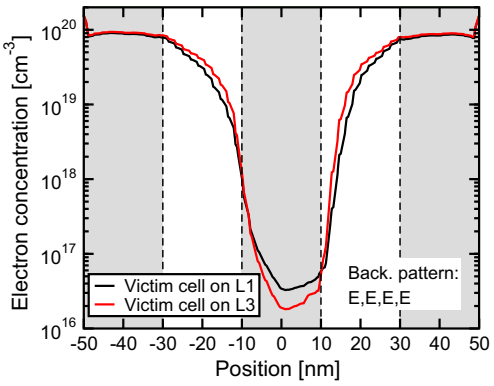

Fig. 14. Same as in Fig. 13, but for a E, E, E, E pattern of the aggressor cells.

bit-line direction, Fig. 13 shows that when these cells are on level $L3$ the inversion of their channel and of the n regions in-between them and the victim cell is weaker than when they are on level E, considered in Fig. 14. This means that when the top and bottom

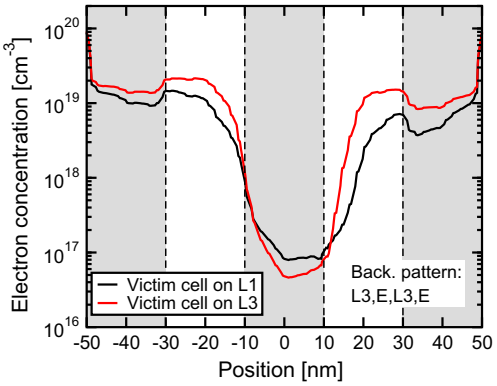

Fig. 13. Electron concentration profile along the central string of the simulated NAND array at threshold, when the victim cell is on level $L1$ and on level $L3$ and the pattern of the aggressor cells $L3, E, L3, E$. The shaded regions corresponds to the position of the floating-gate and of the word-lines of the array.

aggressor cells are on level $L3$ the detrapped charge from their tunnel oxide and from the oxide above the n regions adjacent to the victim cell has a higher impact on string current and, therefore, on the V_T resulting from a read operation on the victim cell than in the case of aggressor cells on level E. In addition to that, owing to the field dependence of the detrapping process, a lower amount of charge is detrapped from the aggressor cells when they are on a lower memory state. Both these effects contribute to making the ΔV_T observed on the victim cell higher when its aggressor cells along the bit-line direction are on level $L3$ than on level $L1$ or E, as appearing in Figs. 4–11. Moreover, Fig. 13 also shows that the state of the victim cell non-negligibly affects the electron concen-tration along the string. In particular, a weaker inversion of the aggressor cells and of the n regions appears when the victim cell is on level $L1$ than on level $L3$. This comes from the higher fringing fields of the central word-line in the latter case, owing to the higher voltage that must be applied to this stripe to reach the string current corresponding to the V_T condition. As a consequence, a stronger BP sensitivity results when the victim cell is on level $L1$ than on level $L3$, as shown in Figs. 4–11.

Finally, despite the dependence of the victim cell ΔV_T on the state of its aggressor cells along the word-line direction appears rather weak from Figs. 5–12, we investigated its physical origin by means of Fig. 15. Here the electron concentration under read

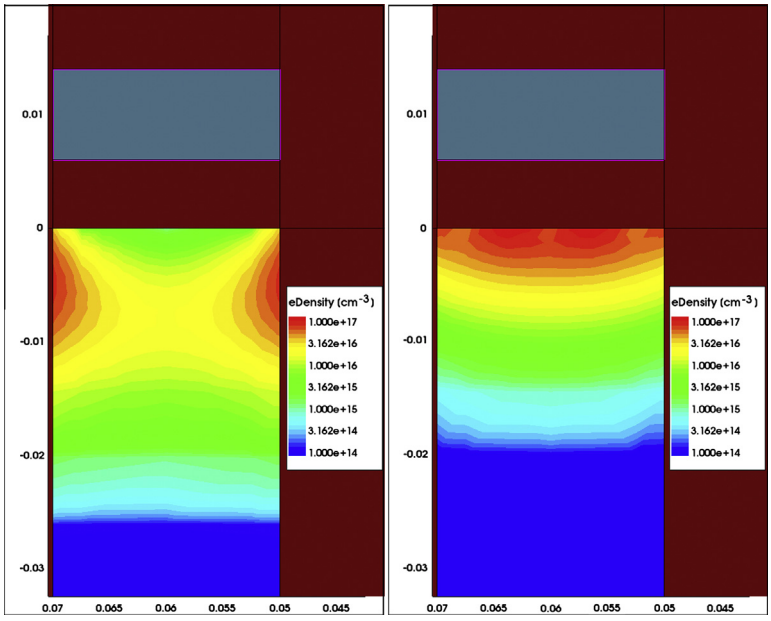

Fig. 15. Electron concentration at threshold in a vertical cross-section of the victim cell in the word-line direction, in the case the left and right aggressor cells are (a) on the E and (b) on the $L3$ level. The victim cell is on level $L1$.

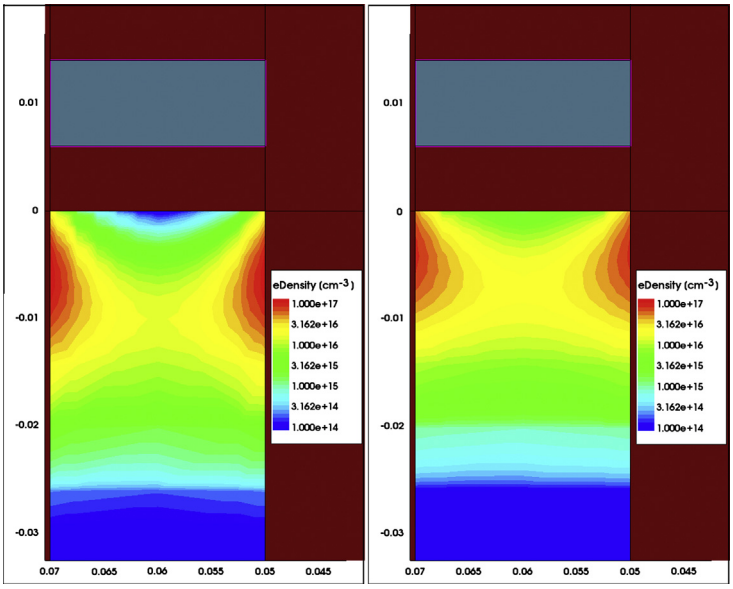

Fig. 16. Same as in Fig. 15 but with the victim cell on level $L3$.

conditions is reported in a vertical cross-section of the device along the word-line direction when the victim cell is on level $L1$ and its left and right aggressor cells are (a) on level E and (b) on level $L3$. Results reveal that when the left and right aggressor cells are on level E, the peak electron concentration is at the side of the cen-tral silicon string, while the peak is at the top of the active area in the case aggressor cells are on level $L3$. This results in a higher impact of the charge detrapped from the tunnel oxide of the victim cell in the latter case [17,18], explaining the BP sensitivity along the word-line direction when the victim cell is on level $L1$. Fig. 16 shows, instead, that the differences between the electron concentration profiles for different states of the aggressor cells in the word-line direction are much smaller in the case the victim cell is on level $L3$. This comes from the large amount of negative charge in the floating-gate of the victim cell in this case and results in a reduced BP sensitivity of the victim cells as observed in Figs. 5–12.

4. Conclusions

This paper showed that the post-cycling V_T instabilities of a (victim) cell in a nanoscale NAND Flash array depend not only on the cell memory state but also on the memory state of its adjacent (aggressor) cells. The magnitude of this effect was shown to decrease for higher V_T levels of the victim cell and to be mostly related to the interaction of the victim cell with its aggressor cells along the bit-line direction. A physical picture of the phenomenon is provided and supported with the help of 3-D numerical simulations.

Acknowledgements

The authors would like to thank F. Colombo from Politecnico di Milano and C. Miccoli, A. Goda, E. Camerlenghi and P. Cappelletti from Micron Technology Inc. for discussions and support.

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