Planar CMOS analog SiPMs: design, modeling and characterization

Yu Zou[a], Federica Villa[a], Danilo Bronzi[a], Simone Tisa[b], Alberto Tosi[a], Franco Zappa[a]

[a] *Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Piazza Leonardo Da Vinci 32, 20133 Milan, Italy;*
[b] *Micro Photon Device S.r.l., Via Stradivari 4, 39100, Bolzano, Italy*

Abstract— **Silicon photomultipliers (SiPMs) are large area detectors consisting of an array of single-photon-sensitive microcells, which make SiPMs extremely attractive to substitute the photomultiplier tubes in many applications. We present the design, fabrication, and characterization of analog SiPMs in standard planar 0.35 µm CMOS technology, with about 1 mm × 1 mm total area and different kinds of microcells, based on single-photon avalanche diodes with 30 µm diameter reaching 21.0% fill-factor (FF), 50 µm diameter (FF = 58.3%) or 50 µm square active area with rounded corner of 5 µm radius (FF = 73.7%). We also developed the electrical SPICE model for CMOS SiPMs. Our CMOS SiPMs have 25 V breakdown voltage, in line with most commercial SiPMs and higher gain (8.8 × 10^6, 13.2 × 10^6, and 15.0 × 10^6, respectively). Although dark count rate density is slightly higher than state-of-the-art analog SiPMs, the proposed standard CMOS processing opens the feasibility of integration with active electronics, for switching hot pixels off, drastically reducing the overall dark count rate, or for further on-chip processing.**

keywoards— **single-photon avalanche diode (SPAD); silicon photomultiplier (SiPM); single-photon sensitivity; photon counting; CMOS technology; SPICE modeling**

I. INTRODUCTION

A silicon photomultiplier (SiPM) is an array of single-photon detecting microcells, each consisting of a single-photon avalanche diode (SPAD) in series with a quenching element. With all microcells connected in parallel, SiPMs are able to provide an output proportional to the sum of independent firing microcells, thus proportional to the incident photon flux, and the sensitivity is down to the single-photon level for each microcell. Eventually, the multi-microcell structure of SiPM, firstly proposed in reference [1], essentially converts an intrinsically digital' (on/off) detector like SPAD [2] into an analog device with the ability to distinguish the number of impinging photons and to detect more than just one photon at a time.

The compactness and design flexibility of solid-state detectors make them easily adaptable to different applications by tailoring their layout, overall size, microcell size, and fill-factor (FF) to enhance the desired properties, such as photon detection efficiency (PDE), already larger than most photomultiplier tubes (PMTs) [3], or dynamic range. SiPMs are compatible to systems with static and dynamic magnetic fields and have been successfully applied, or tested in different applications, which can be divided into three groups: single-photon detection applications (e.g. fNiRS [4], Cherenkov detection[5]); photon-number resolved applications (e.g. quantum random number generators [6]); multi-photon detection applications (like positron emission tomography (PET) [7]and gamma imaging for proton therapy [8]).

Depending on the quenching element in each microcell and readout structure, we distinguish SiPMs as analog SiPMs and digital SiPMs. Digital SiPMs integrate active components inside each microcell. Each microcell provides its own digital output signal, while an on-chip or external counter sums all digital outputs from simultaneously triggered microcells [9]. With also on chip time-to-digital converter (TDC), digital SiPMs provide extremely good timing performance and have been tested for PET applications [10]. Analog SiPMs simply have SPAD and an integrated quenching resistor in each microcell providing an analog output proportional to the sum of independent firing microcells with high FF. Commercial analog SiPMs are developed in vertical custom technologies with p-on-n junction optimized for near ultraviolet light (e.g. SensL B-Series [11] and AdvanSiD NUV-SiPMs [12]) or n-on-p junction optimized for visible range light (e.g. SensL M-Series [13] and AdvanSiD RGB-SiPMs [14]); specially designed quenching resistors are integrated in order to keep high FF reported in [15]–[17]. Custom technologies are exploited in order to optimize the performance of SiPMs, in terms of dark count rate (DCR) and PDE, however, it doesn't allow the integration of complex electronics. High-performance SPADs in 0.35 µm CMOS technology have already been demonstrated in [18] [19]. We designed for the first time analog SiPM in standard 0.35 µm CMOS technology.

The reported good performance achieved open the way to the development of second-generation SiPMs through the integration of CMOS active electronics for on-chip readout and preprocessing. Whereas digital SiPMs designed in deeper CMOS technologies integrate active quenching circuitry in each microcell, the CMOS analog SiPMs that we propose have passive quenching in the microcell (as commercial analog SiPMs) not impairing the FF, and readout and preprocessing electronics on chip (as digital SiPMs), due to the fact that

standard 0.35 μm CMOS technology does not allow the same level of integration while keeping high FF.

This paper is organized as follows: Section 2 focuses on the structure of the planar CMOS SiPM; Section 3 presents the SPICE electrical modeling of such analog single-photon-sensitive detectors; Section 4 reports a detailed characterization of the developed SiPMs; eventually Section 5 draws conclusions.

II. DESIGN OF PLANAR CMOS ANALOG SiPMs

The developed SiPMs consist of four pixels with 8×8 SPADs each. All the 16×16 SPADs share a p-type substrate and common n-well, which forms the SiPM cathode, while each individual p+ anode is connected to its proper quenching resistor of about 264 kΩ. Due to the low resistivity value of polysilicon in standard CMOS technology, the quenching resistor occupies a larger area compared to custom technologies. In order to preserve the FF and the detection performance, we decided to lay out the resistors directly on the p-type substrate around the four edges of the array and not inside each microcell, as shown in Figure 1. We developed three different families of SiPMs: 30R-SiPM (30 μm diameter round SPADs), 50R-SiPM (50 μm diameter round SPADs), and 50S-SiPM (50 μm side square SPADs with 5 μm radius round corners). All families have same 58 μm pitch and 928×928 $μm^2$ total area, with different FFs of 21.0, 58.3, and 73.7%, respectively, comparable to commercial SiPMs whose FFs typically range from 28% [20] to 78% [21]. The FF is calculated by the active area uncovered by metal. Figure 1 shows the layout of 50R-SiPM and a simplified schematic of a generic SiPM. The SiPM cross section is shown in Figure 2: the p+ diffusion and the nwell define the avalanche region, while a p guard-ring avoids edge breakdown. Differently from custom technologies, in planar CMOS technology, SiPMs have cathode and anode contacts on the same side of the chip and there is also an additional substrate contact. The common cathode and the substrate are contacted only at the edge of the SiPM active area, to optimize FF, but introducing high parasitic resistance at the cathode. Furthermore, the presence of the substrate contact introduces two capacitances, i.e. cathode–substrate (C_{cs}) and anode metal–substrate (C_{ms}), as shown in Figure 2, that are instead not present in custom SiPMs. The junction capacitance C_d depends on the size of SPAD active area while Ccs depends only on the total SiPM area, hence it is the same for the three
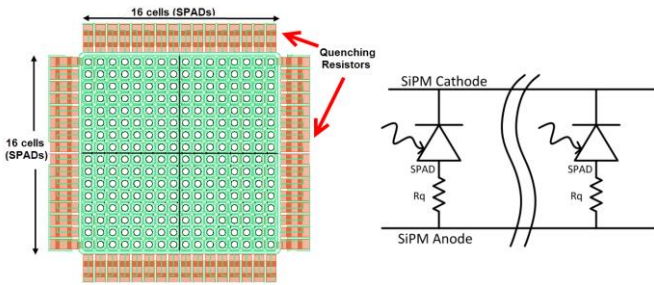

Fig. 2. Cross section of the planar CMOS SiPM, with quenching resistors and main parasitic capacitances.

produced SiPMs.

III. ELECTRICAL SPICE MODELING OF CMOS SiPMs

We developed the electrical SPICE model for planar CMOS SiPMs with all previously discussed parasitic elements. The single microcell model shown in Figure 3(a) was generated starting from the SPICE model of standard SPAD [22]. A fast 'Photon' pulse emulates the triggering photon by turning on the voltage-control switch $S_{TRIGGER}$, which mimics the avalanche ignition. Then the current-control switch S_{SELF} closes when the avalanche current exceeds a threshold (set to 70 μA), thus allowing current to keep flowing independent of the 'Photon' pulse, like the self-sustaining avalanche current through a SPAD. If the avalanche current becomes lower than a threshold level (set to 50 μA), the switch opens thus emulating the avalanche self-quenching, which happens when current gets too low (lower than 100 μA) that statistical fluctuation in impact ionization causes the multiplication to fail to self-sustain [2]. V_B is the SPAD breakdown voltage; R_d is the sum of the space-charge resistance and the resistance of neutral regions crossed by the avalanche current and R_Q is the quenching resistance of each SiPM microcell; C_Q is the parasitic capacitance in parallel to R_Q. When simulating the overall behavior of SiPM, the non-firing cells are simply replaced by the passive elements shown in Figure 3(b) since no avalanche current is triggered therein [23].

We used a 50R-SiPM and transimpedance amplifier shown in Figure 4 to verify the electrical SPICE model. The parameters of 50R-SiPM are extracted with Virtuoso RCX during its design ($C_d = 350$ fF, $C_{cs} = 45$ fF, $C_{ms} = 0.1$ fF, $R_Q = 264$ kΩ, and $C_Q = 2.5$ fF), and the breakdown voltage and the detector resistance are measured with an IV-meter ($V_B = 25$ V,

Fig. 1. (a) Layout of the 50R-SiPM with 16×16 SPADs and quenching resistors; (b) simplified structure of a generic SiPM, with many microcells made by a SPAD and a quenching resistor each; the cathodes and the anode common pad are the only two SiPM electrodes.
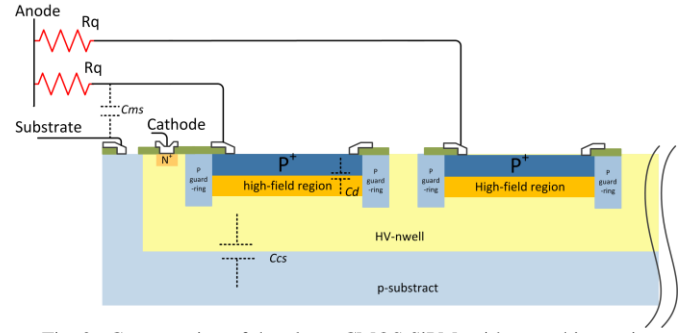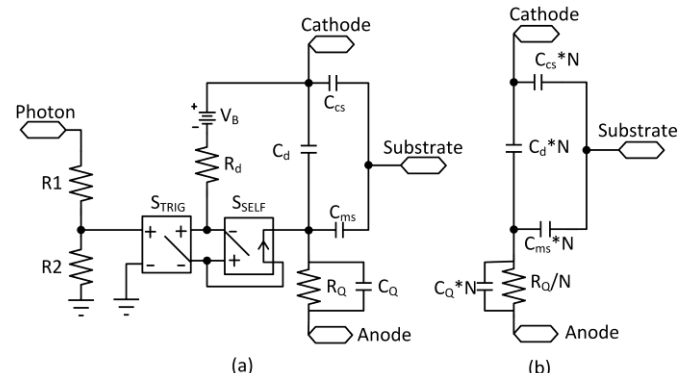

Fig. 3. SPICE modeling of the CMOS SiPMs: with (a) one firing microcell and (b) the equivalent model of the other N not triggered microcells.

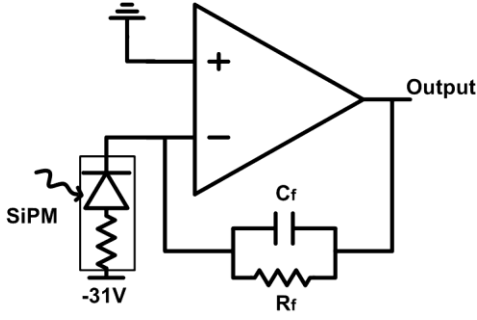Fig. 4. The transimpedance amplifier used for testing SiPMs.

Fig. 6. Comparison between measured results when readout is either from the cathode or from the anode of a 50R-SiPM.

R_d = 300 Ω). The circuit was compensated using feedback network composed by a resistor R_f of 2.2 kΩ and a capacitor C_f of 2.5 pF. In this case, the rising time of the output signal and its amplitude are affected by the bandwidth of the transimpedance systems. The falling edge has two different time constants: the first one is fast and it is determined by the R_d and the total capacitance at the anode; the second one is slower than the first one, is instead determined by the quenching resistance R_Q, C_d, C_{ms}, and C_Q. Figure 5 shows the agreement between simulated and measured results by readout from the cathode of 50R-SiPM. The first parts of falling edge are slightly different between simulation and measurement. This is because the Virtuoso RCX extractor is not very accurate and probably some stray capacitance have been under or over-estimated. As shown in Figure 6, the signals read from cathode and from anode differ due to the presence of substrate contact in standard CMOS technology. In fact, from anode, we read the current flow through R_Q and C_Q; while from cathode, we read the sum of current flow through R_Q, C_Q, and C_{ms}. Finally, the cathode is chosen as readout point to characterize the SiPMs, as they can provide higher signal amplitude verified in both simulation and real measurements.

This SPICE model could be used for simulate the behavior of SiPM with different quenching resistor values. By knowing the self-quench threshold value S_{SELF} (set to 50 μA), it is easy to find that 264 kΩ is sufficient to quench the avalanche even with 6 V of excess voltage [2]: $I_{steady} = V_{ex}/R_Q = 6$ V/264 kΩ = 22.7 μA which is smaller than the self-quench threshold.

If you are using *Word,* use either the Microsoft Equation Editor or the *MathType* add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.
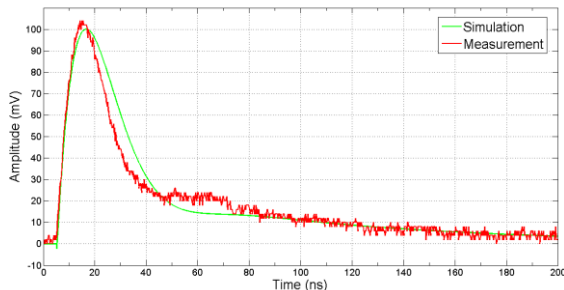
IV. CHARACTERIZATION

Fig. 5. Comparison between simulated and measured results, with readout from the cathode of a 50R-SiPM.
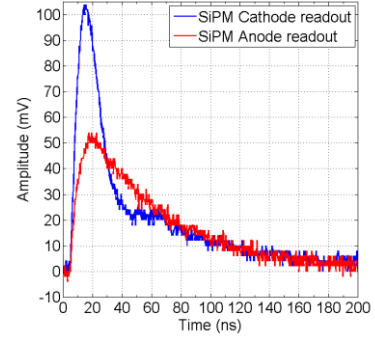
This section provides a detailed characterization of the fabricated CMOS SiPMs, along with the techniques we employed, and the analysis of obtained results.

A. Breakdown voltage (V_B)

The breakdown voltage of SiPMs is a superposition of the breakdown voltages of SPADs in each microcell and can be extracted from the current–voltage (I-V) characteristic curve. Figure 7 shows the I-V curve obtained by a programmable electrometer (Keithley 617). We measured a breakdown voltage of about 25 V with temperature coefficient of 30 mV/℃.

The breakdown voltage we obtained is comparable with most of commercial SiPMs, like Ketek PM1150 (25 V) [24], SensL C series (24.5 V) [25], AdvanSid ASD-NUV1S-P (26 V) [12], while it is much lower than Hamamatsu MPPC S12571–50 (65 V) [26] and Excelitas C30742–11 Series (95 V) [27]. The temperature coefficient is lower than the ones of Hamamatsu (60 mV/℃) and Excelitas (90 mV/℃), and slightly higher than SensL (21.5 mV/℃) and AdvanSid (26 mV/℃) ones.

B. Gain and photoelectron spectrum

Often users of PMTs talk about the photoelectron gain. In a similar way, for SiPMs it is possible to define the gain of a single microcell, determined by the charge derived from each single microcell when triggered by one photon. For our analog SiPM, when readout from the cathode with transimpedance amplifier, the gain can be computed as:
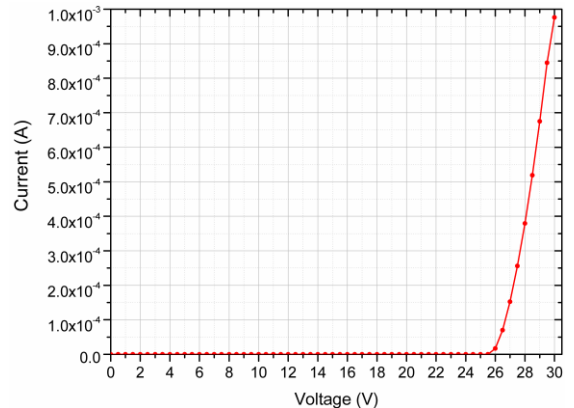

Fig. 7. I-V characteristic in low light condition taken by a programmable electrometer.
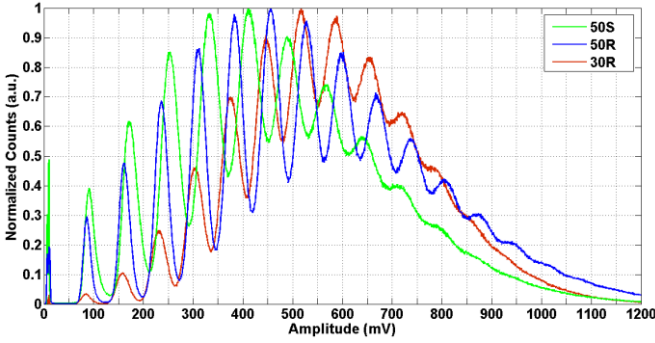
Fig. 8. Photoelectron spectrum of the three families of developed CMOS SiPMs, showing the actual ability to resolve multiple photons hitting the overall SiPM active area.

$$G = V_{ex} \cdot \frac{C_{tot}}{q} = V_{ex} \cdot \frac{(C_d + C_{ms} + C_Q)}{q} \qquad (1)$$

where V_{ex} is the excess bias above breakdown which the SiPM is operated at, C_d is the junction capacitance, C_{ms} is the capacitance between the SPAD's anode metal routing and the substrate, C_Q is the parasitic capacitance in parallel to quenching resistor, and q is the electron charge. All the parameters refer to the single microcell of the SiPM, shown in Figure 3(a). The higher the excess bias voltage and the microcell capacitance are, the higher the gain is.

The three SiPM families have different sizes and dimensions of SPADs, hence different capacitances C_d and different gains. We estimated the value of the C_{tot} capacitor by extracting information from layout, and we computed the gain by considering the applied excess voltage, using equation (1). At 6 V excess bias, the gains are 8.8×10^6 (for 30R-SiPM), 13.2×10^6 (for 50R-SiPM), and 15×10^6 (for 50S-SiPM). Comparing to $50 \times 50 \ \mu m^2$ microcell size commercial SiPMs, considering also the different excess voltages, our gain is still higher than most commercial SiPMs, except for SensL that reports a gain of 6×10^6 at just 2.5 V excess voltage. The higher gain should not be an advantage if considering the longer recovery time caused by the larger capacitance, while it could be an advantage for readout based on charge integration as it provides a larger signal.

Gain and photoelectron spectrum reflects directly the photon-counting properties of SiPMs. A clear photoelectron spectrum indicates low noise and uniform stable gain of
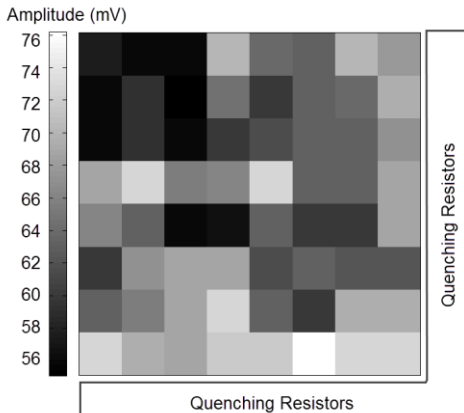
microcells. We obtained the photoelectron spectrum using a multichannel analyzer Varro Silena 16 k channels in gated mode (multichannel analyzer gate width typically about 400 ns) and a faint pulsed laser illumination with 80 ps FHWM at 683 nm and 1 MHz repetition rate. In gated mode, the number of simultaneous firing microcells can be measured with minimal interference from dark pulses, and with faint illumination in each gate window the SiPM is not saturated (i.e. the number of incoming photons is much smaller than the number of microcells).

The photoelectron spectrum of the three families of SiPMs (30R-SiPM, 50R-SiPM, and 50S-SiPM) is shown in Figure 8: up to 15 simultaneous photons can be distinguished. The first peak in the spectrum, often called the pedestal, records the electronic noise in the system with no detected photon. The second peak in the spectrum is the first photoelectron peak and corresponds to a single microcell triggered during the gate-on. Subsequent peaks correspond to two, three, four, and more microcells fired simultaneously during the gate-on. The peaks of the spectrum are well resolved; this demonstrates the good photon counting properties of our CMOS SiPMs. Looking at the first photoelectron peak, the peak of 30R-SiPM (red line) is centered at a lower voltage amplitude than the 50R-SiPM (blue line) and the 50S-SiPM (green line): such a difference is related to the different SiPM gains. The peak-to-valley ratio decreased while increasing the number of instantaneously firing microcells, caused by the non-uniform gain of microcells. To better understand this phenomenon, we plotted the amplitude map of 50S-SiPM. The same laser diode has been focalized in each microcell of a 50S-SiPM. A multichannel analyzer is used to acquire the peak amplitude of each microcell in which the laser is appropriately focalized. Figure 9 shows the amplitude map from one corner of 50S-SiPM. The signals coming from microcells located near the edge have amplitudes higher than the ones in the central zone. This aspect enlarges the standard deviation of peaks in the photoelectron spectrum. This can be explained by the layout of common cathode contact, substrate contact, and quenching resistors: the microcells located near the edge have lower parasitic capacitance and resistance while the ones in the center have larger parasitic values. Better layout will be considered for the second generation of analog SiPMs. The corresponding amplitude (mV) of the peaks in the photoelectron spectrum grows perfectly linear with the number

Fig. 9. Amplitude map obtained by using the laser beam focalized in each microcell of 50S-SiPM. Only one corner of 50S-SiPM is shown.
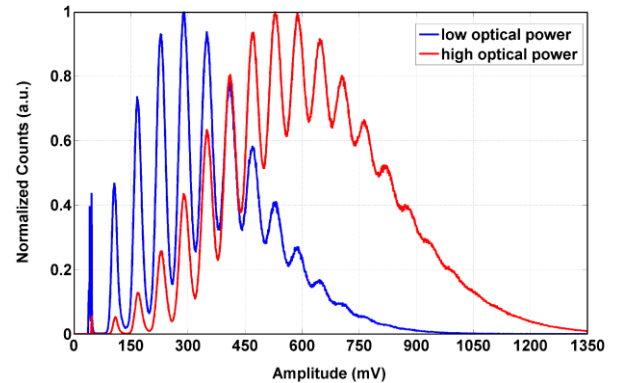

Fig. 11. Photoelectron spectrums of a 50S-SiPM obtained with two different optical powers (i.e. photon fluxes). The shift toward higher peak amplitudes and the presence of more peaks of the red curve is a clear indication of the higher number of photons hitting the SiPM active area.
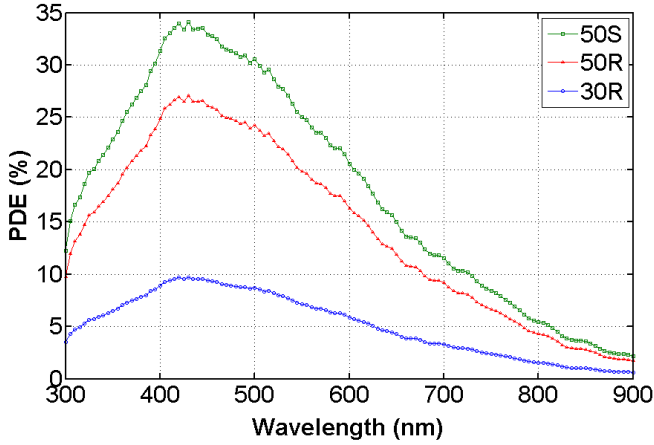
Fig. 12. Effective PDE of the three CMOS SiPM families, measured at 6 V excess bias, including the actual FFs while excluding any crosstalk and afterpulsing contribution.

of simultaneous firing microcells, as shown in Figure 10: from the fitting, the amplitude of a single firing microcell contribution is 78 mV. By increasing the illumination power, a higher number of peaks become visible toward the right-hand side of the spectrum, indicating an average higher number of photons hitting the SiPM, as shown in Figure 11.

C. Photon detection efficiency

The PDE of a SiPM is the ratio between the number of detected photons and the number of photons that reached SiPM itself. It is important to measure the effective PDE and to exclude crosstalk and afterpulsing contributions [28], which will cause an overestimation of detection efficiency. To this aim, we measured the PDE of single SPADs with the same dimension and shape of those integrated into the SiPM microcells and placed on the same silicon wafer. Then the effective PDE of SiPM can be directly computed by multiplying that PDE by the SiPM FF:

$$PDE_{SiPM} = PDE_{SPAD} \times FF \qquad (2)$$

We measured the PDE of the three families of SPADs at 6 V excess bias, from 300 nm to 1100 nm wavelength, using the same optical setup presented in [18]. Figure 12 shows the resulting PDE of the three SiPMs. The PDE peaks are 10% (30R-SiPM), 27% (50R-SiPM), and 34% (50S-SiPM), respectively, but always at about 420 nm wavelength, as shown in Figure 12.

D. Dark count rate

The dark count rate, i.e. the rate of ignitions of a SiPM not due to useful photons, is the contribution from all microcells, including those hot pixels giving the highest contributions. The DCR sets the minimum distinguishable signal level; hence, the signal-to-noise ratio in single-photon or photon-number resolved acquisitions. We acquired the DCR from the three families in a dark environment, at 6 V excess bias, and with a transimpedance amplifier readout from the cathode, as shown in Figure 4. The output of the readout circuit is fed to a digital counter with programmable discriminator threshold. By setting the threshold at the single-photon level, we measured an average DCR of 117 kcps (30R-SiPM), 334 kcps (50R-SiPM), and 503 kcps (50S-SiPM). Instead, Figure 13 shows the count rate at different threshold levels in the dark condition: with a
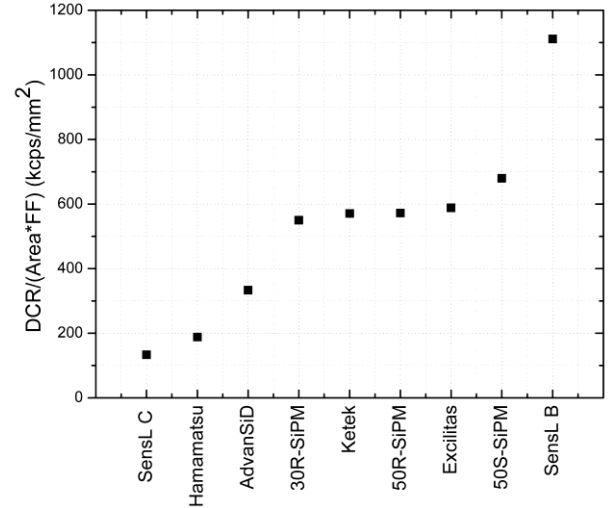

Fig. 14. Comparison of dark counting date density, i.e. referred to unit active area, among our standard CMOS SiPMs and commercial custom SiPMs reported in [11,12,24–27].

threshold higher than 10-photon level, the noise rate is negligible. This parameter can be important for applications that imply the use of the SiPMs to detect the arrival of a given number N of simultaneous hitting photons.

The DCR of SiPMs depends on processing quality and also on layout (e.g. active area's dimension and shape of each microcell). In order to have a fair comparison among the quality of the different manufacturing processes, we use the DCR density, which is defined by DCR per effective active area, i.e.:

$$DCR_{density} = DCR/SensorArea \times FF \qquad (3)$$

Figure 14 shows that our SiPMs provide a DCR density slightly higher than state-of-art commercial SiPMs, notwithstanding our processing was standard CMOS, while DCR is still aligned with Ketek one [24] and Excelitas one [27], and much lower than SensL B series one [11]. All the DCR density values are calculated by considering geometry factor of SiPMs at their typical working condition (therefore different V_{ex} for different SiPMs).

E. Crosstalk

Since SiPMs are based on a large number of neighboring microcells, with large detection area and high FF, both optical and electrical crosstalk can be an issue. We exploited the same setup used for DCR to measure the overall crosstalk. The crosstalk probability can be computed as:

$$X_{talk} = DCR_{2p}/DCR_{1p} \qquad (2)$$

where DCR_{2p} and DCR_{1p} are the noise rates measured with the discriminator threshold set at 1.5 photons level amplitude and at 0.5 photon level amplitude, respectively. This method relies on the assumption that the probability of two uncorrelated avalanche events, triggered within the same avalanche rise time is negligible. We obtain 18.6% (30R-SiPM), 23.0% (50R-SiPM), and 33.5% (50S-SiPM) crosstalk probability, respectively. These values are comparable to those of commercial SiPMs with similar FF and the same no-trench structure. The adoption of deep trench isolation can decrease
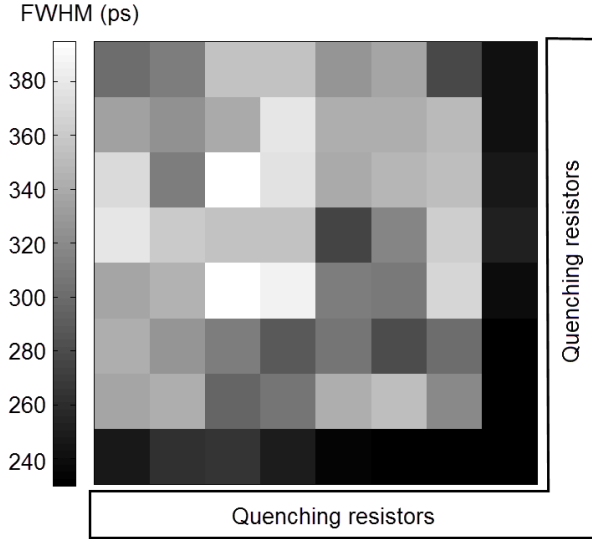
FWHM (ps)

Fig. 15. FWHM map obtained by focalized timing of 30R-SiPM, shown only one corner of 30R-SiPM.

optical crosstalk probability: in fact the commercial Ketek PM1150T SiPMs with trenches have just a 15% crosstalk probability with 63% FF, while for the PM1150NT without trenches the crosstalk becomes 35% with 70% FF.

F. Timing

The time precision, or photon-timing jitter, is an important parameter of single-photon detectors like SiPM in the identification of the photon arrival time. Usually it is measured in terms of Full-Width at Half Maximum (FWHM) of the distribution of arrival times to a repetitive collection of periodic fast laser pulses. FWHM can be measured by means of the time correlated single photon counting (TCSPC) technique [29]. One input of the TCSPC (either Start or Stop) will be pulse signals generated by SiPM, while the other one is a synchronization signal from the laser pulses used to trigger the SiPM. After accumulating a sufficient number of photon events, a histogram of the time delay between two input signals can be build, and its FWHM represents the timing performance. Less than one photon on average must be detected by the SPAD for each laser pulse in order to reconstruct the timing waveform with no distortion. We characterized the photon timing responses by means of TCSPC technique, through the pulse signals generated by SiPM, while the other one is a

TABLE I: Performances of the CMOS SiPMs presented in this work, operated at 6 V excess bias.

	30R-SiPM	50R-SiPM	50S-SiPM	unit
Fill-factor	21	58.3	73.7	%
Gain	8.8×10^6	13.2×10^6	15×10^6	a.u.
Peak PDE	10	27	34	%
DCR (T=25 ℃)	117	334	503	kcps
Crosstalk	18.6	23	33.5	%

synchronization signal from the laser pulses used to trigger the SiPM. After accumulating a sufficient number of photon events, a histogram of the time delay between two input signals can be build, and its FWHM represents the timing performance. Less than one photon on average must be detected by the SPAD for each laser pulse in order to reconstruct the timing waveform with no distortion. We characterized the photon timing responses by means of TCSPC technique, through the SPC-130 timing board by Becker & Hickl. The SiPM has been tested with a pulsed diode laser (λ = 683 nm, 80 ps FWHM) using repetition rate of 5 MHz with 6 V excess voltage. Figure 15 depicts the map of the FWHM of timing responses coming from 8×8 microcells of 30R-SiPM on which the laser has been focalized on the SPAD of each microcell. The FWHM from edge (closer to resistor) to center (far away from resistors), ranges from 240 to 340 ps. The lengths of metal line connecting the SPAD to its quenching resistor are different according to the microcell position in the array and the connections of cathode are only on the four sides of the array, thus strongly influencing the timing performance by introducing different parasitic resistance and capacitance seen by each microcell. For these pixels, the absence of a clear trend is caused by the different values of quenching and internal resistance of the SPADs due to their tolerances.

V. Conclusion

We reported the design, development, and characterization of novel analog SiPMs fabricated in a fully standard planar 0.35 μm CMOS technology. Table 1 summarizes the performance of the developed three families of SiPMs (30R, 50R, and 50S). Instead, Table 2 compares the performance of these CMOS SiPMs with other commercial custom technology SiPMs. The performance in terms of FF, peak PDE, and crosstalk

TABLE II: Performance comparisons of the CMOS SiPMs presented in this work (50R-SiPM) with commercial ones fabricated in custom technologies.

	Microcell size (μm^2)	Number of microcells	FF	V_B(V)	Gain	Peak PDE	DCR (kcps)	Crosstalk probability (%)
This work	58×58	256	58.3%	25	13.2×10^6	27% (420nm)	334	23
[26]	50×50	400	62%	65	1.25×10^6	35% (450nm)	100	35
[24]	50×50	576	70%	25	1.7×10^6	>50% (420nm)	400	35
[25]	50×50	324	72%	24.6	6×10^6	47% (420nm)	96	10
[11]	50×50	324	72%	24.5	6×10^6	47% (420nm)	800	10
[27]	50×50	400	51%	95	1.5×10^6	33% (520nm)	300	-
[12]	40×40	625	60%	26	2.1×10^6	32.5% (420nm)	200	-

probability are comparable to those of best-in-class commercial SiPMs. Only the DCR density is slightly higher than the best ones, but still aligned to Ketek [24] and Excelitas [27] and well lower than SensL B series [11].

This work on the fabrication of analog SiPMs in standard CMOS technology opens the way to the development of more advanced analog SiPMs, with on-chip readout and pre-processing electronics.

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