Modeling of Dynamic Operation of T-RAM Cells

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I. Introduction

THE T-RAM cell represents a promising memory solution for next generation DRAM devices [1]–[5]. The structure of this cell is that of a physical nanoscale thyristor with a gated p-base, whose bistability is exploited to reach, with the same voltage waveforms applied to its contacts, either of two stable states. Thanks to the orders-of-magnitude gap between the current of these states, T-RAM devices offer not only the possibility of a simple process flow but also of very fast read operations, comparable with conventional 1-transistor–1-capacitor DRAM cells.

Leading the T-RAM cell to either of its two stable states with the same reading waveforms is achieved by exploiting early device turn-ON when the gate voltage (V_G) undergoes a fast low-to-high switch. The first rough explanation of the phenomenon was given in [6]: a fast increase in V_G (starting from an initial value V_{GL} negative enough to keep the p-base under hole accumulation) prevents a significant hole discharge of the p-base, then making the potential of this region during the V_G ramp higher than that corresponding to static conditions. This, in turn, results in a higher electron flow from the cathode to the n-base and, therefore, in the possibility of turning the device ON with a lower anode voltage (V_A). The possibility of achieving early turn-ON can be precluded if holes are removed from the p-base prior to cell sensing, for instance, by applying a positive gate pulse with grounded anode. From this discussion, it appears clearly evident that the hole concentration in the p-base represents the physical parameter allowing information storage in the device: the presence of holes in the p-base (state 1) is detected as a high current during read, while a depleted p-base (state 0) results only in a low read current [7].

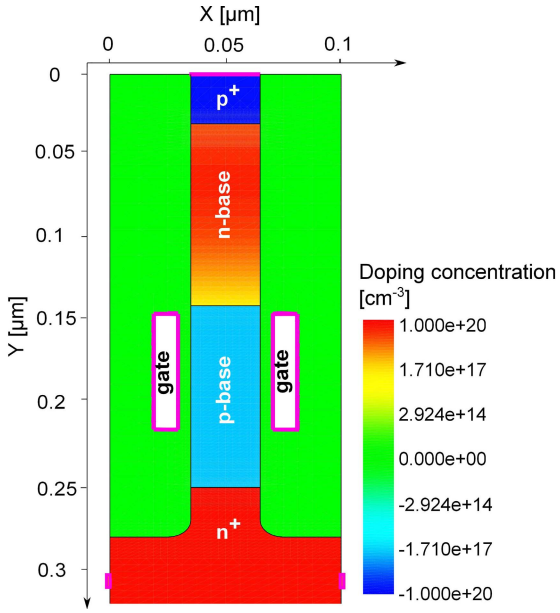

Fig. 1. Structure of the T-RAM cell investigated in this paper.

In this paper, we present a detailed numerical analysis of the dynamic operation of T-RAM cells, focusing on electrostatics and on carrier concentrations and flows in the device during a fast low-to-high switch of V_G. This analysis allows us to investigate both early device turn-ON, i.e., cell read, and the write operations required to modify the cell state. The results provide a comprehensive understanding of the basic physics of T-RAM cells and represent an important step to clearly identify technology performance and prospects.

II. Numerical Model

Fig. 1 shows the template device structure we adopted for our numerical investigation of the dynamic operation of T-RAM cells. The structure is very similar to that originally

Manuscript received January 21, 2015; revised March 12, 2015; accepted April 5, 2015. Date of publication May 1, 2015; date of current version May 18, 2015. The review of this paper was arranged by Editor Y.-H. Shih.

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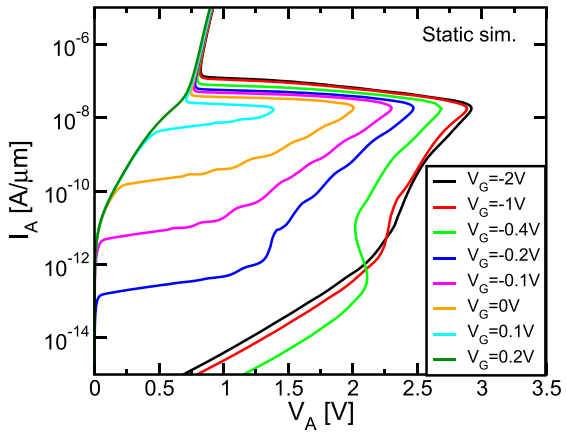

Fig. 2. Simulation results for the static I_A–V_A curve of the T-RAM cell shown in Fig. 1, for different V_G.

proposed in [1], presenting a vertical silicon pillar with a p^+-n-p-n^+ doping sequence. The p^+ and n^+ regions represent the anode and the cathode of the device, while the intermediate n and p regions are the thyristor n-base and p-base. A double metal gate is capacitively coupled to the p-base region through a 5-nm oxide layer. The height of the n-base and p-base regions is 100 nm, and the width of the pillar is 30 nm.

2-D numerical simulations on the template cell structure of Fig. 1 were performed by means of a commercial device simulator [8]. The Poisson and the continuity equations for electrons and holes were solved including carrier drift and diffusion, generation/recombination according to the Shockley–Read–Hall theory, band-to-band tunneling, trap-assisted tunneling, and avalanche multiplication. In order to show that our numerical simulation setup allows the correct reproduction of the main electrical characteristics of T-RAM cells, we first solved the Poisson and continuity equations in the static, i.e., time independent, case. Fig. 2 shows the anode current versus anode voltage (I_A–V_A) curve resulting in this case for different V_G ranging from -2 to $+0.2$ V. The results reproduce the main features observed on experimental samples, including the trend of the forward breakover voltage (V_{FB}) with V_G [1], [9], [10]. In particular, V_{FB} shows an abrupt decrease with V_G when the cathode-to-n-base electron flow given by the weak inversion of the p-base surface becomes relevant [1].

To further check the possibility of reproducing the basic features of T-RAM cell operation with our numerical simulation setup, Fig. 3(b) shows the results of time-dependent numerical simulations implementing the V_A and V_G waveforms reported in Fig. 3(a). These waveforms are those used to sense I_A during read operations [7] and involve raising first V_A and then V_G from their idle values $V_{AL} = 0$ V and $V_{GL} = -2$ V to their read values V_{AH} (changed as a parameter in the simulations) and $V_{GH} = 0$ V. Fig. 3(b) shows the simulated I_A versus V_{AH} curve for different rise times t_r of the V_G pulse (the rise front of the V_A pulse was set to 50 ns). In the case of long t_r, the entire curve and, in turn, the V_{AH} value required for cell turn-ON coincide with static

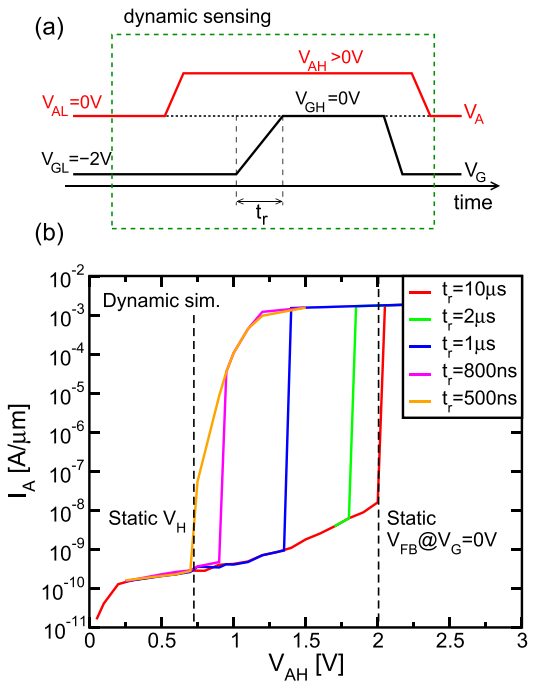

Fig. 3. (a) V_A and V_G waveforms applied for dynamic sensing of I_A (read operation). (b) Simulated I_A versus V_{AH} curve for different rise times t_r of the V_G pulse.

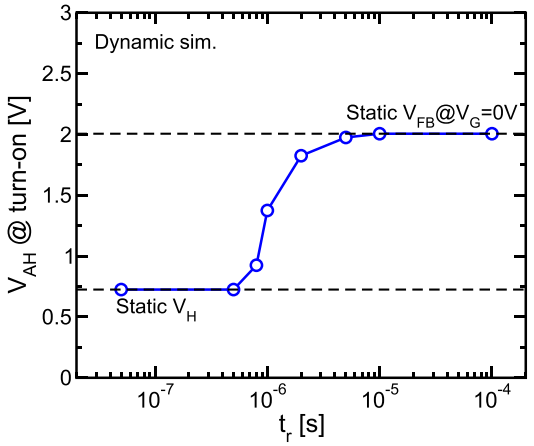

Fig. 4. Simulation results for the V_{AH} leading to cell turn-ON when applying the voltage waveforms of Fig. 3(a), as a function of t_r.

results at $V_G = V_{GH}$. However, in agreement with what experimentally shown in [6] and [7], early device turn-ON appears for short t_r, with the possibility of leading the cell to its high current state at the static hold voltage V_H. Fig. 4 shows that the transition of the V_{AH} allowing cell turn-ON from the static V_{FB} to V_H takes place when t_r decreases below a few microseconds, in agreement with what first reported in [6].

III. Investigation of Early Cell Turn-ON

The possibility for early turn-ON of the T-RAM cell after the application of a fast low-to-high V_G switch represents perhaps the most relevant phenomenon for the operation of the device as a DRAM cell [7]. Early device turn-ON relies, in fact, on the presence of a high hole concentration in the p-base [6]

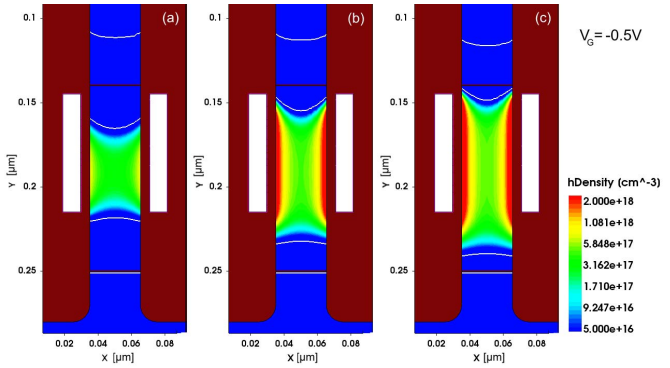

Fig. 5. Simulated hole concentration in the cell p-base (a) under stationary conditions and during dynamic sensing of the cell with (b) $t_r = 100$ μs and (c) 500 ns. $V_A = 1.5$ V and $V_G = -0.5$ V.

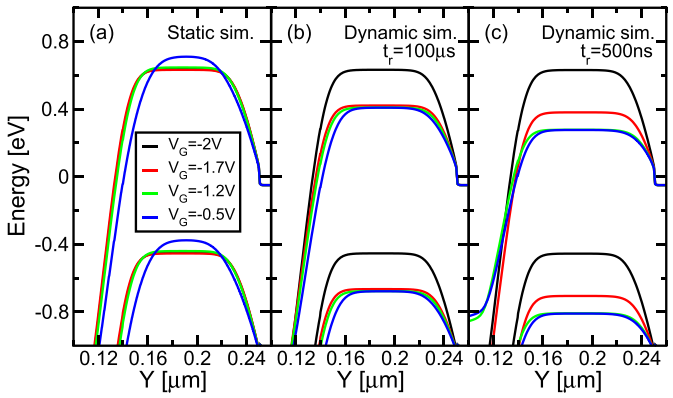

Fig. 6. Vertical cut of the band profile along the center of the p-base under (a) stationary conditions and during dynamic sensing of the cell with (b) $t_r = 100$ μs and (c) 500 ns, for different V_G and $V_A = 1.5$ V.

and is precluded if holes are removed from the p-base prior to cell read [7]. This, in turn, makes hole concentration in the p-base the parameter allowing volatile information storage in the T-RAM cell. In the following sections, the basic physics leading to early cell turn-ON will be investigated in detail.

A. p-Base Electrostatics

As a first step to understand the basic physics leading to early turn-ON of the T-RAM cell, we verified the hypothesis that a high hole concentration remains in the p-base when the front of the V_G pulse in Fig. 3(a) is quick. To this aim, Fig. 5(a)–(c) shows the hole density in the p-base when $V_G = -0.5$ V is applied ($V_A = 1.5$ V) in stationary conditions and during V_G rise with $t_r = 100$ μs and 500 ns ($V_{GL} = -2$ V and $V_{GH} = 0$ V were used for all the reported simulation results). The results clearly confirm that the dynamic low-to-high transition of V_G allows to keep a higher hole concentration in the p-base with respect to the static case, with differences growing with the reduction of t_r. As a consequence of this, the p-base reaches a higher electrostatic potential during dynamic cell operation, as appearing from Fig. 6. In Fig. 6(a)–(c), the band diagram along the center of the p-base is reported for V_G values between $V_{GL} = -2$ and -0.5 V, in the case of static and dynamic simulations.

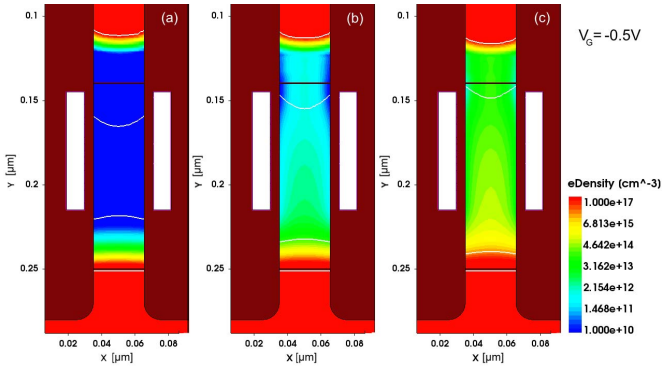

Fig. 7. Same as in Fig. 5, but for the electron concentration.

The results reveal that the increase of V_G in the selected range gives rise to a relevant downward shift of the band diagram in the latter case, while only small variations of the band profile appear in the former case. Moreover, Fig. 6 highlights that in the case of dynamic cell operation, the electrostatic potential in the p-base reaches a stationary level during the V_G ramp, which increases for shorter t_r [compare Fig. 6(b) and (c)].

In order to understand the evolution of p-base electrostatics during the low-to-high V_G transition used for dynamic read operations, Fig. 7 shows that, although the higher p-base potential leads to a higher electron concentration for shorter t_r, electrons remain minority carriers in the p-base along the entire V_G ramp. This means that electrons do not impact p-base electrostatics, which, in turn, is affected only by V_G and the hole concentration. Considering that the V_G ramp takes the p-base into a nonequilibrium condition triggering hole discharge, the time dynamics of the p-base potential (V_3) can be described by the following equation:

$$\frac{dV_3}{dt} = \frac{dV_G}{dt} \cdot \frac{C_G}{C_{\text{tot}}} - \frac{I_{p3}}{C_{\text{tot}}} \tag{1}$$

where C_G and C_{tot} are, respectively, the gate to p-base capacitance and the total p-base capacitance, and I_{p3} is the hole current leaving the undepleted region of the p-base toward the cathode. V_3 represents the p-base potential with respect to the cathode, which, until a significant depletion of the p-base is reached, almost equals the separation between the quasi-Fermi level for holes in the p-base and for electrons in the cathode. The second member of (1) highlights the two opposite terms impacting the p-base potential, namely, the increase of V_G and hole discharge. The increase of V_G is initially dominant and leads to the growth of V_3, but this growth increases I_{p3} up to the point where the two terms on the right-hand side of (1) are equal. When this happens, the p-base potential reaches a stationary condition, with V_3 remaining almost constant and equal to the value V_3^* leading to the hole current I_{p3}^*

$$I_{p3}^* = C_G \cdot \frac{V_{GH} - V_{GL}}{t_r}. \tag{2}$$

In (2), an inverse proportionality of I_{p3}^* on t_r appears, meaning that faster V_G ramps allow to reach higher hole currents discharging the p-base. Owing to the exponential dependence of I_{p3} on V_3, (2) results in a logarithmic dependence of V_3^* on t_r, as shown in Fig. 8. The results in Fig. 8 are shown

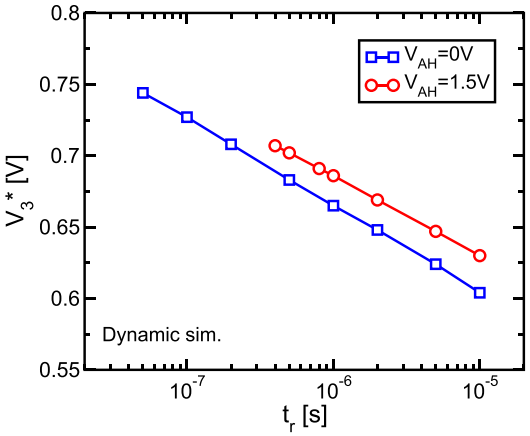

Fig. 8. V_3^* reached during the low-to-high V_G transition from $V_{GL} = -2$ V to $V_{GH} = 0$ V, as a function of t_r. The results for $V_{AH} = 1.5$ and 0 V are shown.

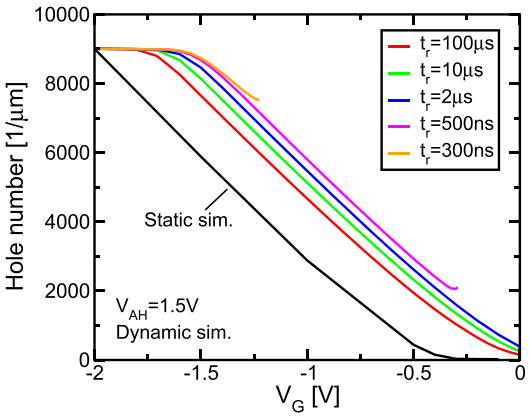

Fig. 9. Simulated number of holes in the p-base during dynamic sensing with different t_r (the results are shown up to cell turn-ON). The curve from static simulations is also shown.

both in the case of $V_A = 1.5$ V, allowing the investigation of the dynamic read conditions of Fig. 3(a) and of write-1, and in the case of $V_A = 0$ V, allowing the investigation of write-0 operations [7]. Note that, on account of the reverse bias of the n-base/p-base junction, in the former case hole discharge takes place only toward the cathode and requires, therefore, a higher V_3^* than in the latter case, where the hole flow is shared between the n-base and the cathode directions.

Fig. 9 shows the evolution of the number of holes in the p-base as a function of V_G. The results reveal that the hole number remains nearly constant up to a V_G value V_G^* depending on t_r, and then decreases almost linearly until significant depletion is achieved. This behavior can be explained considering that for $V_3 < V_3^*$, i.e., $V_G < V_G^*$, the hole current is exponentially lower than I_{p3}^* and, therefore, has a negligible impact on both hole number and p-base electrostatics. Once the stationary hole current I_{p3}^* is reached, instead, a constant-current discharge of the p-base starts to take place, until this region approaches depletion. From this standpoint, the slight leftward shift of the curves in Fig. 9 appearing when longer t_r are considered is the direct result of the lower V_3^* required to reach the stationary p-base electrostatics. This shift leads to a higher hole concentration in the p-base when the same

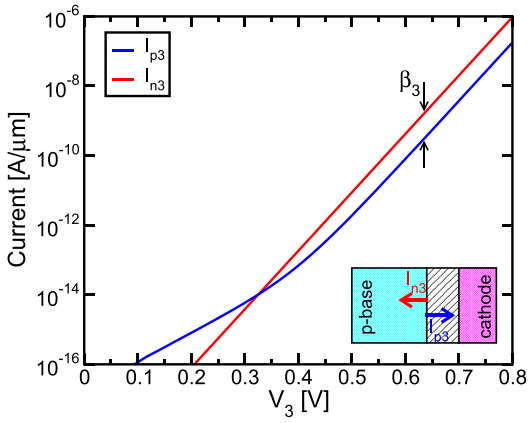

Fig. 10. Current components through the p-base/cathode junction as obtained from static simulations. Inset: schematics for the definition of I_{n3} and I_{p3} (the dashed region represents the junction depletion layer).

V_G is reached with shorter t_r (see also Fig. 5), thanks to a lower outflow of holes from the p-base in the stretch of time required to reach the selected V_G value. Besides, note that the leftward shift of the curves in Fig. 9 for longer t_r results only in a weak increase in the V_G required to deplete the p-base of holes when shorter t_r values are considered. Since this V_G is nearly equal to 0 V from Fig. 9, this means that quite fast write-0 operations can be achieved on T-RAM cells, provided that the anode is grounded and V_G is raised above 0 V.

B. Charging of the n-Base

The increase of the p-base potential following the low-to-high V_G switch gives rise to an exponential increase in the electron current I_{n3} that from the cathode reaches first the p-base and then the n-base. Fig. 10 shows the simulated I_{n3} and I_{p3} taken as shown in the inset, i.e., at the edge of the undepleted region of the p-base toward the cathode. On account of this definition of I_{n3} and I_{p3}, the contribution to current given by electron/hole recombination in the junction depletion layer appears only in I_{p3}, while I_{n3} displays a purely exponential behavior. Note, however, that, thanks to the relatively low doping of the p-base, this contribution is completely negligible for I_{p3}^* values above $\simeq 10^{-13}$ A/μm, corresponding to t_r below 10 ms. This means that the current gain $\beta_3 = I_{n3}/I_{p3}$ of the p-base/cathode junction during the V_G transition leading to early cell turn-ON can be set to a constant equal to the ratio between the electron and the hole current flows coming from Shockley's ideal diode equation (nearly equal to $\beta_3 = 5.4$ from Fig. 10).

Thanks to the narrow width of the p-base, almost all of the electrons injected from the cathode cross this region and enter the n-base. Here electrons are integrated during the V_G transition, lowering the n-base potential and forward biasing the n-base/anode junction, as appearing from the band diagrams reported in Fig. 11. The forward bias V_1 of the n-base/anode junction results in the increase of the electron current I_{n1} leaving the n-base toward the anode and of the hole current I_{p1} injected from the anode to the n-base. These two currents, calculated at the left edge of the undepleted region of the n-base, are shown in Fig. 12.

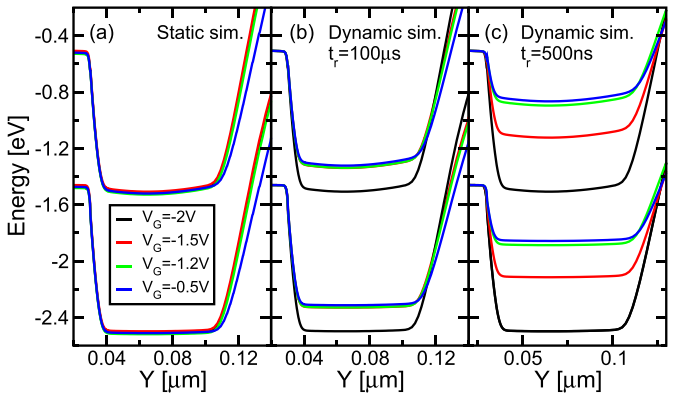

Fig. 11. Same as in Fig. 6, but along the n-base.

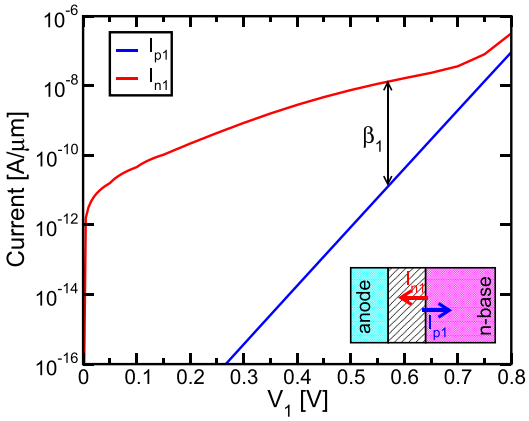

Fig. 12. Current components through the n-base/anode junction as obtained from static simulations. Inset: schematics for the definition of I_{n1} and I_{p1} (the dashed region represents the junction depletion layer).

The convention used in the definition of I_{n1} and I_{p1} makes carrier recombination in the junction depletion layer appear in the electron and not in the hole current component. The results reveal that this recombination contribution is far larger than that in the p-base/cathode junction, owing to the high doping concentration of both the anode and the n-base region. As a consequence of this, the n-base/anode junction can be considered a sink for the electron flow leaving the n-base until cell turn-ON occurs. This, in turn, validates the possibility of investigating p-base electrostatics neglecting the presence of the anode and of the holes coming from it, as done in Section III-A.

C. Cell Turn-ON

Early turn-ON of the T-RAM cell relies on the possibility of achieving a high enough forward bias of the n-base/anode junction during the low-to-high V_G switch as a result of the integration of the electron flow coming from the cathode through the p-base. The increase in the forward bias of the n-base/anode junction leads, in fact, to the increase in the current gain $\beta_1 = I_{p1}/I_{n1}$ of this junction (Fig. 12) and, in turn, to the increase in the positive feedback in the $p^+ - n - p - n^+$ thyristor structure. Note, to this regard, that, as mentioned in Section III-B, for t_r shorter than 10 ms,

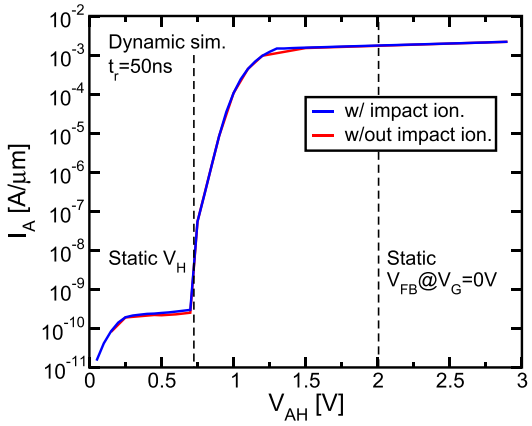

Fig. 13. I_A–V_{AH} curve ($t_r = 50$ ns) simulated when taking into account and when neglecting impact ionization.

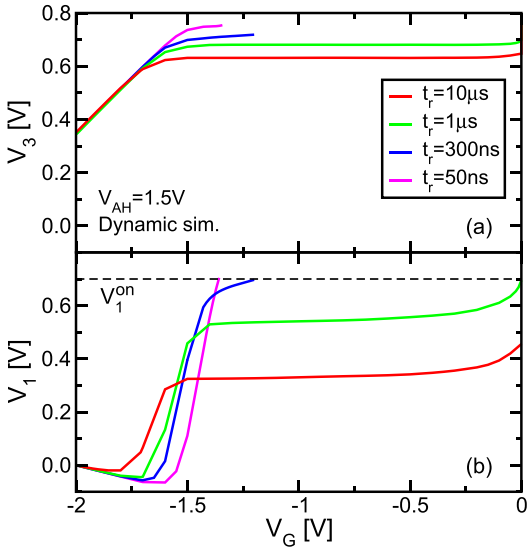

Fig. 14. Simulated evolution of V_1 and V_3 along the V_G ramp during a dynamic read operation, for different t_r ($V_{AH} = 1.5$ V). The curves are shown up to cell turn-ON, occurring when $V_1 = V_1^{ON}$. The small decrease in V_1 in the early stages of the V_G ramp comes from a direct parasitic capacitive coupling of the gate with the n-base [see (3)].

the current gain β_3 of the p-base/cathode junction is constant, and therefore β_1 represents the ultimate parameter determining the possibility of triggering thyristor turn-ON. On account of the low V_A required to turn the cell ON when short t_r values are adopted, in fact, avalanche multiplication plays a negligible role on the positive feedback of the thyristor structure. This is proved in Fig. 13, showing that no change in the I_A versus V_{AH} curve for $t_r = 50$ ns appears when avalanche multiplication is not activated in our simulations. This reveals that avalanche multiplication and high-field effects are not required for the operation of T-RAM cells, allowing the possibility of a very good reliability performance for the technology [9].

The evolution of the forward bias V_1 of the n-base/anode junction and that of V_3 is shown in Fig. 14 for four possible values of t_r and $V_A = 1.5$ V. In the case of $t_r = 10$ μs (red curves), the V_G switch makes V_3 saturate only slightly

above 0.6 V, resulting in a stationary electron current charging the n-base $I^*_{n3} = \beta_3 \cdot I^*_{p3}$. The integration of this current on the n-base leads to the increase in V_1 up to a stationary level about 0.3 V, which is kept until V_G comes close to 0 V. This behavior can be explained by considering that the increase in V_1 corresponds to an increase in I_{n1}, i.e., of the electron flow leaving the n-base toward the anode. The latter current reduces the increase in V_1, according to

$$\frac{dV_1}{dt} = \frac{I^*_{n3} - I_{n1}}{C_{J1} + C_{J2} + C_{\rm gn}} - \frac{dV_G}{dt} \cdot \frac{C_{\rm gn}}{C_{J1} + C_{J2} + C_{\rm gn}} \quad (3)$$

where C_{J1} and C_{J2} are the n-base to anode and to p-base capacitances, and $C_{\rm gn}$ is the parasitic capacitance between the gate and the undepleted n-base region. For the low I^*_{n3} achieved with long t_r, I_{n1} makes V_1 saturate at a level that is lower than the critical value required for thyristor turn-ON ($V_1^{\rm ON}$). When V_G approaches 0 V, however, V_3 has a nonnegligible increase owing to the depletion of the p-base from holes. When this happens, the stationary condition in the p-base electrostatics is lost, with the possibility of a further increase in both the electrostatic potential in this region and in I_{n3}. This, in turn, unbalances the stationary condition reached in the n-base, giving rise to the increase in V_1. Note, however, that, even with its final increase, V_1 is not enough to turn the cell ON. This is, instead, possible when $t_r = 1$ μs (green curves), as the faster V_G switch in this case makes V_1 saturate at a higher level, which is closer to $V_1^{\rm ON}$. For this value of t_r and for shorter values, therefore, early cell turn-ON occurs in the memory cell, as shown in Fig. 4. In the case of shorter t_r, in fact, the consequent increase in V_3^* and I^*_{n3} leads to cell turn-ON before a stationary electrostatics is reached in the n-base (see the blue curve in Fig. 14) or, in the case of a very short t_r, before the p-base itself reaches a stationary condition (see the magenta curve in Fig. 14).

IV. Read and Write Operations

The results reported in the previous section explained the basic evolution of the electrostatics and the carrier flows in the T-RAM cell and leading to early device turn-ON when dynamically operated according to the voltage scheme of Fig. 3(a). This voltage scheme represents a possible read scheme for the cell, making hole concentration in the p-base, the physical parameter determining the stored bit. Note, in fact, that early device turn-ON takes place only when a high hole concentration is present in the p-base, while p-base depletion precludes the phenomenon. This is proved in Fig. 15, where the I_A versus $V_{\rm AH}$ curve is reported with and without a previous write-0 operation, achieved by increasing V_G up to +2 V with grounded anode [7]. The results clearly reveal that after write-0, cell turn-ON happens only when $V_{\rm AH}$ is above the static $V_{\rm FB}$ at $V_{\rm GH}$, opening the possibility of exploiting the bistability window of the device for DRAM operation with the investigated dynamic read scheme.

From the analysis presented in the previous section, cell turn-ON following a read operation happens during the rise front of the V_G pulse. This means that the duration of the pulse plateau can be determined only by the required

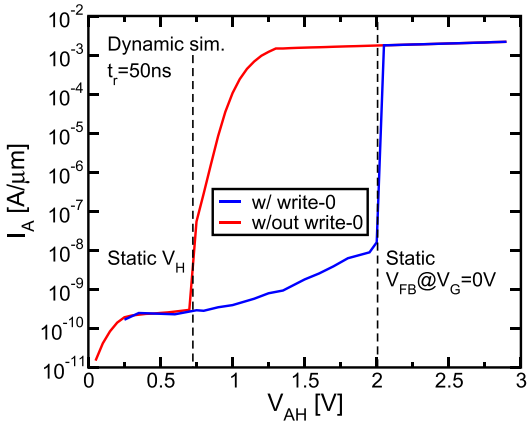

Fig. 15. Simulated I_A versus $V_{\rm AH}$ curve ($t_r = 50$ ns) with and without a previous write-0 pulse.

integration time of the anode current, which can be extremely short [5], [11] thanks to the orders-of-magnitude separation between the low and high current states of the memory cell. In addition to that, even the write-0 and write-1 operations can be very fast. As discussed in relation to Fig. 9, in fact, the discharge of the quasi-neutral p-base is only weakly dependent on t_r and mainly determined by the final value $V_{\rm GH}$ of the V_G pulse, meaning that fast write-0 can be achieved provided that $V_{\rm GH}$ well above 0 V are used. Fast write-1 operations are, instead, the result of the possibility of turning the T-RAM cell ON when this is in its 0 state. To this aim, $V_{\rm GH}$ in Fig. 3(a) should be so high to close the bistability window of the memory cell so that fast cell turn-ON can be achieved with $V_{\rm AH}$ just above the static hold voltage V_H.

V. Conclusion

In this paper, we presented a comprehensive numerical analysis of T-RAM cells, addressing the evolution of the electrostatics and of the carrier flows during dynamic device operation. The results highlight the basic physics on which cell operation relies and explain why T-RAM cells allow a very fast read and write performance.

Acknowledgment

The authors would like to thank A. Grossi, R. Bez, E. Camerlenghi, and P. Cappelletti from Micron Technology, Inc., for the discussions and support.

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