Fitting Cells Into a Narrow V_T Interval: Physical Constraints Along the Lifetime of an Extremely Scaled NAND Flash Memory Array

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I. Introduction

FITTING cells of a NAND Flash array into a narrow threshold-voltage (V_T) interval is of utmost importance for the development of multilevel (ML) technologies [1]–[5]. To this aim, understanding the impact and the relative weight of the major physical effects constraining the possibility of achieving and keeping a tight V_T distribution during array operation represents a mandatory task. Achieving a tight V_T distribution requires suitable program-and-verify algorithms [6], [7] able to move the V_T of the cells in a page of the NAND array close to a target level by calibrating the charge in their floating gate. The accuracy of this placement is limited mainly by the program noise (PN) coming from the statistical process of electron injection into the floating gate [8]–[10] and by random telegraph noise (RTN) [11]–[19]. Once a page has been programmed, then, its V_T distribution may be enlarged when programming the other pages in the array, mainly because of program disturbs and parasitic cell-to-cell interference [4], [20]–[23]. Note, however, that these effects largely depend on how pages are mapped into the NAND array and, moreover, may be largely reduced by increasing the complexity of the program algorithm [4], [24]. In addition, the distribution width may increase as time elapses during idle/bake periods, especially after a high number of program/erase (P/E) cycles has been performed on the array. When error correction codes are implemented to prevent the impact of anomalous cell behaviors on data retention [25], charge detrapping from the tunnel oxide represents the dominant mechanism affecting the V_T distribution [26]–[34]. Charge detrapping leads, in fact, to an average reduction of cell V_T arising from the neutralization of negative charge in the oxide. However, owing mainly to variability in the number of trapped charges, a relevant statistical dispersion of the V_T shift comes also into play, broadening the V_T distribution [27], [30], [33], [34].

In this paper, we compare the impact of the major physical effects constraining the width of the V_T distribution along the lifetime of a state-of-the-art NAND Flash array, focusing on PN, RTN, and charge detrapping. Results highlight how these effects affect the V_T distribution as a function of program conditions, temperature, cycling, and duration of idle/bake periods. Finally, the quantitative assessment of their role points out that these effects are almost equally important in modern technologies.

II. Time-0 Placement

A. Incremental Step Pulse Programming

We started our investigation by considering fresh (uncycled) arrays of our 1×-nm 2-bit/cell NAND Flash technology [1] and the possibility of achieving tight V_T distributions through the program operation. To this aim, we adopted the incremental step pulse programming (ISPP)-and-verify algorithm widely used in state-of-the-art NAND Flash products [6], [7]. ISPP involves applying a sequence of programming pulses to the selected word-line, increasing their amplitude by a constant step V_s. The result is a nice linear increase of the average V_T ($\langle V_T \rangle$) of the cells under program with the number of applied pulses [10], as shown in Fig. 1. This allows to make the major sources of variability among the cells negligible from

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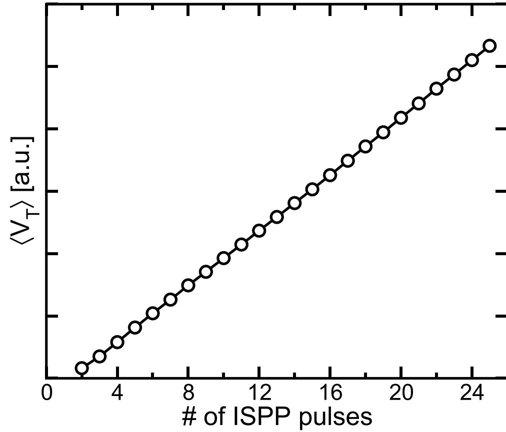

Fig. 1. Trend of the $\langle V_T \rangle$ of one page of the NAND array during ISPP.

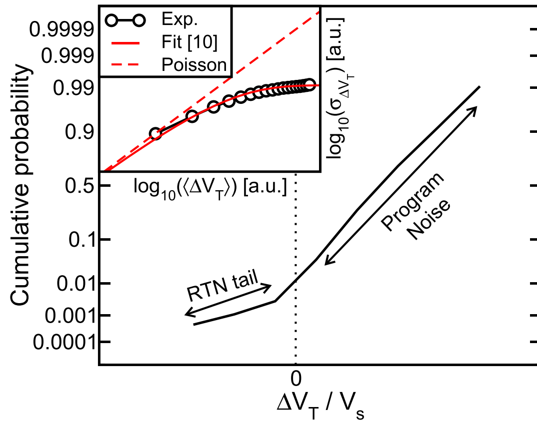

Fig. 2. Cumulative distribution of the ΔV_T of the cells in one page of the NAND array following the application of a single ISPP pulse. Inset: dependence of $\sigma_{\Delta V_T}$ on $\langle \Delta V_T \rangle$.

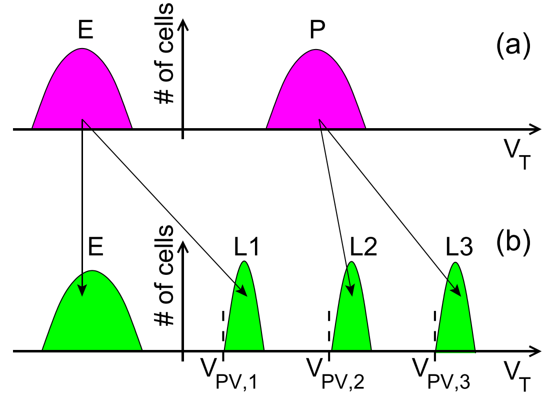

Fig. 3. Schematic for cell placement in the NAND array after (a) SL and (b) ML page programming.

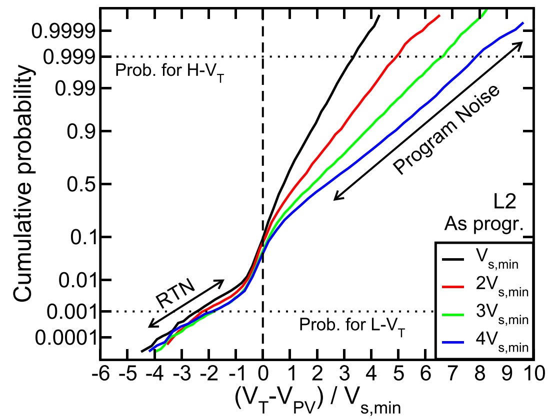

Fig. 4. V_T distribution of the monitored page of the NAND array resulting from the ISPP and verify algorithm, for different V_s multiple of a $V_{s,\min}$. Results refer to the case of programming the monitored page to level L2.

the programming standpoint, as the possibility of achieving nearly the same V_T increases (ΔV_T) per pulse for all of them allows to swiftly and accurately raise their V_T up to a program-verify (V_{PV}) level (note that the average ΔV_T per pulse is almost equal to V_s [10]). Verify operations in-between the ISPP pulses allow, in fact, to stop programming a cell in the selected page when its V_T overcomes V_{PV} and this makes the final displacement of cell V_T from V_{PV} strictly related to the ΔV_T arising from the last programming pulse.

Fig. 2 shows that the ΔV_T following a single ISPP pulse has a relevant statistical spread, attributed to two major physical sources. The first is the PN coming from the statistical process of electron injection into the floating gate [8]–[10], whose primary role on the positive branch of the ΔV_T distribution is proved by the typical sub-Poissonian trend of the resulting standard deviation versus average value ($\sigma_{\Delta V_T}$ versus $\langle \Delta V_T \rangle$) curve (see the inset) [10]. The second is RTN, introducing the low tail departing toward negative ΔV_T in Fig. 2 as a consequence of the possibility that some cells have a lower V_T after the ISPP pulse than before owing to electron emission from their tunnel oxide [19].

B. Accuracy of V_T Placement

The spread of the ΔV_T resulting from a single ISPP pulse represents a constraint to the accuracy of the program operation, reducing the possibility of controlling the displacement of cell V_T from V_{PV} at the end of programming. This point was explored considering the program operation moving the cells in a page of the NAND array from their single level (SL) to their ML placement, as shown in Fig. 3 (note that no other page in the array was programmed after the one under investigation to avoid additional cell-to-cell interference contributions to the page V_T distribution width). Through this operation, cells in the erased state (E) are either kept on the erased level or programmed to the lowest programmed level L1, while cells on the programmed state (P) are moved either to the intermediate programmed level L2 or to the highest programmed level L3. The V_T distribution resulting from the ISPP and verify algorithm is shown in Fig. 4 for level L2 and different V_s (multiple of a minimum value $V_{s,\min}$). The effect of PN and RTN clearly appears from the figure, with the former broadening the distribution well above $V_{\mathrm{PV}}+V_s$ and the latter introducing a tail of cells below V_{PV}. The distribution width is quantitatively addressed in Fig. 5, where the low (L-V_T) and high (H-V_T) edges of the distribution extracted, respectively, at a probability of 0.001 and 0.999, are shown as a function of V_s. Results reveal that the growth of H-V_T with V_s has a slope higher than 1, meaning that

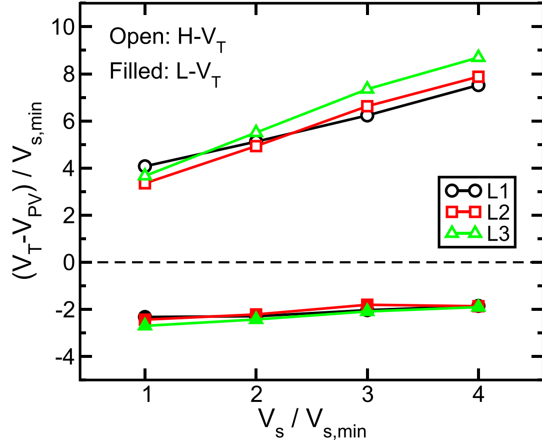

Fig. 5. L-V_T and H-V_T of the monitored page of the NAND array, as a function of V_s. Results achieved when moving the page to levels L1–L3 are shown.

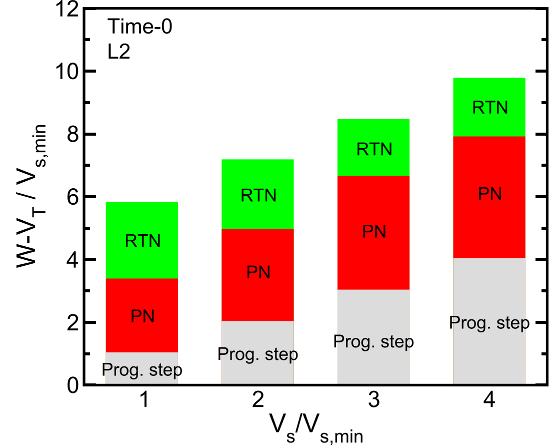

Fig. 7. Width of the V_T distribution (W-V_T) of the monitored page, decomposed in its major contributions, as a function of V_s.

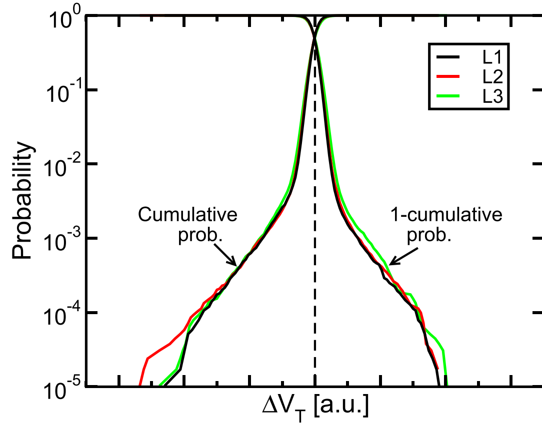

Fig. 6. Cumulative distribution of the ΔV_T between two consecutive read operations on a page of the NAND array (no programming pulse in-between reads), for the three programmed V_T levels of the monitored page. To better highlight the behavior of the distributions close to 1 in the semilogarithmic plot, their complementary is also shown.

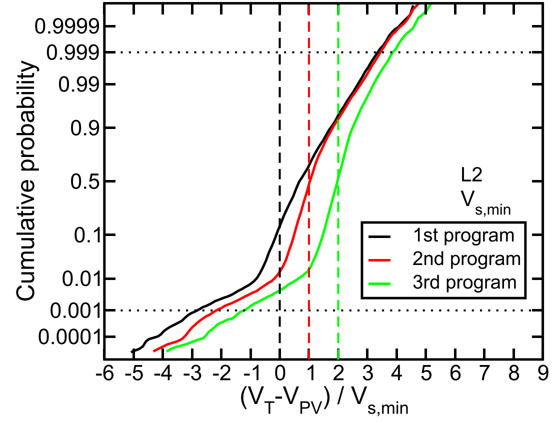

Fig. 8. V_T distribution of the monitored page after subsequent ISPP program operations. The program verify level has been increased by V_s from one program operation to the next.

the PN contribution to the width of the V_T distribution increases for higher V_s. In addition, the broadening of the V_T distribution above $V_{\rm PV}$ for higher V_s comes along with a slight narrowing of the distribution below $V_{\rm PV}$, as appearing from the slight increase of L-V_T in Fig. 5 and as previously discussed in [19]. The figure shows, moreover, that both L-V_T and H-V_T are almost independent of the target level of the program operation. This comes from the fact that PN depends only on $\langle \Delta V_T \rangle$, i.e., on V_s, [10] and that RTN instabilities are nearly equivalent on all of the programmed levels, as shown in Fig. 6.

Summarizing the previous results, Fig. 7 highlights the contribution of the program step, PN and RTN, to the width of the V_T distribution (W-V_T $=$ H-V_T-L-V_T) of our ML device, as a function of V_s. Results reveal that, further to scaling of cell capacitances, PN represents today the most relevant contribution to W-V_T for the relatively high V_s adopted in 2-bit/cell arrays ($V_s = 4V_{s,\rm min}$). For the small V_s required by 3-bit/cell devices ($V_s = V_{s,\rm min}$), instead, PN and RTN have almost the same impact on W-V_T.

C. Improving Placement Accuracy

The PN contribution to W-V_T can be reduced by lowering V_s or using more complex and time-consuming programming schemes [35]. We explored this latter possibility in Fig. 8, where the monitored page is first programmed to level L2 and then reprogrammed (no erase operation in between) increasing the program-verify level from the initial value $V_{\rm PV}$ (first program) to $V_{\rm PV}+V_s$ (second program) and then to $V_{\rm PV}+2V_s$ (third program). Results show a clear narrowing of the V_T distribution further to page reprogramming, as quantitatively highlighted in Fig. 9. This comes from the reduction of the ISPP voltage to its initial value when repeating the program operation. This reduction, in fact, makes the cells below the increased program-verify level raise their V_T much less than V_s during the first steps of the new ISPP ramp, reducing, in turn, PN [35]. The reduction of PN makes W-V_T eventually hit against the RTN constraint, representing an unavoidable process-related limitation to the possibility of targeting more than 2-bit/cell storage.

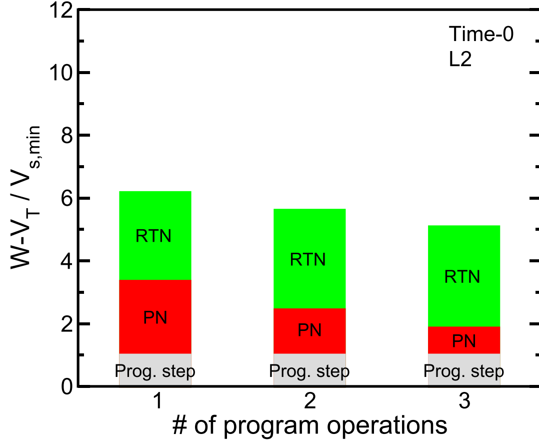

Fig. 9. Same as in Fig. 7, but as a function of the number of program operations on the monitored page according to Fig. 8.

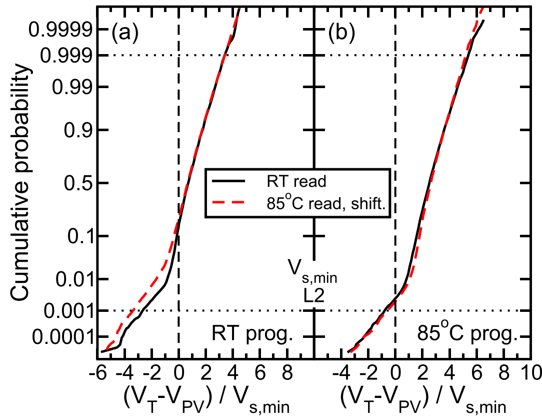

Fig. 10. V_T distribution of the monitored page. (a) Programmed at RT and read at RT and at 85 °C. (b) Programmed at 85 °C and read at RT and at 85 °C. The curve at 85 °C has been horizontally shifted to allow a better comparison of the distribution width.

D. Impact of Temperature on V_T Placement

To investigate the possible impact of temperature on W-V_T, we considered first the case where temperature is increased after cell placement, i.e., programming takes place at room temperature (RT) and then temperature is increased. Fig. 10(a) shows that the V_T distribution is barely affected by a temperature increase from RT to 85 °C, revealing that the statistical distribution of RTN instabilities is almost temperature independent. In addition to that, in Fig. 10(b), we addressed the case where program-and-verify is directly performed at high temperature. Results show that the achieved V_T distribution is nearly identical to that obtained at RT in Fig. 10(a), meaning that both the RTN and the PN [9] constraint to programming accuracy are not affected by temperature.

III. Impact of P/E Cycling on Cell Placement

P/E operations are a well-recognized source of electrical stress for the tunnel oxide of Flash cells, increasing the trap and the charge density therein. In particular, P/E cycles create new traps active in the RTN process, broadening the distribution of the ΔV_T detected between two consecutive read operations on a page of the memory array, as shown in Fig. 11 (in order to investigate only the RTN contribution

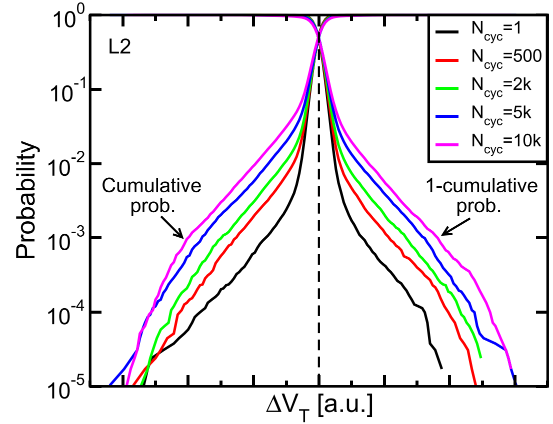

Fig. 11. RTN distribution for increasing cycling doses on the array.

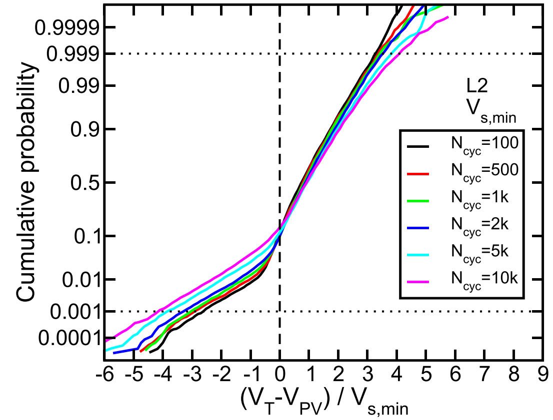

Fig. 12. Results of V_T placement on a cycled array for increasing cycling doses N_{cyc}. Target level is L2 and $V_s = V_{s,\text{min}}$.

to ΔV_T, no programming pulse has been applied between the two read operations). Note that, as previously discussed in [36], this broadening comes from the increase of the height of the exponential tails of the ΔV_T distribution, with negligible changes in their slope.

As a consequence of the higher RTN instabilities, Fig. 12 shows a slight reduction of the accuracy of cell placement by ISPP-and-verify after heavy array cycling. The programmed V_T distribution, in fact, broadens below V_{PV} on cycled arrays (see also L-V_T in Fig. 13), reflecting the broadening of the ΔV_T distribution in Fig. 11. Thanks to the PN independence of cycling [9], the positive branch of the V_T distribution in Fig. 12 is, instead, barely modified for N_{cyc} up to 2k. For higher N_{cyc}, instead, a slight enlargement also of the right branch of the distribution starts to appear at high probabilities (see H-V_T in Fig. 13). This is attributed, again, to the increase of RTN instabilities and to the broadening of the ΔV_T distribution shown in Fig. 11, making the displacement of some cells above V_{PV} higher than that determined by PN alone [37].

IV. Charge Detrapping During Idle/Bake Periods

Detrapping of charge from the tunnel oxide represents one of the most relevant reliability issues for state-of-the-art NAND Flash technologies. The phenomenon leads, first of all, to an average reduction of cell V_T as time elapses

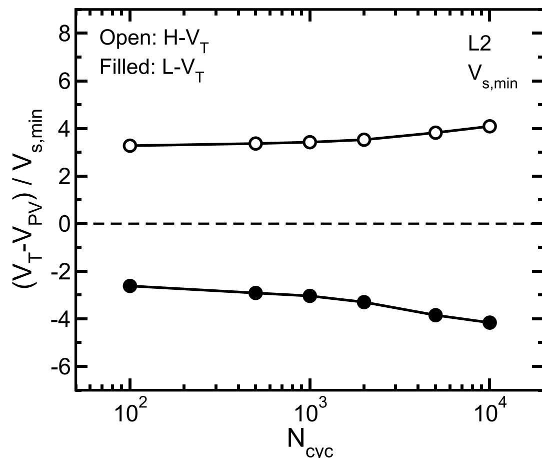

Fig. 13. L-V_T and H-V_T of the monitored page as a function of N_{cyc} for $V_s = V_{s,\text{min}}$.

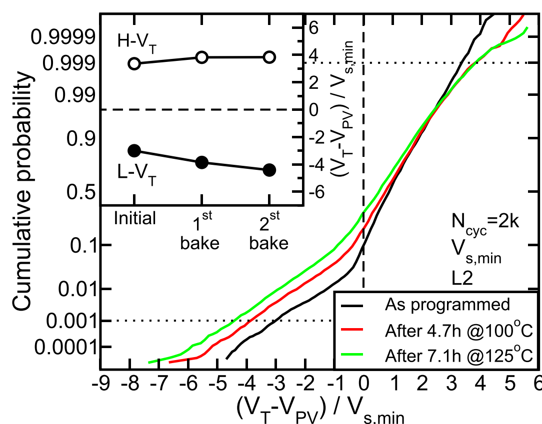

Fig. 14. V_T distribution of the monitored page as programmed to level L2, after a 4.7-h bake at 100 °C and after an additional 7.1-h bake at 125 °C. Results have been obtained on a cycled array ($N_{\text{cyc}} = 2$ k) with $V_s = V_{s,\text{min}}$.

during idle/bake periods [26]–[29], owing to a dominant neutralization of negative charge in the oxide. In addition to that, however, a nonnegligible statistical dispersion of the V_T shift as a function of time has been clearly detected in decananometer Flash arrays [27], [30], [33], [34]. This dispersion, attributed mainly to variability in the amount, and even in the polarity, of the charge trapped in the tunnel oxide of the array cells, results in a broadening of the V_T distribution, which is particularly relevant on cycled arrays, on account of charge trapping in the tunnel oxide arising from the electrical stress determined by P/E cycles.

To address the broadening of the V_T distribution coming from charge detrapping, we performed two consecutive bake experiments on a cycled array, monitoring the V_T of the cells in a page previously placed on one of the three possible programmed levels of the ML device (Fig. 3). To test our cells in realistic on-field use conditions, array cycling was performed following [38], with N_{cyc} P/E cycles done over a stretch of time 500-h long at 85 °C. Keeping the device at elevated temperature during cycling and reducing the pace at which the P/E cycles are performed with respect to the minimum required time aim at reproducing the so-called distributed-cycling effect. This effect consists in the reduction of the total charge trapped in the tunnel oxide of the array

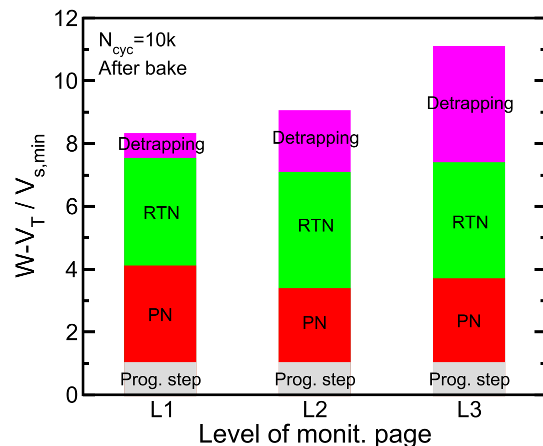

Fig. 15. Same as in Fig. 7, but as a function of the V_T level of the monitored page. Results refer to a heavily cycled sample ($N_{\text{cyc}} = 10$ k) after bake tests.

cells at the end of cycling when idle periods are present in-between the P/E cycles, as usually happens under real on-field usage of the device [27]–[29]. The two following bake tests were performed at 100 °C for 4.7 h and at 125 °C for 7.1 h, respectively, representing typical accelerated retention tests [38]. The V_T distribution after programming and after the next bake tests is shown in Fig. 14 in the case of $N_{\text{cyc}} = 2$ k P/E cycles and of page placed on level L2. A clear enlargement of the distribution toward lower V_T values appears after the bake test, with minor changes in the upper part of the distribution (see the evolution of H-V_T and L-V_T in the inset). Fig. 15 directly compares the contribution of charge detrapping to W-V_T with that coming from the program step, PN, and RTN. Results reveal that charge detrapping is as relevant as RTN and PN on heavily cycled arrays ($N_{\text{cyc}} = 10$ k P/E cycles) when cells are on level L3, while its contribution is less important when cells are on lower V_T levels. Note, in fact, that charge detrapping displays a significant reduction when moving NAND cells from L3 to L1, as previously reported in [29].

V. Conclusion

We have presented a comparative analysis of the physical effects constraining the possibility of fitting the cells of a 1×-nm NAND array into a narrow V_T interval. Results have highlighted the role of PN, RTN, and charge detrapping along array lifetime, giving clear design hints for the development of next-generation technology nodes.

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