

# Investigation of the Turn-ON of T-RAM Cells Under Transient Conditions

Halid Mulaosmanovic, Christian Monzio Compagnoni, *Senior Member, IEEE*, Niccolò Castellani, Giovanni M. Paolucci, Gianpietro Carnevale, Paolo Fantini, Domenico Ventrice, Andrea L. Lacaita, *Fellow, IEEE*, Alessandro S. Spinelli, *Senior Member, IEEE*, and Augusto Benvenuti, *Member, IEEE*

## I. INTRODUCTION

**T**HE idea of controlling the turn-ON and the turn-OFF of a thyristor by the field-effect exerted by insulated gate contacts has been largely exploited in the past for high-power applications [1], [2]. However, only more recently has this idea been explored to develop next-generation nanoscale solid-state volatile memory cells [3]–[12]. In particular, the exploitation of the bistability of a nanoscale gated-thyristor to achieve dynamic RAM (DRAM)-like operation relies on the possibility of creating a transient condition in the device affecting its turn-ON when a specific gate voltage ( $V_G$ ) waveform is applied [7], [11]. This transient condition is typically obtained by changing the carrier density in some of the device regions [7], [11], [13]–[15], thus triggering the

generation/recombination processes trying to restore the stationary concentration profiles.

T-RAM cells represent one of the most promising exploitations of nanoscale gated-thyristors for DRAM-like applications [7], [11]. Device operation relies on the possibility of leading the thyristor either to its ON or to its OFF state during *dynamic sensing* operations depending on the hole concentration in the  $p$ -base [16]. Dynamic sensing consists in the fast increase of  $V_G$  from a low ( $V_{GL}$ ) to a high ( $V_{GH}$ ) value in the presence of an anode bias ( $V_A$ ) lower than the static forward-breakover voltage ( $V_{FB}$ ) and results in device turn-ON during the rise front of  $V_G$  only if a high enough amount of holes is present in the  $p$ -base [17]. This makes the hole concentration in the  $p$ -base the physical element determining the memory effect, with the possibility of having a stable 1 state in the presence of the stationary hole concentration at  $V_{GL}$  and a transient 0 state corresponding to a depleted  $p$ -base [16]. For best technology performance, prolonging the maximum stretch of time allowing the thyristor to remain in its OFF state during dynamic sensing after a write-0 operation, representing the cell data retention time, is of utmost importance and requires a careful investigation of the applied voltage waveforms.

In this paper, enhancing the preliminary work reported in [18], we present the first experimental investigation of the dynamic turn-ON of T-RAM cells under the transient conditions given by a depleted  $p$ -base, as a function of the voltage waveforms used for device operation. The results reveal that the stretch of time along which dynamic turn-ON is precluded after a write-0 operation depends on the gate and anode bias during the hold phase ( $V_{GL}$  and  $V_{AL}$ , respectively) and on  $V_{GH}$ , i.e., the high gate voltage used for dynamic sensing. This is explained considering the rate of electron–hole pair generation in the device and the  $p$ -base potential required to turn the device on during dynamic sensing as a function of the hold and sensing voltages. The design guidelines coming from these results are a significant contribution to the development of next-generation nanoscale T-RAM cells.

## II. EXPERIMENTAL RESULTS

### A. Main Evidence

Figs. 1(a) and 1(b) show the schematics of the nanoscale T-RAM cell investigated in this paper and its corresponding

Manuscript received October 21, 2014; revised January 8, 2015; accepted January 28, 2015. Date of publication February 23, 2015; date of current version March 20, 2015. The review of this paper was arranged by Editor U. E. Avci.

H. Mulaosmanovic, C. Monzio Compagnoni, N. Castellani, G. M. Paolucci, and A. S. Spinelli are with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan 20133, Italy (e-mail: halid.mulaosmanovic@polimi.it; monzio@elet.polimi.it; ncastellani@elet.polimi.it; paolucci@elet.polimi.it; spinelli@elet.polimi.it).

G. Carnevale, P. Fantini, D. Ventrice, and A. Benvenuti are with the Process Research and Development, Micron Technology Inc., Agrate Brianza 20864, Italy (e-mail: gcarneva@micron.com; pfantini@micron.com; dventric@micron.com; abenvenu@micron.com).

A. L. Lacaita is with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan 20133, Italy, and also with the Istituto di Fotonica e Nanotecnologie-Consiglio Nazionale delle Ricerche, Milan 20133, Italy (e-mail: andrea.lacaita@polimi.it).

Color versions of one or more of the figures in this paper are available online.

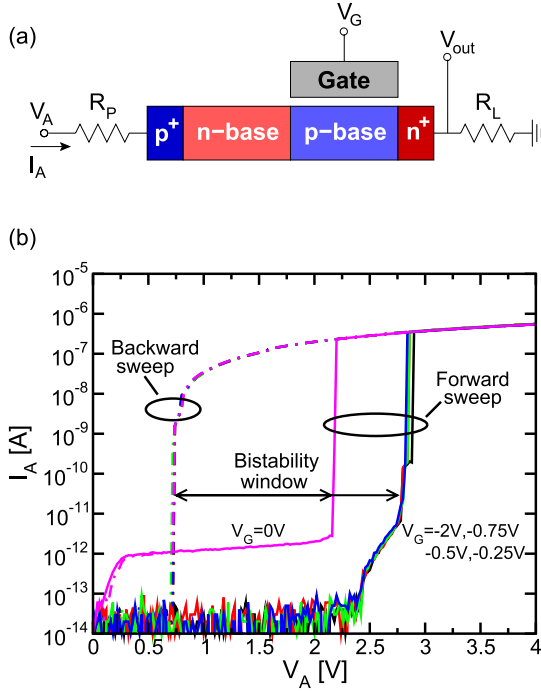


Fig. 1. (a) Schematics for the nanoscale gated-thyristor investigated in this paper (the  $n$ - and  $p$ -base are nearly 100 nm long, the silicon thickness is  $30 \times 30 \text{ nm}^2$ , and the gate oxide thickness is 5 nm). (b) Corresponding  $I_A$ - $V_A$  characteristics as obtained from a slow forward and backward sweep of  $V_A$  at constant  $V_G$  (static  $I_A$ - $V_A$  curves). A protection resistance of 5.5 M $\Omega$  was put in series to the anode of the device in this measurement, aiming at limiting  $I_A$  when the gated-thyristor is ON [17].

anode current versus anode voltage ( $I_A$ - $V_A$ ) characteristics as obtained from a slow forward and backward sweep of  $V_A$  at constant  $V_G$ , ranging between  $-2$  and  $0$  V. Thanks to the low ramp rate of  $V_A$  (in the tens-of-seconds timescale), the curves reported in Fig. 1(b) correspond to the *static* electrical characteristics of the device, allowing the definition of its bistability window as the region of  $V_A$  between the sudden increase of  $I_A$  during the forward sweep (static  $V_{FB}$ ) and the sudden drop of  $I_A$  during the backward sweep (static hold voltage,  $V_H$ ). As clearly appearing from Fig. 1(b), this window is barely dependent on  $V_G$  when this voltage increases from  $-2$  to  $-0.25$  V, while a significant reduction of its width appears for  $V_G = 0$  V, due to a reduction of the static  $V_{FB}$  [4], [18].

In agreement with what has been reported in [17], Fig. 2(a) shows that a fast transition of  $V_G$  from a low value  $V_{GL} = -2$  V to a high value  $V_{GH} = -0.25$  V allows a *dynamic* turn-ON of the gated-thyristor for whatever  $V_A$  in the bistability region highlighted in Fig. 1(b) ( $V_{AH} = 1.5$  V was used in the example, with the rise of  $V_A$  preceding that of  $V_G$ ). This results from a reduction of  $V_{FB}$  from the static value when the device is dynamically operated, thanks to a higher  $p$ -base potential and, in turn, electron current from the cathode to the  $n$ -base triggering device turn-ON, when the  $V_G$  increase is so fast to limit the hole discharge of the  $p$ -base (a rise time of the  $V_G$  pulse equal to 50 ns was used in the experiment, limited by our setup). Note, in this regard, that device turn-ON happens on the rise front of the  $V_G$  pulse and

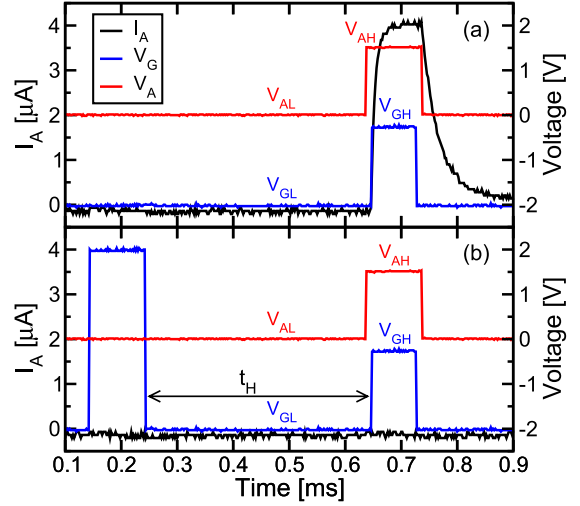


Fig. 2. (a) Example of the  $V_G$  and  $V_A$  waveforms applied for dynamic sensing of the T-RAM cell state and resulting  $I_A$  (obtained as  $V_{out}/R_L$  in the setup of Fig. 1, where no protection resistance  $R_P$  was used and  $R_L = 100 \text{ k}\Omega$ ): thanks to the fast  $V_G$  transition ( $\approx 50$  ns, limited by our experimental setup), device turns ON even with a  $V_{AH}$  lower than its static  $V_{FB}$  (1.5 V in this case). (b) Dynamic turn-ON is inhibited when a highly positive  $V_G$  pulse is applied prior to dynamic sensing. All the main experimental parameters have been highlighted in the figures.

does not depend on the duration of the pulse plateau. This latter duration was set to 100  $\mu\text{s}$  in the experiment to clearly observe the  $I_A$  waveform in the presence of the load resistance  $R_L = 100 \text{ k}\Omega$  in the setup of Fig. 1(a).

Starting from these preliminary results, highlighting the strong differences between the static and the dynamic operations of T-RAM cells, Fig. 2(b) shows that the dynamic turn-ON of the gated-thyristor can be avoided if a highly positive gate pulse ( $V_G = +2$  V was used in the example) is applied prior to dynamic sensing of  $I_A$ , thanks to the consequent depletion of the  $p$ -base of holes which makes the dynamic  $V_{FB}$  of the device increase up to the static value. This paves the way for the exploitation of the T-RAM cell as a DRAM device, with holes in the  $p$ -base representing the physical parameter determining the memory state of the cell [16]. When the  $V_A$  and  $V_G$  waveforms shown in Fig. 2(a) are applied to read the cell current, in fact, the possibility to turn the cell on depends only on the  $p$ -base potential and, in turn, on the amount of holes in the  $p$ -base, determining the electron current flowing from the cathode to the  $n$ -base. The positive  $V_G$  pulse applied prior to read in Fig. 2(b) acts, therefore, as a write-0 operation on the cell, removing holes from the  $p$ -base and then affecting the possibility for cell turn-ON during the next dynamic sensing operations. Note, however, that the consequences of the pulse on the dynamic turn-ON of the T-RAM cell are just transient, due to carrier generation taking place in the hold time ( $t_H$ ) between pulse and sensing, and bringing the device back to its stable state 1 [19]–[21].

To address the transient nature of  $p$ -base depletion and its consequences on the dynamic turn-ON of T-RAM cells, we repeated the experiment of Fig. 2(b)  $10^3$  times to statistically evaluate the probability to turn the device on when

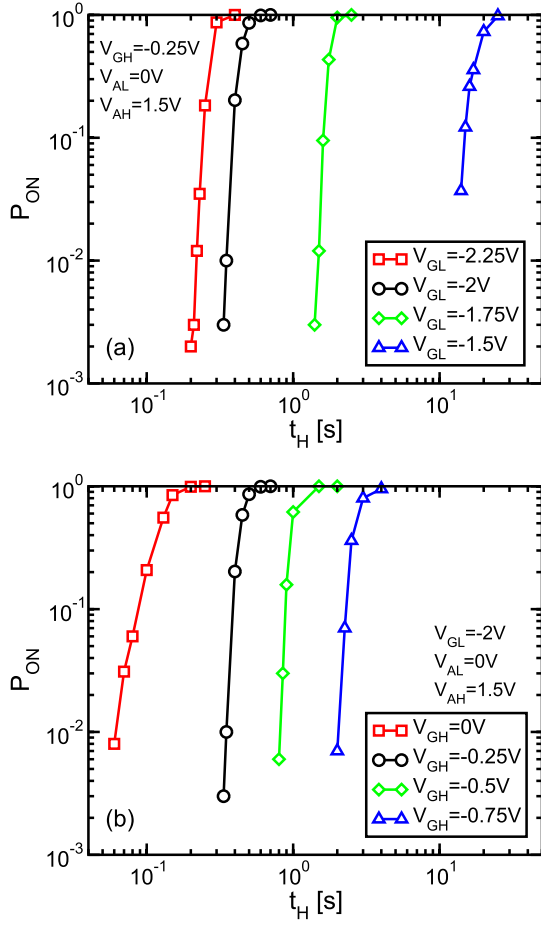


Fig. 3.  $P_{ON}$  dependence on  $t_H$  when changing (a)  $V_{GL}$  ( $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V) and (b)  $V_{GH}$  ( $V_{GL} = -2$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V) in the experimental test of Fig. 2.

dynamically sensing its  $I_A$  ( $P_{ON}$ ), as a function of  $t_H$ .  $P_{ON}$  represents the probability of a memory cell failure after storing bit-0 and grows for longer  $t_H$  due to hole generation in the device. The results are shown in Fig. 3(a) and (b) for different  $V_{GL}$  ( $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V) and different  $V_{GH}$  ( $V_{GL} = -2$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V). First of all, the curves display a very strong sensitivity of  $P_{ON}$  on  $t_H$ , revealing a negligible impact of the statistical nature of the carrier generation process on the results. Moreover, the curves exhibit a shift toward longer  $t_H$  for higher  $V_{GL}$  [Fig. 3(a)] and lower  $V_{GH}$  [Fig. 3(b)]. To quantify more in detail these dependences, Fig. 4 reports the median data retention time  $\overline{t_H}$  (i.e., the  $t_H$  corresponding to  $P_{ON} = 0.5$ ) as a function of  $V_{GH}$ , with  $V_{GL}$  as a parameter ( $V_{AL} = 0$  V,  $V_{AH} = 1.5$  V): an increase of more than a factor 60 and 20 appears, respectively, in the retention time when increasing  $V_{GL}$  from  $-2.25$  to  $-1.5$  V with  $V_{GH} = -0.25$  V and when decreasing  $V_{GH}$  from 0 to  $-0.75$  V with  $V_{GL} = -2$  V.

In addition to the  $V_G$  dependence, Fig. 5(a) shows that the  $P_{ON}$  curves display a significant dependence on  $V_{AL}$ , i.e., the anode bias during the hold phase, while are mostly unaffected by  $V_{AH}$  [Fig. 5(b)], i.e., the anode bias during dynamic sensing. In particular, Fig. 5(a) shows that the reduction

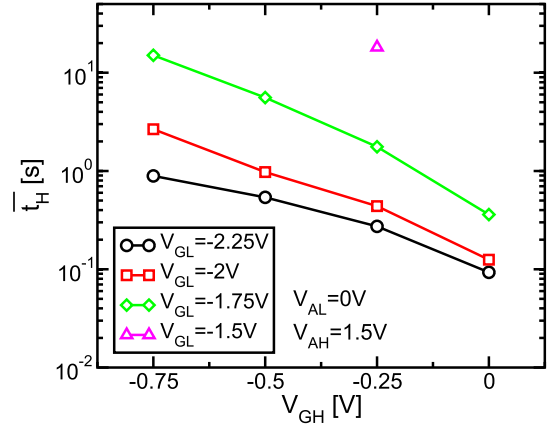


Fig. 4.  $\overline{t_H}$  as a function of  $V_{GH}$ , with  $V_{GL}$  as a parameter, for  $V_{AL} = 0$  V and  $V_{AH} = 1.5$  V.

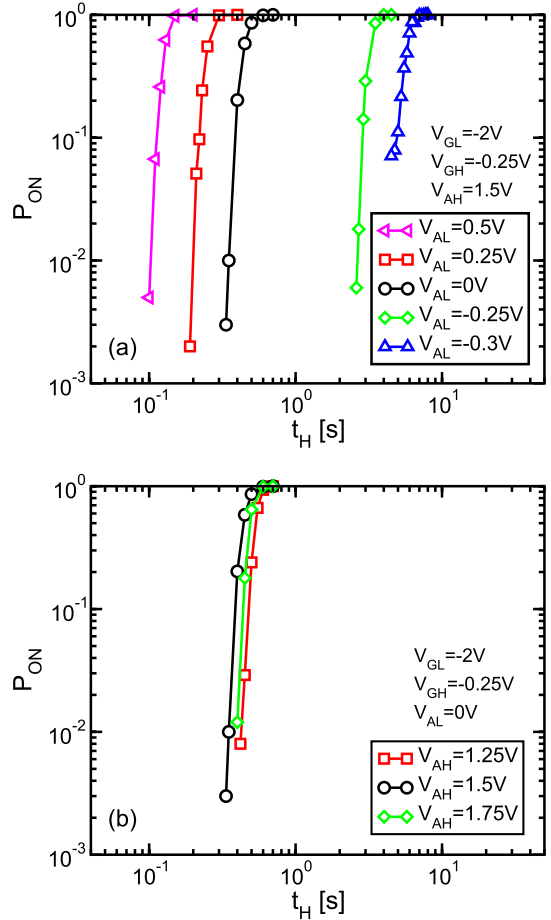


Fig. 5. Same as in Fig. 3, but for different (a)  $V_{AL}$  and (b)  $V_{AH}$  and fixed  $V_{GL} = -2$  V and  $V_{GH} = -0.25$  V.

of  $V_{AL}$  moves the  $P_{ON}$  curves toward longer  $t_H$ , positively impacting, in turn, cell data retention. This is also better quantified by the  $\overline{t_H}$  trend in Fig. 6, revealing an increase of more than a factor 40 in data retention when  $V_{AL}$  is reduced from 0.5 to  $-0.3$ .

As a final remark, note that the test of Fig. 2(a) (no pulse prior to dynamic sensing) was also repeated  $10^3$  times for

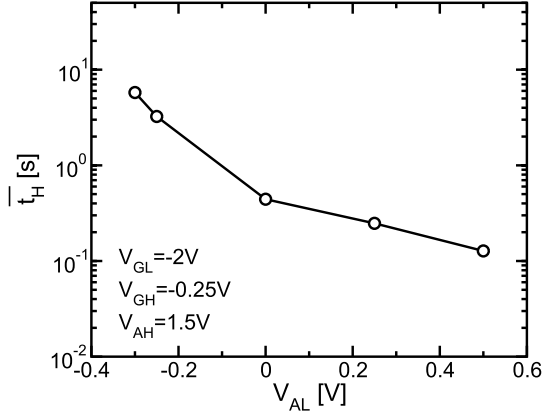


Fig. 6.  $\overline{t_H}$  as a function of  $V_{AL}$ , with  $V_{GL} = -2$  V,  $V_{GH} = -0.25$  V, and  $V_{AH} = 1.5$  V.

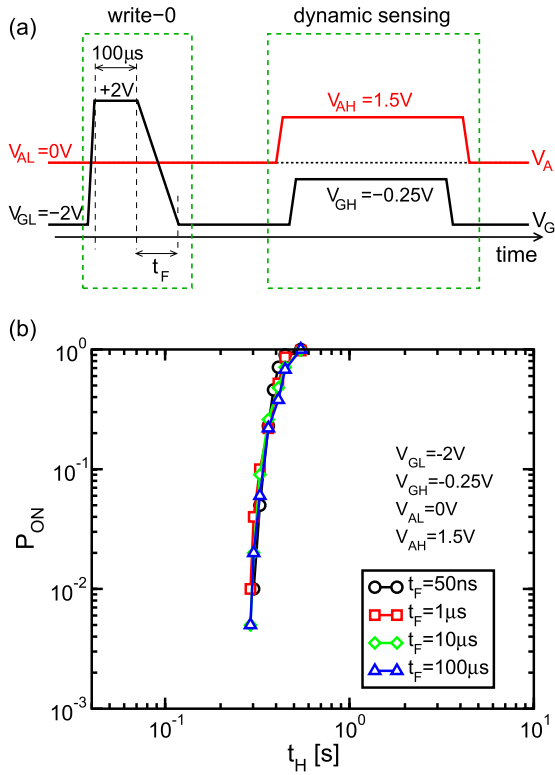


Fig. 7. (a)  $V_G$  and  $V_A$  waveforms used to investigate the effect of the fall time  $t_F$  of the write-0 pulse on the  $P_{ON}$  versus  $t_H$  curve. (b) Corresponding results obtained with  $V_{GL} = -2$  V,  $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V.

the same  $V_{GL}$ ,  $V_{GH}$ ,  $V_{AL}$ , and  $V_{AH}$  considered in Figs. 3–5 and device turn-ON was observed in 100% of the cases. This confirms, first of all, that state 1 is stable for the explored operating voltage levels [18] and, then, that the inhibition of cell turn-ON and, in turn, the resulting  $P_{ON}$  curves obtained from the experiment of Fig. 2(b) are only the consequence of the write-0 pulse and not of any parasitic experimental effect. Exploring higher values of  $V_{GL}$  or lower values of  $V_{GH}$  than those considered in Figs. 3 and 4 may result, however, in the possibility that the cell does not turn ON in the experiment of Fig. 2(a) [18], representing a nonsuitable

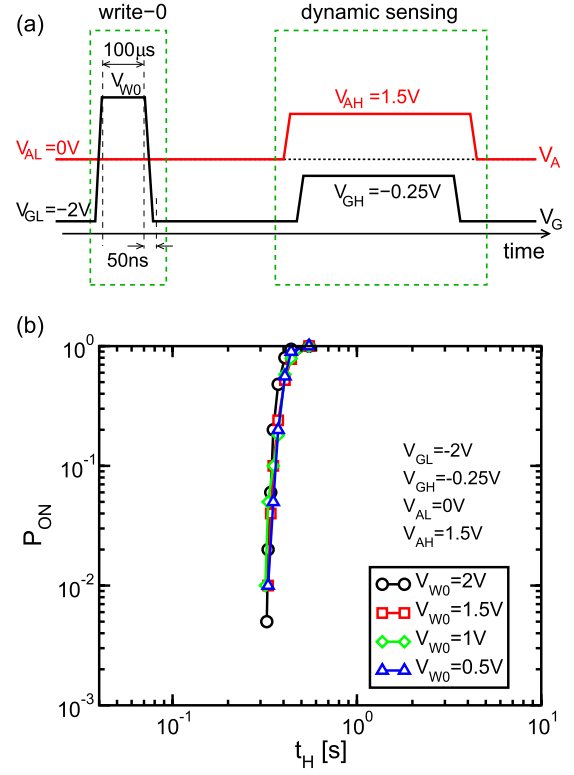


Fig. 8. (a)  $V_G$  and  $V_A$  waveforms used to investigate the effect of the amplitude of the write-0 pulse  $V_{W0}$  on the  $P_{ON}$  versus  $t_H$  curve. (b) Corresponding results obtained with  $V_{GL} = -2$  V,  $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V.

operating condition. Moreover, even increasing  $V_{GH}$  above 0 V may be unsuitable for cell operation, as this may lead to the closure of the bistability window shown in Fig. 1(b) and, therefore, to cell turn-ON even after a write-0 pulse.

### B. Further Control Experiments

To investigate more in depth the origin of the dependence of cell turn-ON inhibition after a write-0 pulse on the operating voltage waveforms, we modified some of the parameters of the experimental test of Fig. 2(b). First of all, we explored the possibility that a different number of holes remains in the  $p$ -base after the write-0 pulse when a different  $V_{GL}$  is adopted, due to transient parasitic hole injections during the falling edge of the pulse. To this aim, we measured the  $P_{ON}$  versus  $t_H$  curve increasing the duration of the falling edge of the write-0 pulse ( $t_F$ ) from 50 ns up to 100  $\mu$ s, with fixed  $V_G$  and  $V_A$  levels, according to the experimental scheme of Fig. 7(a). The results are shown in Fig. 7(b) ( $V_{GL} = -2$  V,  $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V) and do not display any significant change with the reduction of the steepness of the falling edge of the write-0 pulse. This confirms that the dependence of the  $P_{ON}$  versus  $t_H$  curve on  $V_{GL}$  appearing in Fig. 3(a) is not the result of a different effectiveness of the write-0 pulse in depleting the  $p$ -base but only of changes in the physical processes taking place during the hold phase. This is further confirmed in Fig. 8(b), where the  $P_{ON}$  versus  $t_H$  curve appears unaffected by the reduction of

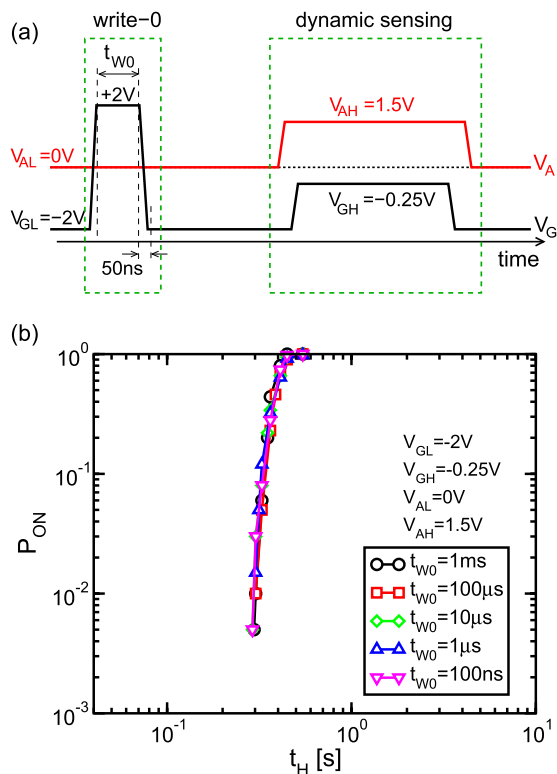


Fig. 9. (a)  $V_G$  and  $V_A$  waveforms used to investigate the effect of the duration of the write-0 pulse  $t_{W0}$  on the  $P_{ON}$  versus  $t_H$  curve. (b) Corresponding results obtained with  $V_{GL} = -2$  V,  $V_{GH} = -0.25$  V,  $V_{AL} = 0$  V, and  $V_{AH} = 1.5$  V.

the amplitude of the write-0 pulse ( $V_{W0}$ ) from  $+2$  to  $+0.5$  V [see the experimental scheme of Fig. 8(a)], meaning that the explored time and amplitudes of the write-0 pulse allow a complete depletion of the  $p$ -base from holes. Finally, Fig. 9 considers the case where the duration of the write-0 pulse ( $t_{W0}$ ) is reduced down to  $100$  ns (a), highlighting that the  $P_{ON}$  versus  $t_H$  curve remains mostly unaltered (b). This clearly confirms that the T-RAM cell has the possibility to address DRAM applications [11], requiring very fast write and read operations.

### III. PHYSICAL PICTURE

The experimental results of Section II can be explained considering that the dynamic turn-ON of nanoscale gated-thyristors relies on the presence of holes in the  $p$ -base when  $V_G$  experiences its fast transition from  $V_{GL}$  to  $V_{GH}$  [17]. As a consequence, when the highly positive write-0 pulse is applied to the device gate in Fig. 2(b) and the  $p$ -base goes fully depleted from holes, dynamic turn-ON is precluded over the stretch of time immediately following the pulse application. However, this represents a nonequilibrium condition which triggers the generation of electron-hole pairs, with electrons rapidly leaving the  $p$ -base and holes accumulating in it [7], [11], [13], [14], thus restoring the possibility for a dynamic turn-ON after a certain  $t_H$ . Within this picture, the shift of the  $P_{ON}$  curves toward longer  $t_H$  when lowering  $V_{AL}$  [Fig. 5(a)] or increasing  $V_{GL}$  [Fig. 3(a)] is just the direct consequence of the reduced reverse bias

of the  $p$ -base with its neighboring  $n$  regions, resulting in the reduction of the electron/hole generation rate trying to restore the stationary charge conditions in the device that correspond to  $V_{GL}$ . This, in turn, increases the  $t_H$  required to have enough holes in the  $p$ -base to allow device turn-ON during the next dynamic sensing operation at  $V_{GH}$ . More specifically, note that the T-RAM cell of Fig. 1 turns on when a high enough electron flow from the cathode to  $n$ -base, i.e., a high enough potential of the  $p$ -base, is obtained as a result of the fast increase of  $V_G$  involved in the dynamic sensing operation. For fixed  $V_{GH}$ , this means that the same amount of holes must be present in the  $p$ -base when changing  $V_{AL}$  and  $V_{GL}$  and this can be achieved only after longer  $t_H$  when  $V_{AL}$  is reduced and when  $V_{GL}$  is increased, as a consequence of a lower electric field. When  $V_{GH}$  is reduced, instead, triggering the same electron flow from the cathode to the  $n$ -base and the same potential in the  $p$ -base requires a larger amount of holes in this region and this requires, for fixed  $V_{GL}$  and  $V_{AL}$ , a longer  $t_H$ , leading to the rightward shift of the  $P_{ON}$  curves in Fig. 3(b). Note, finally, that in the case the thyristor remains OFF during dynamic sensing, a higher  $V_{GH}$  may contribute to keep a hole depletion condition in the  $p$ -base at the end of the sensing phase, contributing to the regeneration of state 0 in the memory cell and achieving a similar effect to the application of the high  $V_G$  pulse in Fig. 2 [22].

### IV. CONCLUSION

In this paper, we presented a detailed experimental investigation of the dynamic turn-ON of nanoscale T-RAM cells after hole depletion is created in the  $p$ -base by a write-0 operation. The results showed that hole depletion prevents dynamic device turn-ON over a stretch of time largely changing with  $V_{GL}$ ,  $V_{AL}$ , and  $V_{GH}$ . A physical explanation of the results was provided, based on the dependence of the hole generation rate and of the amount of holes in the  $p$ -base required for dynamic device turn-ON on the applied biases. The results represent a significant contribution to the design of the operating waveforms of next-generation T-RAM technologies targeting DRAM-like applications.

### ACKNOWLEDGMENT

The authors would like to thank A. Grossi, R. Bez, E. Camerlenghi, and P. Cappelletti from Micron Technology Inc. for their discussions and support.

### REFERENCES

- [1] V. A. K. Temple, "MOS controlled thyristors (MCT's)," in *IEEE IEDM Tech. Dig.*, 1984, pp. 282–285.
- [2] V. A. K. Temple, "MOS-controlled thyristors—A new class of power devices," *IEEE Trans. Electron Devices*, vol. 33, no. 10, pp. 1609–1618, Oct. 1986.
- [3] F. Nemati and J. D. Plummer, "A novel high density, low voltage SRAM cell with a vertical NDR device," in *Symp. VLSI Technol. Dig. Tech. Papers*, 1998, pp. 66–67.
- [4] F. Nemati and J. D. Plummer, "A novel thyristor-based SRAM cell (T-RAM) for high-speed, low-voltage, giga-scale memories," in *IEEE IEDM Tech. Dig.*, 1999, pp. 283–286.
- [5] F. Nemati *et al.*, "Fully planar  $0.562 \mu m^2$  T-RAM cell in a 130 nm SOI CMOS logic technology for high-density high-performance SRAMs," in *IEEE IEDM Tech. Dig.*, Dec. 2004, pp. 273–276.

- [6] R. Roy *et al.*, "Thyristor-based volatile memory in nano-scale CMOS," in *Proc. IEEE ISSCC*, Feb. 2006, pp. 2612–2621.
- [7] H.-J. Cho *et al.*, "A novel capacitor-less DRAM cell using thin capacitively-coupled thyristor (TCCT)," in *IEEE IEDM Tech. Dig.*, Dec. 2005, pp. 311–314.
- [8] T. Sugizaki *et al.*, "Extremely low-voltage and high-speed operation bulk thyristor-SRAM/DRAM (BT-RAM) cell with triple selective epitaxy layers (TEL)," in *IEEE IEDM Tech. Dig.*, Dec. 2007, pp. 933–936.
- [9] T. Sugizaki *et al.*, "35-nm gate-length and ultra low-voltage (0.45 V) operation bulk thyristor-SRAM/DRAM (BT-RAM) cell with triple selective epitaxy layers (TELS)," in *Proc. Symp. VLSI Technol.*, Jun. 2008, pp. 198–199.
- [10] C. Salling *et al.*, "Reliability of thyristor-based memory cells," in *Proc. IEEE IRPS*, Apr. 2009, pp. 253–259.
- [11] R. Gupta *et al.*, "32 nm high-density high-speed T-RAM embedded memory technology," in *IEEE IEDM Tech. Dig.*, Dec. 2010, pp. 12.1.1–12.1.4.
- [12] A. Z. Badwan, Z. Chbili, Y. Yang, A. A. Salman, Q. Li, and D. E. Ioannou, "SOI field-effect diode DRAM cell: Design and operation," *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 1002–1004, Aug. 2013.
- [13] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A compact capacitor-less high-speed DRAM using field effect-controlled charge regeneration," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 179–181, Feb. 2012.
- [14] U. E. Avci, D. L. Kencke, and P. L. D. Chang, "Floating-body diode—A novel DRAM device," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 161–163, Feb. 2012.
- [15] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Progress in  $Z^2$ -FET 1T-DRAM: Retention time, writing modes, selective array operation, and dual bit storage," *Solid-State Electron.*, vol. 84, pp. 147–154, Jun. 2013.
- [16] H. Mulaosmanovic *et al.*, "Working principles of a DRAM cell based on gated-thyristor bistability," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 921–923, Sep. 2014.
- [17] G. M. Paolucci *et al.*, "Dynamic analysis of current-voltage characteristics of nanoscale gated-thyristors," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 629–631, May 2013.
- [18] H. Mulaosmanovic *et al.*, "Reliability investigation of T-RAM cells for DRAM applications," in *Proc. IEEE IRPS*, Jun. 2014, pp. MY.8.1–MY.8.4.
- [19] W. Shockley and W. T. Read, Jr., "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, Sep. 1952.
- [20] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2090–2098, Sep. 1992.
- [21] M. Aoulaiche *et al.*, "Origin of wide retention distribution in 1T floating body RAM," in *Proc. IEEE Int. SOI Conf.*, Oct. 2012, pp. 1–2.
- [22] H. Mulaosmanovic *et al.*, "Data regeneration and disturb immunity of T-RAM cells," in *Proc. 44th ESSDERC*, Sep. 2014, pp. 46–49.