Modular Architectures of Multistage Switching Networks

Dario G. Garao, Guido Maier, *Senior Member, IEEE*, and Achille Pattavina, *Senior Member, IEEE*

I. Introduction

THE optical implementation of Optical Multistage Switching Networks (OMSNs) has been widely studied by researchers. Several architectures have been studied, proposing various implementations based on different transmission media (including fiber, waveguide and free-space optics) and relying upon various types of components (e.g., MEMS, micro-ring resonators, directional couplers, etc.) used as switching elements.

Recently, research on *Optical interconnections* is casting new light on optical switching, and in particular on OMSNs. *Optical interconnections* is the conventional term that indicates the usage of photonic systems to interconnect several optoelectronic high-speed transmitters and receivers located at short distance from one another. "Short" means in general the range of distances separating subsystems within a system, and the embodiments of such definition encompass a very wide spectrum of applications: rack-to-rack (e.g., inside data-center, supercomputing or top-line switching facilities), shelf-to-shelf (e.g., backplane of a rack of servers or pc blades or card modules), board-to-board (e.g., the bus inside a computer), chip-to-chip (e.g., over a printed-circuit board), on-chip (e.g., interconnecting the cores of a multicore microprocessor). For all these applications, light offers strong advantages over current of electrons as means to propagate information [2], [3]. These are: extremely large bandwidth; attenuation not increasing with frequency; absence of electro-magnetic interference; low cost, high robustness and small footprint of the transmission media; low power consumption; etc. Such advantages can be better exploited if also switching is carried out optically, possibly integrated with electronic buffering.

The desired interconnection architecture should be *flexible* with reference to: (a) target application, (b) network topology, (c) adopted technology. As for item (a), the vast range of applications of optical interconnections demands for fabric architectures that are applicable to different interconnection scale, from the intra data-center infrastructure for the new cloud applications [4]–[6] to the sub-millimetric System-on-Chip (SoC) and Network-on-Chip (NoC) [7]–[9]. With regards to the selection of network topology (b), the procedure should allow the designer to add switching stages in a modular way and to configure the interstage-link patterns according to the degree of network connectivity (e.g., blocking network, rearrangeable/strictly non-blocking network, etc.) needed by the application. W. r. t. item (c), the architectures should be little dependent, or invariant if possible, to the implementation technology selected for the optical switching elements and for the links between stages. The approach we are going to describe here is in some aspects similar to a well known method adopted in Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI) integrated circuit design, that is the Thompson grid model [10].

After a comparative review of the literature on the subject (Section II), this paper proposes a novel design approach of interconnection networks (Sections III–V) that faces the three above aspects, (a–c), of design flexibility. This design procedure does not set any specific constraint on the network size $N \times N$, making it suitable to a vast set of use cases (a). Section VI applies the design procedure to examples of either blocking or rearrangeable interconnection networks (b). Section VII explains how electronic technologies can exploit our design approach (c), duly taking into account specific technological constraints.

Manuscript received June 11, 2013; revised October 10, 2013, February 21, 2014, and June 19, 2014; accepted July 17, 2014. Date of publication July 29, 2014; date of current version September 19, 2014. This paper was presented in part at IEEE INFOCOM, Torino, Italy, April 2003. The associate editor coordinating the review of this paper and approving it for publication was C. Assi.

The authors are with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan 20133, Italy (e-mail: dario.garao@polimi.it; guido.maier@polimi.it; achille.pattavina@polimi.it).

Color versions of one or more of the figures in this paper are available online.

II. Optical Multistage Switching Networks

There are recent works proposing OMSN design techniques, some similar to the direct implementation of the architectures known from the classical switching theory, some others developed ad-hoc for optics. These works are interesting but rather generic about the physical interconnection of the stages and the switching elements [11], [12]. Other studies have proposed solutions not compatible with an integrated-optics implementation [13]–[15]. Some papers appeared in 2004 [16] and 2008 [17] present architectures developed for MEMS switching elements. More recent studies deal with multistage network architectures exploiting waveguides and micro-ring resonators [18], [19]. Most of these papers focus on networks of specific size, without caring too much about the scalability of the proposed architectures. An example of scalability study of MEMS matrices is presented in [20]. However, in this work, as in the others cited so far, the proposed architecture is a direct implementation of classical switching networks (e.g., Benes).

Novel optically-oriented architectures for OMSN have been introduced in the 80's and 90's [21]–[23], exploiting directional couplers as switching elements. Also these works are more focused on the topology and are not very specific on the interconnection layout. A first paper investigating the modularity of an integrated-optics architecture based on directional couplers [24], appears in 2000: in the work a recursive design technique is proposed. In 2001, another similar study [25] reports a recursive technique to design the stages of a multistage network, independently on the technology of the switching elements; little attention is however dedicated to the interconnection of the stages. Meanwhile, in [26] an analogous approach is adopted to design MEMS-based stages.

We can classify the cited works into these categories:

- Topology specific, in which the architecture can be implemented with many different switching technologies, but it can be configured only for a specific network topology and/or for a specific number of inlets/outlets;
- Technology specific, in which the architecture can be embodied in many different switching network topologies, but it can be implemented only by a specific switching-element and link technology.

Indeed, to the best of our knowledge, all the past papers in OMSNs-related literature fall within one of the two categories or in both of them.

Our proposal is innovative compared to the past literature since it addresses the following targets at the same time: it is compatible with different optical and even non-optical implementation technologies and it allows to design the layout of a vast class of switching networks. Our work deals both with internal stage architecture and interconnections between stages, allowing a highly-modular implementation of the network. The design is the result of a systematic analysis of the properties of multistage switching architectures. By exploiting the concept of module, in this paper we show how such systematic approach leads to a flexible design of a vast class of multistage topologies, including all the banyan networks and the EGS networks [27].

The modules are easily configurable. Each module is defined according to the internal stage structure and to the connectivity properties of the corresponding stage in a specific network architecture. By cascading a number of properly configured modules, we can obtain the layout of the overall desired multistage architecture. This layout can be used as blueprint for the physical implementation of the network. Although the switching modules are only similar, not exactly identical, this reduces the implementation complexity in building large optical switches.

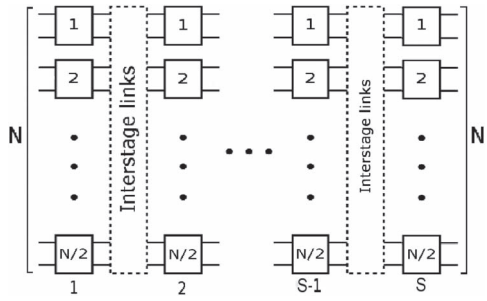

Fig. 1. General scheme of a multistage network.

In order to simplify the discussion we will refer to a planar implementation, in which optical signals propagate (in waveguides or free-space) over a plane parallel to the substrate of the network over which the switching elements are fabricated. The planar layout is also common to non-optical technologies as for instance electronic Integrated Circuit (IC) technology. Being the approach of our technique very general, we will briefly discuss the possibility of applying the proposed technique to the electronic case. Wavelength division multiplexing (WDM) is not considered here, due to space limitations, though it can be potentially adopted in the proposed OMSNs.

III. Multistage-Network Basic Definitions and Decomposition

As well known from the switching theory [27], a *multistage network* is composed by elementary switching elements (SEs) organized as a sequence of switching element stages (SESs), interconnected by interstage links. Here only networks with 2×2 switching elements (SEs) are considered, each element having only two possible states: bar and cross. The links between two adjacent switching stages form an *interstage-link pattern* (ILP). We will consider only networks with N inlets and outlets $(N \times N)$ with S switching stages, numbered from 1 to S and $N/2$ SEs per stage. The number of interstage-link patterns is $S-1$, numbered after the upstream switching stage (see Fig. 1).

The routing, blocking and reachability properties of a multistage network depend on the number of SESs and the connection patterns built in the ILPs. Both SESs and ILPs perform *permutations*. In general, an $N \times N$ stage performs a permutation $o = \eta(i)$ by mapping its inputs $i = \{0, N-1\}$ one-to-one over its outputs o, with $0 \leq o \leq N-1$. The *identity* permutation I occurs when $\eta(i) = i \, \forall \, i$. The permutation performed by two adjacent stages is the *cascade* of the permutations of each single stage, i.e., $\eta_1\eta_2 = \eta_2[\eta_1(i)]$, if η_1 and η_2 are the two individual permutations. The relation $\eta I = I\eta$ always holds, but in general the commutative property does not hold, and thus $\eta_1\eta_2 \neq \eta_2\eta_1$.

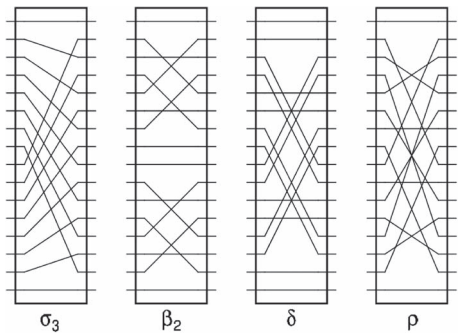

Fig. 2. Examples of interstage link permutations.

An SES performs a *switching permutation* π which changes over time according to the network state, while an ILP performs a fixed *interstage permutation* μ. Thus the overall permutation of a multistage network can be written as

$$\pi_1\mu_1\pi_2\mu_2\cdots\pi_{S-1}\mu_{S-1}\pi_S = \pi_S\left(\mu_{S-1}\left(\pi_{S-1}\left(\cdots\left(\mu_1\left(\pi_1(i)\right)\right)\right)\right)\right).$$

The switching theory has identified a number of interstage permutations that can be effectively used as basic building blocks in the construction of multistage networks. These networks are classified on the basis of the type of μ they adopt in their ILPs. Two basic types of ILP can be identified [27]: the Extended Generalized Shuffle (EGS) permutation and the *bit-exchanging* permutations.

In this paper we will deal only with this latter type, though the method we describe is quite general and it can be applied also to EGS permutation (as mentioned later on). The well-known banyan networks are all based on bit-exchanging permutation ILPs. In bit-exchanging permutations, N is an integer power of 2 ($N = 2^n$) and thus inlets (outlets) of a generic stage are identified by a binary address of type: $a = a_{n-1}a_{n-2}\cdots a_0$ ($a_j = 0, 1$), where a_{n-1} is the most significant bit. The inlet of stage s with address $i_{n-1}i_{n-2}\cdots i_0$ is connected to the outlet of s with address $o_{n-1}o_{n-2}\cdots o_0 = f\left(i_{n-1}i_{n-2}\cdots i_0\right)$, where f indicates an operator that scrambles the bits (i.e., exchanges the position of one or more bit) in a prefixed order.

For the construction of the different banyan network topologies the following bit-exchanging permutations are defined [27]:

- $\sigma_h(i_{n-1}\cdots i_0) = i_{n-1}\cdots i_{h+1}i_{h-1}\cdots i_0 i_h$
- $\sigma_h^{-1}(i_{n-1}\cdots i_0) = i_{n-1}\cdots i_{h+1}i_0 i_h\cdots i_1$
- $\beta_h(i_{n-1}\cdots i_0) = i_{n-1}\cdots i_{h+1}i_0 i_{h-1}\cdots i_1 i_h$
- $\delta(i_{n-1}\cdots i_0) = i_1 i_2\cdots i_{n-1}i_0$
- $\rho(i_{n-1}\cdots i_0) = i_0 i_1\cdots i_{n-2}i_{n-1}$
- $I(i_{n-1}\cdots i_0) = i_{n-1}i_{n-2}\cdots i_0$

where $(0 \le h \le n-1)$. Fig. 2 shows σ_3, β_2, δ, and ρ with $N = 16$.

Permutations σ_h and σ_h^{-1} are called *h-shuffle* and *h-unshuffle*, respectively, as they are one the mirror of the other. If $h = n-1$, the two permutations are named *perfect shuffle* (σ) and *perfect unshuffle* (σ^{-1}). The β permutation is called *butterfly*, the δ and the ρ are known as *bit-switch* and *bit-reversal*, respectively, while I is the *identity*. It can be easily seen that $\sigma_0 = \sigma_0^{-1} = \beta_0 = I$.

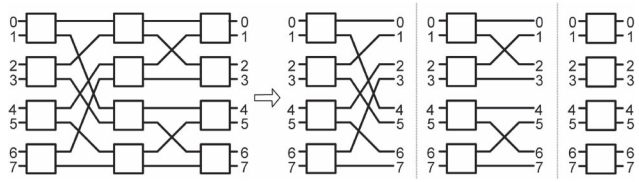

Fig. 3. Multistage network decomposition in SuSs.

The family of bit-exchanging permutations can be further divided into two classes, according to the property of preserving or not preserving the parity of the inlet in the input-output mapping. Formally, if $o_{n-1}o_{n-2}\cdots o_0 = f(i_{n-1}i_{n-2}\cdots i_0)$ is the permutation, then:

- the permutation is *parity-preserving* if $o_0 = i_0\ \forall\, i$;
- the permutation is *non parity-preserving* otherwise.

Observation 1: Bit-switch and identity permutations are parity-preserving, while shuffle, unshuffle, butterfly and bit-reversal are non parity-preserving.

In this paper we restrict the illustration of our method only to bit-exchanging permutations that are non parity-preserving (for short, named NPBP in the following), not due to lack of generality, but just for space limitations. In fact the method is applicable to all banyan networks, but for those based on parity-preserving permutations ad-hoc theorems are needed which would require a text extension to be covered.

Let us now introduce a final concept we need for the following discussion. We define a *superstage* (SuS) as the set composed by the cascade of a switching stage and the following adjacent interstage-link pattern. In a multistage network of S stages, in which π_s (μ_s) is the permutation of the generic SES (ILP), the SuS permutation is given by

$$\omega_s = \begin{cases} \pi_s\mu_s & \text{for } 1 \le s \le S-1 \\ \pi_s & \text{for } s = S. \end{cases}$$

In order to describe a SuS, and without loss of generality, in the following we will assume that the SES permutation is the identity: $\pi_s = I$. This is equivalent to consider all the switching elements in the bar state and it implies that all connections between SuS inlets and outlets are arranged as the links of the ILP. This artifice will be useful to simplify the explanations of the optical SuS in Section IV.

Any multistage network can be decomposed in a cascade of SuSs, as shown in Fig. 3 for the case of an 8×8 network with shuffle ILPs. Dually, we can create a multistage network by cascading SuSs. These two statements seem obvious at a first glance, but they will gain a more substantial meaning when the optical implementation will be introduced. The cascadability of SuSs is made possible by their layout, chosen so that the outlets of a first SuS spatially matches with the position of the inlets of the following SuS. This property is essential to make the architecture *modular*, i.e., decomposable in elementary building-blocks.

IV. Optical Superstage Architecture

This section defines the general properties of the architecture we propose for implementing multistage networks with optical

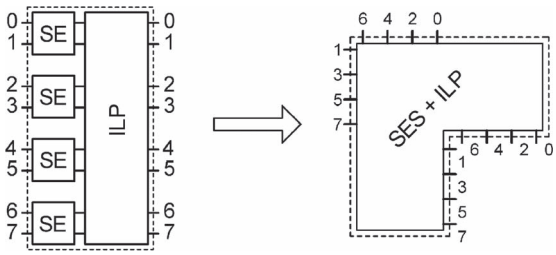

Fig. 4. Optical SuS layout.

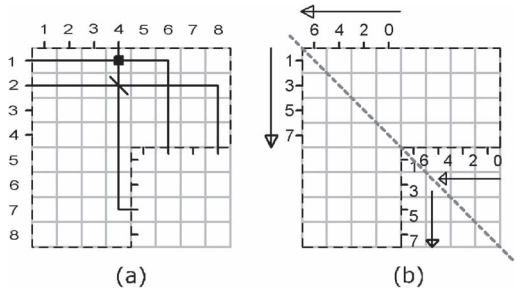

Fig. 5. Substrate grid with (a) three optical paths and (b) SuS inlets and outlets.

technology, as anticipated in Section I. The basic idea is to exploit the SuS definition reported above in order to decompose the network in a set of simple building blocks which can be easily cascaded and which have a similar layout. Each block corresponds to a SuS and its internal architecture can be modified so to reproduce the SES and ILP of the SuS.

According to the definition of an $N \times N$ SuS, its optical implementation has to contain a set of N inlets, a set of N outlets and $N/2$ optical 2×2 switching elements. The role of the interstage links is played by the optical paths connecting inlets to outlets of a SuS. As mentioned in Section I, the path can be free-space optical or wave-guided, matching the fabrication technology of the switches. The following discussion is independent of the specific implementation: it will show how to design the optical SuSs so that they display the same switching properties and perform the same permutations as defined by the theory. Moreover, modularity has to be preserved, so to be able to assemble an OMSN by cascading the SuS modules. Therefore, the plan of the optical SuS and the location of inlets and outlets is selected in order to guarantee matching of outlets of a SuS to inlets of the next adjacent SuS, as explained in Section III.

We are proposing a physical layout of an optical SuS with a "Γ" shape as shown in Fig. 4. The "Γ" shape ensures modularity and enables a simple and uniform design of the optical paths.[1]

A useful tool to represent the SuS layout and its internal architecture is provided by the *substrate grid* represented in Fig. 5 (in the case $N = 8$). The grid has size $N \times N$, with columns and rows numbered from 1 to N; the SuS is inscribed in this grid: due to the "Γ" shape, the lower-right quarter of the grid is unused. Row height and column width are equal to the same size, that we call *base unit*. Three sample optical paths are shown in Fig. 5(a) in order to give a quick idea of the internal structure of the SuS. Optical paths are composed only of vertical or horizontal segments joined by 90-degrees turns. Each element of the grid identified by the position (*row*, *column*) can be only of a finite number of types: horizontal straight segment (e.g., (1, 1) in the grid), vertical straight segment (e.g., (4, 4)), left turn[2] (e.g., (7, 4)), right turn (e.g., (2, 8)), turn pair[3] (e.g., (2, 4)), path crossing intersection (at 90°) (e.g., (2, 6)) and path crossing intersection with an optical 2×2 switching device[4] (that is supposed to have the two states cross and bar) (e.g., (1, 4)). In this work we do not consider wavelength division multiplexing: all signals are at the same wavelength. Therefore the following conflict-prevention rule must be enforced: every non empty element of the substrate grid can be occupied either by a single input-to-output optical path segment or by two input-to-output optical path segments with different direction.

The rest of this section explores in detail the aspects of SuS planning, which are:

- inlet and outlet placement,
- type of optical path,
- positioning of the optical switching elements.

A. Inlet/Outlet Placement

Inlets and outlets of the optical SuS are positioned as represented in Fig. 5(b). They are partitioned according to their parity and the distance between two adjacent inlets (outlets) is equal to the base unit. Even inlets, starting from inlet 0, are placed at the edge of the top row, from column $N/2$ to column 1; odd inlets, starting from inlet 1, are placed at the edge of the leftmost column, from row 1 to row $N/2$. The inlets have been numbered so that inlets 0 and $N-1$ are symmetrical relative to the main diagonal of the grid (see Fig. 5(b)).[5] Outlets are placed in positions which match the position of the inlets of the next SuS: odd outlets are located at the edge of column $N/2$, from row $N/2+1$ to row N; even outlets are at the edge of row $N/2$, from column N to column $N/2+1$. Fig. 6 shows an example of a OMSN built by cascading three 8×8 SuSs.

B. Optical Paths

We require that optical paths have to connect inlets to outlets along the shortest possible route. In fact by reducing the distance traveled by light inside the module, we also reduce

[1] An OMSN could be decomposed in single stages in different ways. The "Γ" shape has been chosen as it is simple and easily identifiable. Other shapes may be chosen without affecting the generality of the proposed mathematical analysis, provided that they ensure modularity and arrangement of optical paths in orthogonal patterns. For further explanation see Appendix A.

[2] Turns are implemented by fixed mirrors in case of free-space optics and by bended waveguides in integrated optics.

[3] The diagonal segment represents a double-faced mirror (or a pair of 90° bends) to indicate that both the optical paths change direction.

[4] Represented as a solid black square.

[5] The proposed inlet/outlet placement descends from the "Γ" shape selected for the SuS. If other shapes are chosen, positions may have to be redefined accordingly, but without affecting the generality of the proposed method, provided that symmetry with respect to the main diagonal of the grid is preserved. Also note that even/odd positioning of inlets/outlets can be reversed, if that is done for all the SuS.

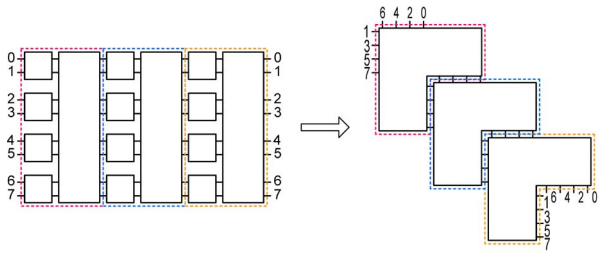

Fig. 6. Three-stage network with corresponding SuS implementation.

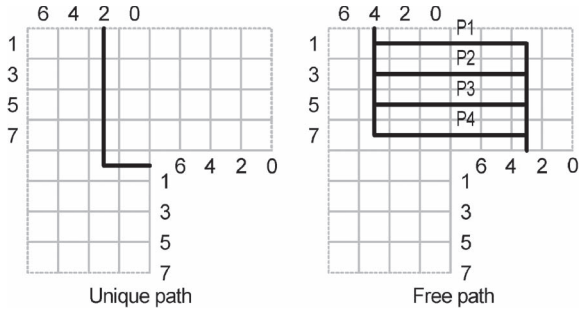

Fig. 7. Optical path types.

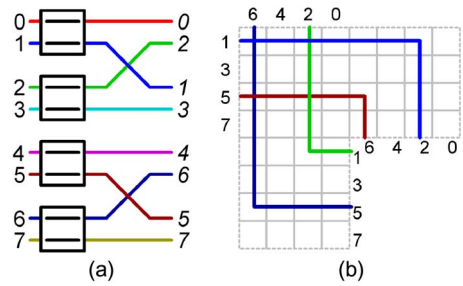

Fig. 8. *1-shuffle* SuS: (a) NPBP and (b) unique paths.

the number of path turns and thus the loss (due to bending or reflection on non-ideal mirrors).

As shown in Fig. 7, when an even (horizontal) inlet is connected to an odd (vertical) outlet, the simplest and shortest possible path is composed only by two segments and one turn. The same applies to a connection between an odd (vertical) inlet and an even (horizontal) outlet. These are named *unique paths* since one single path exists, once the inlet-outlet pair $[i, o]$ to be connected is selected. If the inlet i is even (odd), the first segment of the path will lay on the column (row) c_i (r_i) and the second segment will lay on the row (column) r_o (c_o).

When the inlet and the outlet to be connected have the same parity (i.e., both are odd or even), the shortest possible path is composed of three segments and two turns. In this case, however, there are multiple paths, all with the same length, as visible in Fig. 7. Therefore there is a degree of freedom in the selection of the path: we introduce then the name *free paths*. If the source inlet is even (odd) the free path is described by (c_i, r_t, c_o) $((r_i, c_t, r_o))$; r_t $(1 \leq r_t \leq N/2)$ and c_t $(1 \leq c_t \leq N/2)$ indicate the row and column, respectively, selected for placing the central segment. The paths are named horizontal or vertical based on the orientation of their longest segment, which is the first one for the unique paths and the middle one for the free paths. In Section V we will define the criterion to select the best possible central-segment position in the free paths.

Observation 2: All SuS bit-exchanging permutations have at least two free paths implementing the links [0, 0] and $[N-1, N-1]$.

In fact the two links are obviously parity preserving, and thus correspond to free paths.

Theorem 1: In a SuS implementing an NPBP (NPBP-SuS), the number of unique paths is $N/2$.

Proof: The number of unique paths is given by the number of non parity-preserving connections in a SuS (or in the μ permutation of its ILP). The parity of inlet i is given by the value of its least significant bit (LSB) i_0 (even when $i_0 = 0$, odd when $i_0 = 1$). By definition of NPBP (see Section III), we know that i is to be connected to $o = \mu(i)$, with LSB $o_0 = i_k$ where $1 \leq k \leq n-1$. There are four possible cases:

i_0	o_0	Parity change
0	0	no
0	1	yes
1	0	yes
1	1	no

These four cases uniformly partition the set of $N = 2^n$ possible binary n-bit combinations representing the N inlets. In fact, let us consider the matrix (with N rows and n columns) displaying all the input addresses i encoded in their binary form. i_0 is the last column of such a matrix, while i_k (and thus o_0) is another column. For each one of the pairs $[i_0, o_0]$ reported in the table above, we have to compute how many rows of the matrix exist containing that pair. This is equivalent to counting the number of different strings of n bits when the value of two of them is fixed: there are $2^{n-2} = N/4$ different strings for each case. Thus the number of parity-changing connections is $N/4 + N/4 = N/2$. As a consequence, this is also the number of parity-preserving connections. □

Corollary 1: The set of $N/2$ unique paths includes $N/4$ vertical and $N/4$ horizontal unique paths. Moreover, unique paths can never generate conflicts between themselves.

The proof is rather trivial and it will be omitted here for brevity.

Let us introduce the free-path discussion with an example. Fig. 8 shows the optical implementation of a σ_1 SuS with $N = 8$ in which all the unique paths have been already routed.

We consider one of the remaining connections that are still to be routed, for example the free path originating from inlet $i = 0$ which in a σ_1 is connected to outlet $o = 0$. We recall that this is the three-segment path $(c_i = N/2, r_t, c_o = N)$. According to the conflict-prevention rule (see above), no element of the substrate grid can be occupied by two co-propagating optical paths. Thus, the choice of row r_t where to position the central segment is constrained by the presence of the horizontal unique paths already established in the substrate grid. Out of $N/2 = 4$ possible choices, there are actually only 2 positions available $(r_t = \{2, 4\})$, as shown in Fig. 9. The selection of the free path [0, 0], on its turn, sets an additional constraint on the selection of the next free path. Fig. 9 represents the consequence of the routing decision for connection [0, 0] on the path [4, 4].

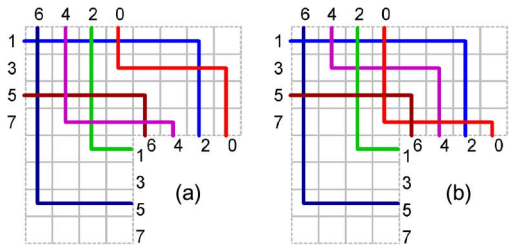

Fig. 9. Possible configurations of the free paths [0, 0] and [4, 4].

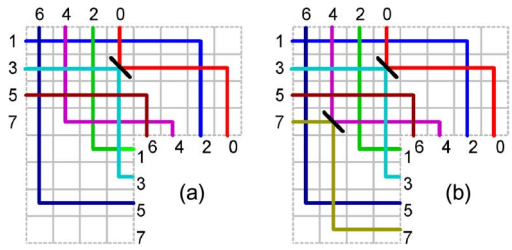

Fig. 10. Vertical free path routing: (a) path [3, 3] and (b) path [7, 7].

The example is generalized as follows. From Theorem 1 it follows immediately:

Theorem 2: In an NPBP-SuS, the number of free paths is $N/2$.

Corollary 2: The set of the $N/2$ free paths includes $N/4$ vertical and $N/4$ horizontal free paths.

Then we have the following:

Theorem 3: There are $(N/4)!$ possible configurations of the $N/2$ free paths.

Proof: First, let us observe that horizontal (vertical) free paths can potentially conflict with other horizontal (vertical) free paths and with horizontal (vertical) unique paths; any possible conflict of this kind concerns only the central segment of the free path.

Without loss of generality, let us start by routing the set of horizontal free paths. The first free path of the set has only $N/4$ possible routings out of $N/2$, due to the presence of the horizontal unique paths; once the first path has been established, for the second horizontal free path there are only $(N/4)-1$ alternatives; for the next free paths, $(N/4)-2$ possibilities, and so on, until the last $N/4$-th horizontal free path for which only a single route will be available.

This is the situation depicted in Fig. 9. Clearly, the described assignment of the horizontal free paths can be performed in $(N/4)!$ different ways.

Once horizontal free paths have been established, we shall move to the vertical free paths. Thus, we start from a substrate grid occupied by all horizontal free and unique paths and vertical unique paths. Let (r_i, c_t, r_o) be the topmost vertical free path yet to be set up. Row r_i contains at this moment $N/4$ elements crossed by vertical segments of the established horizontal unique paths. Moreover, there will be one and only one already established horizontal free path with $r_t = r_i$. Let this path be (c_j, r_i, c_u): then element (r_i, c_j) will contain the turn of the path, while elements of r_i at its right will also host the central segment of (c_j, r_i, c_u). Finally, all the other $(N/4)-1$ horizontal free paths cross r_i without deviation, and thus occupy an equal number of r_i elements with their vertical segments. In such conditions, to avoid any conflict, there is only one possible position for the column c_t of the central segment of (r_i, c_t, r_o): that is $c_t = c_j$. All the other positions are forbidden as they would cause conflict between vertical segments. Thus the free path is configured and the element (r_i, c_j) is transformed from a turn to a pair of turns. Fig. 10(a) shows the single possible configuration of path [3, 3] in σ_1.

Now let us consider the second-topmost vertical free path yet to be set up. This path meets the same conditions described for the topmost one, with the only difference that the total number of vertical paths crossing the row is $(N/4)+(N/4)-2$. But now we have to take into account a new forbidden column c_j occupied by the descending vertical segment of the first vertical free path. Thus also for the second vertical free path there is only one possible configuration. Fig. 10(b) shows the constrained routing of path [7, 7] in the σ_1 example.

This reasoning can be repeated for all the other vertical free paths, proving that, in conclusion, once all the horizontal paths are configured, the vertical ones are also decided. That concludes the proof (which could obviously be repeated the same configuring vertical paths first). □

We will show that not all the $(N/4)!$ possible configurations of the $N/2$ free paths are actually suitable to create an optical SuS.

C. Optical Switching-Element Location

In the SES of an $N \times N$ SuS there are $N/2$ 2×2 SEs. SE k $(0 \le k \le (N/2)-1)$ of the SuS is connected to inlets $2k$ and $2k+1$. Thus the optical device implementing the SE has to be placed at the crossing points of the paths coming from inlets $2k$ (even) and $2k+1$ (odd), respectively. We recall that a path from an inlet is of the unique type if it changes inlet parity, while it is of the free type if it preserves the parity.

Theorem 4: In an NPBP-SuS, the paths originating from the pair of adjacent inlets $2k$ and $2k+1$ $(0 \le k \le (N/2)-1)$ are one free and one unique.

Proof: Let us recall the binary matrix mentioned in the proof of Theorem 1. The assumption that the permutation is not parity-preserving implies that after the permutation the last column of the matrix (representing the least significant bit) must be substituted by some other columns of the matrix. Before the permutation, the last column was a string of 0 and 1 alternated. In all the other columns of the matrix the elements of two adjacent rows $2k$ and $2k+1$ have always the same value (00 or 11), for any k. Thus, each pair of inlets $2k$ and $2k+1$, having as LSB (0, 1), respectively, are connected to a pair of outlets having as LSB either (0, 0) or (1, 1). Therefore, one path always changes the parity, while the other preserves it. □

Theorem 5: In an NPBP-SuS, the paths originating from the pair of adjacent inlets $2k$ and $2k+1$ $(0 \le k \le (N/2)-1)$ either do not intersect each other or intersect twice.

Proof: Let us assume without loss of generality that from inlet $2k$ stems the unique path, while from inlet $2k+1$ starts the free path $(2k+1, r_i, c_o)$. Fig. 11 shows four different configurations of the free path (a, b, c, d) which originate all the four possible scenarios of intersection with the unique path. The

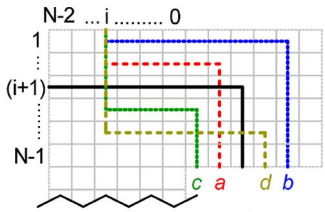

Fig. 11. Possible intersecting points between unique and free paths.

position of the crossing points depends on the position of the intermediate horizontal segment r_i and of the vertical segment c_o of the free path. While c_o is dictated by the permutation, r_i can be chosen. The following Lemma 1 proves that scenarios a and c can never occur, thus proving this theorem. □

Lemma 1: In an NPBP-SuS in which inlets $2k$ $(0 \leq k \leq (N/2)-1)$ and $2k+1$ are connected to outlets o_1 and o_2, respectively, then o_1 lays on a column (row) having greater (smaller) index than the column (row) occupied by o_2.

Proof: To simplify notation, we assume $i = 2k$. Inlet i $(i+1)$ is connected to outlet $\mu(i)$ $(\mu(i+1))$, according to NPBP μ. As stated before, the outlets of the SuS are sorted with the same rule of the inlets. Given that, we only need to prove that $\mu(i) < \mu(i+1)$. In that case, in fact, the index of the column (row) of outlet $\mu(i)$ is greater (smaller) than the index of the column (row) of outlet $\mu(i+1)$.

The binary representation of the input of the μ NPBP is:

$$\begin{cases} (i)_2 = i_{n-1} \cdots i_1 i_0 \\ (i+1)_2 = i_{n-1} \cdots i_1 \overline{i_0}. \end{cases}$$

The LSB will be shifted by the permutation in a new position h $(1 \leq h \leq N-1)$. Then the output will be:

$$\begin{cases} (\mu(i))_2 = o_{n-1} \cdots o_h \cdots o_0 \\ (\mu(i+1))_2 = o_{n-1} \cdots \overline{o_h} \cdots o_0. \end{cases}$$

Let us switch to the decimal representation:

$$\mu(i) = \sum_{i=h+1}^{n-1} o_i 2^i + o_h 2^h + \sum_{i=0}^{h-1} o_i 2^i,$$

$$\mu(i+1) = \sum_{i=h+1}^{n-1} o_i 2^i + \overline{o_h} 2^h + \sum_{i=0}^{h-1} o_i 2^i.$$

Since i is even, then $i_0 = o_h = 0$ and $\overline{i_0} = \overline{o_h} = 1$, hence

$$\mu(i) = \sum_{\substack{i=0 \\ i \neq h}}^{n-1} o_i 2^i \quad \text{and} \quad \mu(i+1) = \sum_{\substack{i=0 \\ i \neq h}}^{n-1} o_i 2^i + 2^h,$$

thus $\mu(i) < \mu(i+1)$ for i even. □

In conclusion, we have proven that it is always possible to configure the paths in a way such that the pair of paths from inlets $2k$ and $2k+1$ intersects twice. One of the intersections occurs in the element $(r_i(2k+1), c_i(2k))$ of the substrate grid: in this element we can locate the optical SE. From the inlet layout it descends that the set of SEs of the SuS occupies the secondary diagonal of the subgrid $N/2 \times N/2$ with origin in (1, 1), as shown in Fig. 12.

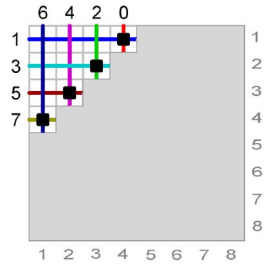

Fig. 12. Switching-element locations.

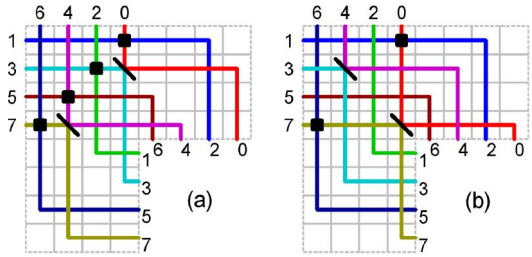

Fig. 13. Feasible (a) and unfeasible (b) configuration for placing SEs.

V. Optical Superstage Design Rules

We stated that not all the $(N/4)!$ possible configurations of the free paths lead to an implementable optical SuS. For example, Fig. 13 shows the final result of the path configuration of the 8×8 σ_1 SuS initiated in Fig. 9 in the two possible ways. The solution shown in Fig. 13(a) is actually implementable, since the paths generate the four crossing points suitable to locate all the four SEs of the SuS. On the other hand, Fig. 13(b) shows that only two crossing points are generated by the path-pairs originating from inlets $(2k, 2k+1)$: thus there are not enough sites to accommodate all the SEs.

Thus we need to define a systematic design strategy for a correct construction of the optical SuS.

Theorem 6: An implementable optical SuS is generated if the following rule is adopted to configure the horizontal free paths from the even inlets (after having set up the unique paths).

1) Configure the free paths in sequence in order of increasing inlet.
2) For each horizontal free path, select the first topmost central segment available; i.e., set the central segment on the row with the least possible index.

Proof: This theorem provides a *sufficient condition*, i.e., there may be other configuration policies leading to implementable SuSs as well, but we are stating that at least *these* particular rules are effective. For proving the theorem we need to show that by applying the rules, the configuration of paths is such that it originates crossing points between the paths distributed as in Fig. 12 in every NPBP-SuS.

For this proof, the destinations of the connections are irrelevant, as it will be clear later on. Thus in this proof let's focus only on the substrate grid reduced to the upper-left quarter with $1 \leq r \leq (N/2)$ and $1 \leq c \leq (N/2)$ (see Fig. 14).

Let consider a generic NPBP-SuS where all the unique paths are already generated. Let $I = \{0, 1, 2, \ldots, N-2, N-1\}$ be the tuple of the inlets, $I_E = \{0, 2, \ldots, N-2\}$ the tuple of

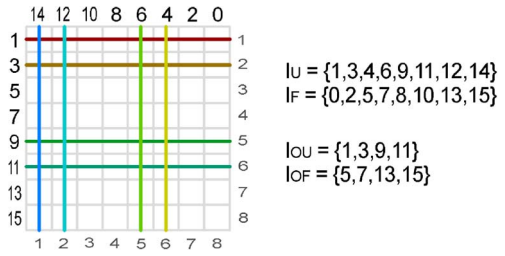

Fig. 14. Subgrid of a 16 × 16 2-shuffle with unique paths only (I_U).

the even inlets, $I_O = \{1, 3, \ldots, N-1\}$ the tuple of the odd inlets, $I_F = \{i_F\}$ the tuple of the inlets with a free path and $I_U = \{i_U\}$ be the tuple of the inlets with a unique path. Let $I_{EF} = I_F \cap I_E = \{i_{EF}\}$ be the tuple of the even inlets with a free path, $I_{OF} = I_F \cap I_O = \{i_{OF}\}$ the tuple of the odd inlets with a free path, $I_{EU} = I_U \cap I_E = \{i_{EU}\}$ the tuple of the even inlets with a unique path and $I_{OU} = I_U \cap I_O = \{i_{OU}\}$ the tuple of the odd inlets with a unique path. Let $R = \{1, 2, \ldots, (N-1)/2, N/2\}$ be the tuple of the rows of the substrate grid, $R_u = \{r_u^{(i)} = (i+1)/2\}$ the tuple of the rows occupied by the initial segment of the (unique) paths of the inlets $i \in I_{OU}$, $R_f = \{r_f^{(i)} = (i+1)/2\}$ the tuple of the free rows, corresponding to the rows of the inlets $i \in I_{OF}$, and $r_t^{(i)}$ the row where the central segment of the (free) paths of the inlets $i \in I_{EF}$ will be placed. We clearly have $R = R_f \cup R_u$ and $r_t \in R_f$.

The condition to originate the crossing points between the inlet pair $(2k, 2k+1)$ can be derived from path d of Fig. 11 (path a and c can never occur by Theorem 5): the central segment of the free path of inlet $2k$ must be placed in a free row (r_f) with a index greater than the index of the row where the initial segment of the unique path of inlet $(2k+1)$ is placed (r_u). This condition must be satisfied for every inlet pair $(2k, 2k+1)$ with $2k \in I_{EF}$, $(2k+1) \in I_{OU}$. Thus

$$\forall\, i_{OU}\ \exists i_{EF} :\ r_t^{(i_{EF})} > r_u^{(i_{OU})},$$

namely (because $r_t \in R_f$)

$$\forall\, i_{OU}\ \exists i_{OF} :\ r_f^{(i_{OF})} > r_u^{(i_{OU})},$$

namely (because of the definition of $r_f^{(i)}$ and $r_u^{(i)}$)

$$\forall\, i_{OU}\ \exists i_{OF} :\ i_{OF} > i_{OU}.$$

Let the tuples of the odd inlets be:

$$\begin{cases} I_{OU} = \left\{ i_{OU}^{(j)} \right\} & \text{with} \quad i_{OU}^{(j)} < i_{OU}^{(j+1)} \\ I_{OF} = \left\{ i_{OF}^{(j)} \right\} & \text{with} \quad i_{OF}^{(j)} < i_{OF}^{(j+1)}. \end{cases}$$

To prove this theorem we have to prove that at least $i_{OF}^{(j)} > i_{OU}^{(j)}\ \forall\, j$, namely the central segment of every free path must be placed in the first free row still available.

The binary representation of the generic odd inlet i is:

$$(i)_2 = i_{n-1} i_{n-2} \cdots i_1 1,$$

then the binary representation of a generic permutation $\mu(i)$ (of odd inlet i) will be:

$$(\mu(i))_2 = o_{n-1} \cdots o_{h+1} 1 o_{h-1} \cdots o_0 (n-1 \le h \le 1).$$

Owing to the definition of unique and free path, the representations of the generic permutation $\mu(i_{OU})$ and $\mu(i_{OF})$ are:

$$(\mu(i_{OU}))_2 = o_{n-1} \cdots o_{h+1} 1 o_{h-1} \cdots 0,$$
$$(\mu(i_{OF}))_2 = o_{n-1} \cdots o_{h+1} 1 o_{h-1} \cdots 1;$$

then the representations of the generic inlet i_{OU} and i_{OF} are:

$$\left(i_{OU} = \mu^{-1}\left(\mu(i_{OU})\right)\right)_2 = i_{n-1} \cdots i_{h+1} 0 i_{h-1} \cdots i_1 1,$$
$$\left(i_{OF} = \mu^{-1}\left(\mu(i_{OF})\right)\right)_2 = i_{n-1} \cdots i_{h+1} 1 i_{h-1} \cdots i_1 1.$$

Switching to the decimal representation:

$$i_{OU} = \sum_{\substack{l=1 \\ l \neq h}}^{n-1} i_l 2^l + 1, \quad i_{OF} = \sum_{\substack{l=1 \\ l \neq h}}^{n-1} i_l 2^l + 2^h + 1.$$

The two inlet classes above differ from each other only for the bit in position h, thus if the odd inlet tuples are generated as a increasing succession (as it is) then:

$$i_{OF}^{(j)} > i_{OU}^{(j)} \quad \forall\, j.$$

□

Let us display the example of a 16 × 16 perfect-unshuffle. Beginning from unique paths already established, we start configuring the horizontal free paths from the one originating from the lowest inlet, which in this case is the path [0, 0]. Fig. 15(a) shows the four alternatives P1, P2, P3, and P4. According to the criterion mentioned above, we chose P1. The second inlet to consider is 4: here we have three choices (P1, P2, P3) (Fig. 15(b)). Again, P1 is selected. Finally, the selection is repeated for the two alternatives P1 and P2 for the path from 8 (Fig. 15(c)), to end up with the path from 12, which has only one possible routing (Fig. 15(d)). The rest of free paths (i.e., paths from inlets 3, 7, 11, and 15), as explained, are then constrained. We observe that all needed crossing points are lined up in the diagonal of the top-left subgrid, ready to host the SEs (Fig. 15(e)).

We finally deal with a last detail. In an OMSN decomposed in SuSs the last SuS simply implements the identity permutation (see Fig. 3). This terminal SuS can be more effectively designed according to an ad-hoc procedure, derogating from the one described above for the other SuSs. In fact the terminal SuS can be simplified, since there is no need to connect it to a further stage. Fig. 16 represents the terminal SuS.

VI. Design Procedure of Optical Multistage Networks

Based on the discussion above, the design procedure of the architecture of an OMSN can be summarized as follows:

1) consider the multistage network represented as a sequence of SESs and ILPs ("classical" representation);

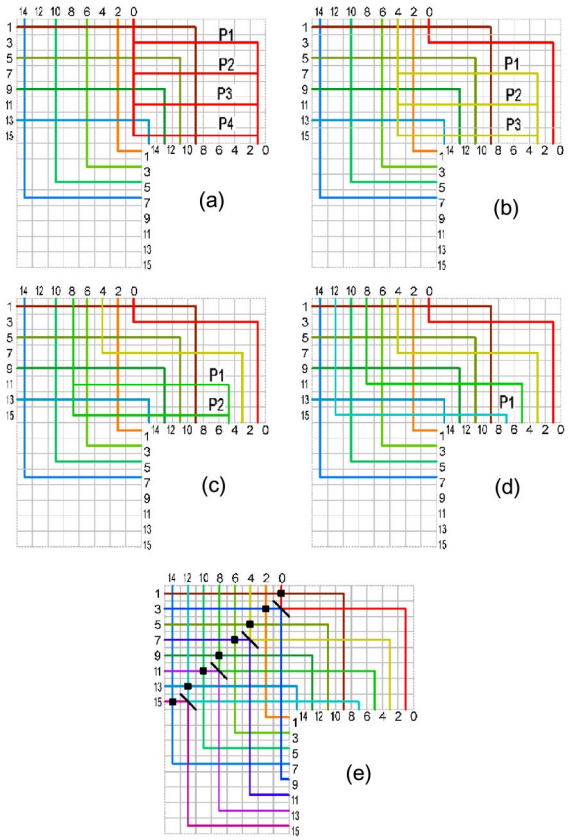

Fig. 15. Example of sufficient-condition application.

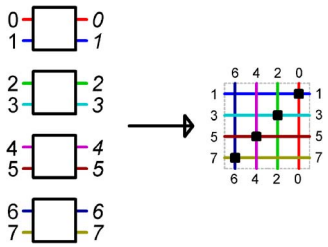

Fig. 16. Terminal SuS.

2) decompose the network in SuSs;
3) iteratively define the configuration of each optical SuS by means of the SuS design algorithm;
4) connect all the SuS modules to obtain the full network.

The SuS design algorithm integrates all the concepts reported in Section IV and adopts Theorem 6 as configuration policy. The main steps of the algorithm are depicted by the flow chart in Fig. 17. Blocks A deals with the generation of the unique paths, while blocks B are dedicated to the free paths.

In our work we have implemented the design procedure of the OMSN (including the SuS algorithm) in a software tool. We have then used the tool to carry out the design of several banyan optical multistage networks of various sizes.

We report here two examples: a 16 × 16 switching-banyan (blocking) network (Fig. 18(a)) and a 16 × 16 Benes (rearrangeable) network (Fig. 18(b)). The optical architectures are represented rotated by 45° counter-clockwise compared to the convention adopted in the previous figures. Network inlets are on the left edge and outlets on the right edge of the networks.

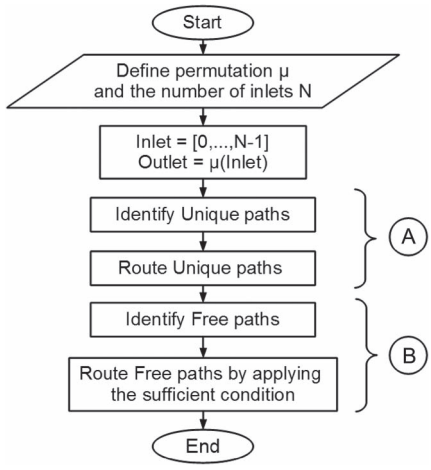

Fig. 17. SuS design algorithm.

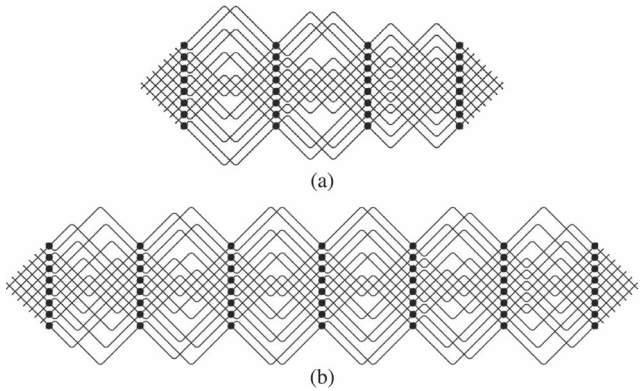

Fig. 18. Optical multistage network examples. (a) 16 × 16 SW-banyan network. (b) 16 × 16 Benes network.

VII. Implementation Issues

What presented so far has been conceived to be technology-implementation invariant. However, technology becomes relevant once a specific implementation has been chosen: the embodiments of the switching architectures we have proposed may require particular extra features to match the technology. We will not attempt here to go into many details, given the primary theoretical nature of this work, but we shall discuss in the following the main concepts by focusing on a set of three cases.

As mentioned in Section II, we may leave the optical world for a while and consider the electronic implementation of our architecture. The evolution of technology of IC has allowed a huge increment in the complexity of the circuits which can be fabricated on a single semiconductor chip. Nowadays, from ten thousand up to a hundred million transistors can be integrated on a single chip by VLSI and ULSI process. By such a huge amount of transistors, an entire system can be integrated on a single chip, leading to the System-on-Chip (SoC) paradigm. All the components of such a system need a communication sub-system, namely a Network-on-Chip, to exchange data each other. In VLSI/ULSI, the layout of a NoC is usually derived according to the Thompson grid model [10]. In this model

[28], [29] the interconnect architecture is mapped on a grid of vertical and horizontal tracks which are spaced apart at regular unit intervals. Two layers of interconnect are used to route the wires. Vertical wires are built in the top layer, while horizontal wires are built in the bottom layer. Hence, wires belonging to two different layers may cross each other without being incident, that is avoiding any direct contact of the metal strips. To change direction, a vertical (horizontal) wire is connected to an horizontal (vertical) wire in the other layer by contact cuts or vias between the two layers.

Our layout complies to the Thompson grid model: the two approaches share the concept of grid mapping and horizontal/vertical wire separation. In fact it is trivial to see from the previous sections that two layers hosting horizontal and vertical segments would be sufficient to obtain each SuS, making our procedure suitable to implement Banyan networks for a VLSI/ULSI SoC.[6]

Let us go back to the photonic world: in this context, loss, crosstalk, spectral distortion and other phenomena may contribute to limit in practice the maximum size of the OMSN that allows error-free transmission of high-rate optical signals. Each optical implementation technology exhibits a set of impairments which are predominant in limiting OMSN scalability.

Let us consider the case of free-space optics interconnection exploiting, for instance, 2-D MEMS switching technology. Being crosstalk between optical beams practically negligible, the most limiting parameter is insertion loss. This is due to several phenomena: Gaussian-beam divergence, air absorption, reflection coefficient of mirrors, mirror curvature and mirror angular misalignment [30]–[32]. Loss caused by beam divergence depends on the free-space distance between the inlet port and the outlet port and on the radius of the mirrors encountered by the beam. The other loss components are directly related to the number of mirrors encountered by the optical beam on its path from the inlet port and the outlet port. Mirror radius is a critical parameter. In fact, it should be kept small to limit power consumption and ensure reliability. On the other hand, the mirror area should be larger than the largest cross-section the Gaussian beam reaches along the optical path due to divergence, otherwise a high amount of optical power will be lost, falling outside the reflecting surface. In Appendix C we report a brief and approximate feasibility analysis, to show how the beam divergence-related impairments can limit the architecture scalability.

Let us discuss now the case of integrated-optics implementation, in which waveguides are used for signal propagation. The insertion loss is determined by: beam path length (because of surface roughness), number of waveguide crossovers and number of waveguide bends [33]. Loss due to the first two factors is predominant, while loss due to waveguide bending is negligible if the bending radius is not too small. But in this case, the major concern is crosstalk, rather than loss. Crosstalk is generated by the waveguide crossovers and the switching elements. Crosstalk due to the latter strictly depends on the optical switching technology used; total crosstalk due to the former is a function of the number of crossovers and also depends on the fabrication process of each of them. Though techniques such as multimode tapered structures [34], [35] are able to improve the crosstalk of each single waveguide crossover (also mitigating the loss), it is more effective to decrease the total number of waveguide crossovers in the network. In single-layer integrated optics, this can be achieved by modifying the construction procedure of the architecture that we have presented in the previous sections. We are currently studying modifications to the technique reported in this paper to reduce the number of crossing points. The results will be reported in further publications.

If we assume that the OMSN can be fabricated using a multi-layer integrated optics structure, a complete elimination of all the waveguide crossovers would be possible. In fact we may adopt the very same Thompson approach mentioned before and used in VLSI/ULSI electronics, to separate vertical from horizontal waveguide segments. Such an optical multi-layer technology is currently not still available for commercial, large scale fabrication, but there are many works in literature proposing the exploitation of multi-layer structures to suppress the crosstalk at the waveguide crossovers [36]–[39].

VIII. Conclusion

We have defined a systematic technique for the design of optical multistage networks based on "classical" switching architectures, known from the switching theory. Our approach lets us precisely specify the structure of the switching-stage modules and how to interconnect them, and it is compatible with both integrated and free-space optics, several photonic-device technologies and VLSI/ULSI electronics. In this paper we have shown the application of the method to the family of banyan networks based on NPBP permutations. However the extension of the technique to networks based on other families of interstage permutations (i.e., parity-preserving banyan and EGS) has been already developed and has been presented in [40].

Appendix A
Superstage Layout

The "Γ" shape we propose is compliant with all the features of the architecture (i.e., modularity and arrangement of optical paths in orthogonal patterns). Modifications of the SuS boundary shape that do not modify the internal geometry of the optical paths and the positions of the SEs are equivalent to the one we are proposing (see Fig. 4). Fig. 19(b) and (c) shows two of the possible alternative layouts of the SuS. As it can be seen, the parity-direction accordance of the inlets/outlets is kept (i.e., odd = vertical; even = horizontal), the concept of unique and free paths can still be applied to such a shape and, moreover, the cascadability property remains unmodified. Therefore all the theorems are still valid. Obviously the layout of the last stage must be modified accordingly to the shape of the SuS.

[6]In the original definition of the Thompson model there is a particular constraint that deserve a separated discussion. For more information see Appendix B.

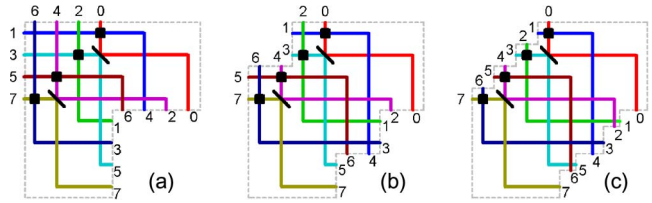

Fig. 19. SuS alternative layouts.

TABLE I
MIRROR RADIUS [μm] VS. NETWORK SIZE (NUMBER OF INLETS AND STAGES)

		N				
		8	16	32	64	128
S	2	106	154	235	372	616
	3	154	235	372	616	1069
	4	196	306	497	845	1509
	5	235	372	616	1069	1943
	6	271	435	732	1290	2375
	7	306	497	845	1509	2805
	8	339	557	958	1726	3234
	9	372	616	1069	1943	3662
	10	404	674	1180	2159	4090
	11	435	732	1290	2375	4518
	12	466	789	1400	2590	4946
	13	497	845	1509	2805	5373

APPENDIX B
THE KNOCK-KNEE PROBLEM

A knock-knee is a position in the layout where two wires turn by 90° in the same point [41]. For example, see position (2, 4) in Fig. 5(a).

The knock-knees occur in our architecture, but they are not allowed in the Thompson model according to its basic and original definition. However the knock-knee problem has been extensively studied in the past and several solutions have been presented [42]–[44]. By resorting to the modified Thompson model, known as Knock-Knee model, our architectures become compliant with the VLSI/ULSI layout.

APPENDIX C
FEASIBILITY AND PERFORMANCE IN FREE-SPACE OPTICS

Using the Gaussian-beam theory [31], [45] we can calculate the minimum mirror radius needed to guarantee a maximum power loss of 3% due to mirrors. The parameter is computed as a function of the size (number of inlets/outlets and of stages) of the OMSN. Table I shows the results.

Owing to the fabrication-process limitations, the mirror size cannot exceed 500 μm, hence only networks with a size corresponding to a mirror radius less than 500 μm are feasible. For example, we can observe that all the possible 8×8 and 16×16 Banyan networks ($N = 8 - S = 3, N = 16 - S = 4$), and 8×8 and 16×16 Benes networks ($N = 8 - S = 5, N = 16 - S = 7$) are feasible. We can conclude that, for free-space MEMS optical-switching technology, there are scalability bounds to our OMSN, mainly due to reliability, fabrication and packaging concerns [31]. In case of actual implementation all these issues must be taken into account to improve the architecture scalability.

REFERENCES

[1] D. G. Garao, G. Maier, and A. Pattavina, "Modular architectures of optical multi-stage switching networks," in *Proc. IEEE INFOCOM*, Torino, Italy, Apr. 2013, pp. 555–559.

[2] A. Saleh and J. Simmons, "All-optical networking: Evolution, benefits, challenges, and future vision," *Proc. IEEE*, vol. 100, no. 5, pp. 1105–1117, May 2012.

[3] R. Essiambre and R. Tkach, "Capacity trends and limits of optical communication networks," *Proc. IEEE*, vol. 100, no. 5, pp. 1035–1055, May 2012.

[4] L. Chen, E. Hall, L. Theogarajan, and J. Bowers, "Photonic switching for data center applications," *IEEE Photon. J.*, vol. 3, no. 5, pp. 834–844, Oct. 2011.

[5] M. Taubenblatt, "Optical interconnects for high-performance computing," *J. Lightw. Technol.*, vol. 30, no. 4, pp. 448–457, Feb. 2012.

[6] S. Yoo, Y. Yin, and K. Wen, "Intra and inter datacenter networking: The role of optical packet switching and flexible bandwidth optical networking," in *Proc. ONDM*, Colchester, U.K., Apr. 2012, pp. 1–6.

[7] S. Pasricha and N. Dutt, *On-Chip Communication Architectures: System on Chip Interconnect*. San Francisco, CA, USA: Morgan Kaufmann, 2008.

[8] L. Benini and G. De Micheli, "Networks on chips: A new SoC paradigm," *Computer*, vol. 35, no. 1, pp. 70–78, Jan. 2002.

[9] *The International Technology Roadmap for Semiconductors—2005 Edition*, ITRS Semiconductor Industry Association, Washington, DC, USA, 2005.

[10] C.-H. Yeh, E. Varvarigos, and B. Parhami, "Multilayer VLSI layout for interconnection networks," in *Proc. Parallel Process.*, Toronto, ON, Canada, Aug. 2000, pp. 33–40.

[11] S.-C. Chau and A. W.-C. Fu, "An optical multistage interconnection network for optimal all-to-all personalized exchange," in *Proc. Parallel Distrib. Comput., Appl. Technol.*, Chengdu, China, Aug. 2003, pp. 292–295.

[12] G. Shen, T. H. Cheng, S. K. Bose, C. Lu, and T. Y. Chai, "Architectural design for multistage 2-D MEMS optical switches," *J. Lightw. Technol.*, vol. 20, no. 2, pp. 178–187, Feb. 2002.

[13] K. Noguchi, T. Sakano, and T. Matsumoto, "A rearrangeable multichannel free-space optical switch based on multistage network configuration," *J. Lightw. Technol.*, vol. 9, no. 12, pp. 1726–1732, Dec. 1991.

[14] M. Taylor and J. Midwinter, "Optically interconnected switching networks," *J. Lightw. Technol.*, vol. 9, no. 6, pp. 791–798, Jun. 1991.

[15] A. Cassinelli, M. Naruse, and M. Ishikawa, "Multistage network with globally controlled switching stages and its implementation using optical multi-interconnection modules," *J. Lightw. Technol.*, vol. 22, no. 2, pp. 315–328, Feb. 2004.

[16] X. Ma and G.-S. Kuo, "A novel integrated multistage optical MEMS-mirror switch architecture design with shuffle Benes inter-stage connecting principle," *Opt. Commun.*, vol. 242, no. 1–3, pp. 179–189, Nov. 2004.

[17] G. Zhu and G.-S. Kuo, "A novel integrated multistage 2-D MEMS optical switch with Spanke–Benes architecture," *J. Lightw. Technol.*, vol. 26, no. 5, pp. 560–568, Mar. 2008.

[18] A. Bianco *et al.*, "Optical interconnection architectures based on microring resonators," in *Proc. Photon. Switching*, Pisa, Italy, Sep. 2009, pp. 1–2.

[19] J. Zhang, H. Gu, and Y. Yang, "A high performance optical network on chip based on Clos topology," in *Proc. ICFCC*, Wuhan, China, May 2010, vol. 2, pp. V2-63–V2-68.

[20] G. Maier, L. Savastano, A. Pattavina, S. Bregni, and M. Martinelli, "Optical-switch Benes architecture based on 2-D MEMS," in *Proc. HPSR*, Poznan, Poland, Jun. 2006, pp. 265–270.

[21] R. A. Spanke and V. Benes, "An N-stage planar optical permutation network," *Appl. Opt.*, vol. 26, no. 7, pp. 1226–1229, Apr. 1987.

[22] R. Spanke, "Architectures for guided-wave optical space switching systems," *IEEE Commun. Mag.*, vol. 25, no. 5, pp. 42–48, May 1987.

[23] C.-C. Lu and R. A. Thompson, "The double-layer network architecture for photonic switching," *J. Lightw. Technol.*, vol. 12, no. 8, pp. 1482–1489, Aug. 1994.

[24] H. Okayama, Y. Okabe, T. Arai, T. Kamijoh, and T. Tsuruoka, "Two-module stage optical switch network," *J. Lightw. Technol.*, vol. 18, no. 4, pp. 469–476, Apr. 2000.

[25] F. Suliman, A. Mohammad, and K. Seman, "A new nonblocking photonic switching network," in *Proc. IEEE GLOBECOM*, San Antonio, TX, USA, Nov. 2001, vol. 4, pp. 2071–2076.

[26] T. Yeow, K. Law, and A. Goldenberg, "Micromachined L-switching matrix," in *Proc. IEEE ICC*, New York, NY, USA, Apr. 2002, vol. 5, pp. 2848–2854.

[27] A. Pattavina, *Switching Theory: Architectures and Performance in Broadband ATM Networks*, 1st ed. Hoboken, NJ, USA: Wiley, 1998.
[28] C. D. Thompson, "Area–time complexity for VLSI," in *Proc. 11th Annu. ACM STOC*, New York, NY, USA, Jan. 1979, pp. 81–88.
[29] C. D. Thompson, "A complexity theory for VLSI," Ph.D. dissertation, Dept. Comput. Sci., Carnegie Mellon Univ., Pittsburgh, PA, USA, Aug. 1980.
[30] L. Lin and E. Goldstein, "Opportunities and challenges for MEMS in lightwave communications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 8, no. 1, pp. 163–172, Jan./Feb. 2002.
[31] L.-Y. Lin, E. L. Goldstein, and R. W. Tkach, "On the expandability of free-space micromachined optical cross connects," *J. Lightw. Technol.*, vol. 18, no. 4, pp. 482–489, Apr. 2000.
[32] C. Li *et al.*, "Using 2×2 switching modules to build large 2-D MEMS optical switches," in *Proc. IEEE GLOBECOM*, San Francisco, CA, USA, Dec. 2003, vol. 5, pp. 2798–2802.
[33] Y. Vlasov and S. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Opt. Exp.*, vol. 12, no. 8, pp. 1622–1631, Apr. 2004.
[34] C.-H. Chen and C.-H. Chiu, "Taper-integrated multimode-interference based waveguide crossing design," *IEEE J. Quantum Electron.*, vol. 46, no. 11, pp. 1656–1661, Nov. 2010.
[35] C.-H. Chen, "Waveguide crossings by use of multimode tapered structures," in *Proc. WOCC*, Kaohsiung, Taiwan, Apr. 2012, pp. 130–131.
[36] A. M. Jones *et al.*, "Ultra-low crosstalk, CMOS compatible waveguide crossings for densely integrated photonic interconnection networks," *Opt. Exp.*, vol. 21, no. 10, pp. 12 002–12 013, May 2013.
[37] P. Koonath and B. Jalali, "Multilayer 3-D photonics in silicon," *Opt. Exp.*, vol. 15, no. 20, pp. 12 686–12 691, Oct. 2007.
[38] Y. Kokubun, Y. Hatakeyama, M. Ogata, S. Suzuki, and N. Zaizen, "Fabrication technologies for vertically coupled microring resonator with multilevel crossing busline and ultracompact-ring radius," *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 1, pp. 4–10, Jan./Feb. 2005.
[39] Y. Hatakeyama, T. Hanai, S. Suzuki, and Y. Kokubun, "Loss-less multilevel crossing of busline waveguide in vertically coupled microring resonator filter," *IEEE Photon. Technol. Lett.*, vol. 16, no. 2, pp. 473–475, Feb. 2004.
[40] D. G. Garao, G. Maier, and A. Pattavina, "Modular EGS architectures for optical interconnections," in *Proc. ICCCN*, Nassau, Bahamas, Aug. 2013, pp. 1–7.
[41] C. Mead and L. Conway, *Introduction to VLSI Systems*. Reading, MA, USA: Addison-Wesley, Dec. 1979.
[42] M. Formann and F. Wagner, "The VLSI layout problem in various embedding models," in *Graph-Theoretic Concepts in Computer Science*, vol. 484, R. Mhring, Ed. Berlin, Germany: Springer-Verlag, Jun. 1991, ser. Lecture Notes in Computer Science, pp. 130–139.
[43] K. Mehlhorn, F. Preparata, and M. Sarrafzadeh, "Channel routing in knock-knee mode: Simplified algorithms and proofs," *Algorithmica*, vol. 1, no. 1–4, pp. 213–221, Nov. 1986.
[44] M. Brady and M. Sarrafzadeh, "Stretching a knock-knee layout for multilayer wiring," *IEEE Trans. Comput.*, vol. 39, no. 1, pp. 148–151, Jan. 1990.
[45] J. T. Verdeyen, *Laser Electronics*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1995, ser. Solid State Physical Electronics Series.