Assessing the width of Gaussian density of states in organic semiconductors

Francesco Maddalena [a], Carlo de Falco [b,c,*], Mario Caironi [a], Dario Natali [d,a,**]

[a] *Center for Nano Science and Technology @PoliMi, Istituto Italiano di Tecnologia, via Pascoli 70/3, 20133 Milano, Italy*
[b] *MOX Modeling and Scientific Computing, Dipartimento di Matematica, Politecnico di Milano, Piazza L. da Vinci 32, 20133 Milano, Italy* [c] *CEN Centro Europeo di Nanomedicina, Piazza L. da Vinci 32, 20133 Milano, Italy*
[d] *Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Piazza L. da Vinci 32, 20133 Milano, Italy*

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1. Introduction

Organic electronics has been rapidly advancing in the last thirty years, with impressive performance improvements for organic transistors [1,2], light emitting diodes [3,4] and solar cells [5,6]. In spite of the progress so far, the fundamental properties of these materials are still not fully understood and the Density of States (DOS), the accurate description of which is mandatory to rationalize

* Corresponding author at: Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Piazza L. da Vinci 32, 20133 Milano, Italy.
** Principal corresponding author.
E-mail addresses: francesco.maddalena@iit.it (F. Maddalena), carlo.defalco@polimi.it (C. de Falco), mario.caironi@iit.it (M. Caironi), dario.natali@polimi.it (D. Natali).

semiconductor optoelectronic properties, makes no exception [7–17]. The determination of the DOS is a far-from-trivial problem in van der Waals, disordered molecular solids such as organic semiconductors, where every molecule has its own unique environment created by its neighbors [18,19]. Atomistic simulations based on realistic morphologies are in principle possible, but the overwhelming computational cost of this approach strongly limits the system sizes it allows to access [20,21].

From the experimental point of view, various techniques have been proposed to assess the DOS. Approaches based on electrical measurements rely upon driving the semiconductor out of thermal equilibrium and measuring carrier mobility under a variety of experimental conditions (space charge limited current [22], Thin Film Transistor (TFT) transfer characteristic curves [23–26], photoconductivity [10], impedance spectroscopy [27]). Since carrier transport actually depends on the DOS, there is a strong concern whether the extracted DOS is really the physical one or rather an *effective* one. Such effective DOS, together with the chosen transport model, can often reproduce the experimental mobility of a specific device, but its use in determining other optoelectronic properties of the organic semiconductor would be questionable [16,15].

Other methods not involving carrier transport have been proposed such as photoemission spectroscopy (PES)[28–30], thermally stimulated luminescence (TSL) [31], electron spin resonance (ESR) [32,33], Kelvin probe method (KP) [34–36], scanning Kelvin probe force micros-copy (SKPM) of TFT channel, electrochemical methods (ECM) [37,38]. Until now none of them has gained enough consensus to be regarded as the reference benchmark [39]: PES suffers from charging in case of thick samples [36], TSL requires non trivial theoretical models for interpretation [40,41]; ESR requires a very specialized experimental setup; KP involves the non-trivial preparation of a set of samples of increasing thickness; SKPM is mostly suited for very thin active layers [14,41]; in ECM doping is likely to introduce additional structural and electrostatic disor-der, making it very difficult to assess the neat material properties [42].

We propose an approach based on Capacitance–Voltage (CV) measurements on Metal–Insulator–Semiconductor (MIS) structures: thanks to suitably low-frequency applied signals, MIS capacitors work in the quasi static regime thus keeping the semiconductor in thermal equilibrium. In addition, the relatively simple experimental setup is in favor of a wide applicability of the method. We assume a Gaussian shape for the DOS: the justification for this choice- indeed very commonly adopted [43–45] – lies in the fact that coupling between a charge carrier and a random distribution of static or induced dipoles leads to a Gaussian function [46]. We focus our efforts to extract the DOS width and we accomplish this by numerical fitting of experimental measurements, exploiting the fact that the DOS width has a sizable impact on the spatial distribution of accumulated carriers, which in turn affects the shape of the CV curve. Apart from few exceptions [47,48], the correlation between the dependence of the MIS capacitance on the gate bias and the DOS width has been overlooked, and CV measurements on organic MIS structures have been analyzed in the framework of Mott-Schottky depletion region [49–51] or have been used to extract the contact resistance at the metal/semiconductor interface [52,53].

We report on the application of our method to two model and widely studied materials: the n-type polymer poly[N, N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarbox-imide)-2,6-diyl]-alt-5,5'-(2,2'-dithiophene) (P(NDI2OD-T2)) and the p-type polymer poly(2,5-bis(3-tetradecylthio-phen-2-yl) thieno [3,2–50] thiophene) (PBTTT) (see Fig. 1). For both materials we are able to obtain very good fittings of experimental CV curves and to robustly extract DOS widths. In addition, we show that the extracted DOS widths, combined with the Extended Gaussian Disorder Model for transport, allow for a detailed modeling of the linear regime of P(NDI2OD-T2) and PBTTT based transistors.

2. Methods

2.1. Numerical model

The structure of a MIS capacitor is sketched in Fig. 1a. It consists of a stack comprised of: a metal (back) contact which is kept grounded, a semiconducting layer, an insulating layer and a top (gate) metal contact where the external voltage bias is applied. The geometrical setting for the numerical model is reported in Fig. 2. We denote by z the spatial coordinate normal to the semiconductor/insulator interface and we place the origin of the z axis in correspondence of such interface. We denote by t_{sc} (t_{ins}) the thickness of the semiconductor (insulator) layer. We assume the extension of the device in the x and y directions (the coordinates in the plane parallel to the interface) to be much larger than both t_{ins} and t_{sc} and we consider both materials to be homogeneous and isotropic. We further assume that: (i) the semiconductor is intrinsic, as it is very often the case in organic semiconductors; (ii) the semiconductor is unipolar and to fix ideas is of n-type; (iii) thermal carrier generation can be disregarded, as energy gaps are usually relatively large; (iv) insulator leakage currents are negligible.

In DC, the MIS capacitor is in quasi equilibrium irrespective of the gate bias, as no DC current can flow across the structure; therefore we can introduce a well-defined Fermi level E_F independent of z. With no loss of generality, we can set $E_F = 0$. We denote by $E_{LUMO}(z)$ the energy of the Lowest Unoccupied Molecular Orbital and by $E_{HOMO}(z)$ the energy of the Highest Occupied Molecular Orbital at a given point z in our computational domain. We define the energy barrier for electron injection at the metal/semi-conductor interface as

$$\Phi_B := E_{LUMO}(-t_{sc}) - E_F(-t_{sc}) = E_{LUMO}(-t_{sc}).$$

The total amount of charge per unit volume at a given point z in the device can be expressed as the sum over all admissible energies of the DOS, $g_\sigma(E)$, times the occupation probability for that state, $f(E)$, *i.e.*

$$n = \int_{-\infty}^{\infty} g(E - E_{LUMO}) f(E - E_F)\, dE. \quad (1)$$

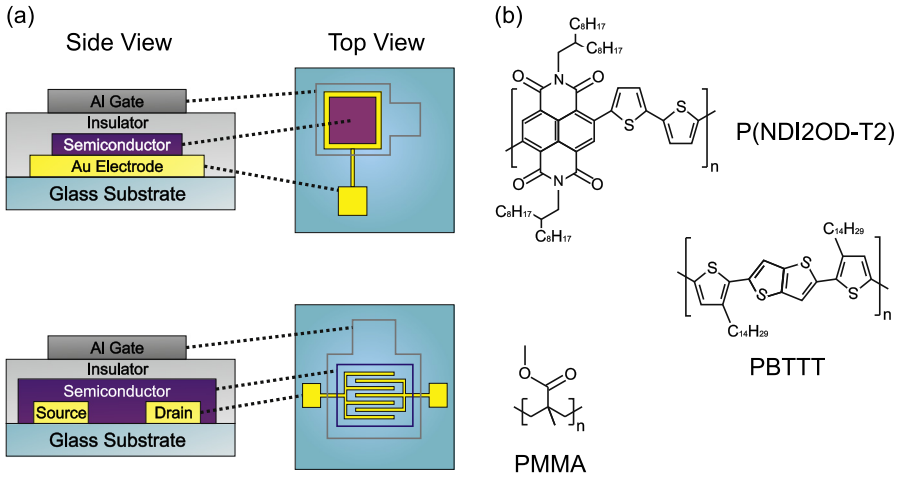

Fig. 1. Panel (a): Top and side view of the devices used throughout this paper: the MIS capacitor on top and the TFT on bottom. Panel (b): Chemical structure of the polymer materials used in this study.

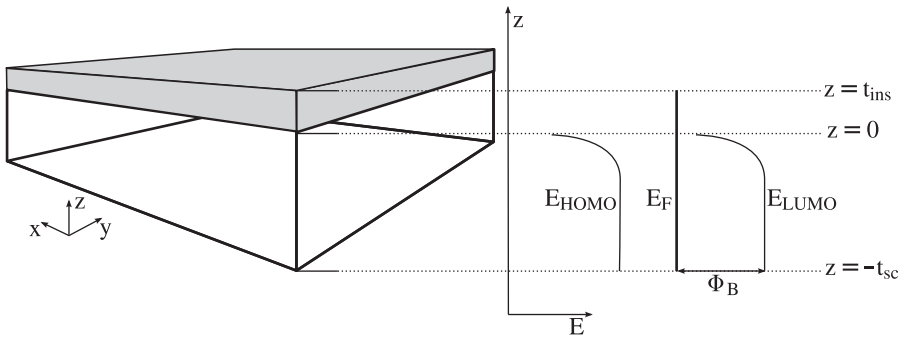

Fig. 2. Geometrical setting for the numerical model and qualitative sketch of energy levels for a positive gate voltage applied (bottom and top metal contacts not shown).

In the following we will always assume that Fermi statistics applies. As to the DOS we adopt a single symmetric Gaussian centered at E_{LUMO} and parametrized by its standard deviation

$$g_\sigma(\cdot) = \frac{N_0}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(\cdot)^2}{2\sigma^2}\right), \tag{2}$$

where N_0 denotes the total number of available states per unit volume, assumed equal to $10^{21}\mathrm{cm}^{-3}$ according to Refs. [54–56,43]. The electrical potential φ within the one-dimensional device structure corresponding to a voltage V_g applied at the gate contact is obtained by solving the non-linear elliptic boundary value problem comprised of the Poisson equation together with the integral relation reported in Eq. (1). This task is accomplished by means of a damped-Newton type functional iteration technique [57–59] and then discretizing the resulting linear differential boundary value problems by piece-wise linear continuous Finite Elements [60–62]. The differential capacitance at a given bias point is evaluated via the procedure described in Refs. [63,64] (see Supplementary Material for details).

2.2. Experimental aspects

Devices and experimental measurements have been devised in order to ease as far as possible the comparison between measured CV curves and numerically simulated ones. Since simulations are performed in 1 dimension the device structure has been purposely engineered in order to minimize 2D effects. As shown in Fig. 3(a), the area of the top electrode A_{gate} (defined with a shadow-mask), is larger (hundreds of μm) than the area of the bottom one A_{bottom} (defined by lithography), in order to allow some tol-erance in their mutual alignment during sample prepara-tion. In unpatterned devices a lateral spreading of accumulated charges (from A_{bottom} to A_{gate}) occurs as a function of V_g. The issue is solved by patterning the semi-conductor area smaller than both A_{bottom} and A_{gate}, so that charge accumulation takes place in a 1D fashion affecting a constant area (see Supplementary Material).

As to the measurement scheme, the MIS capacitance is probed by applying a sinusoidal perturbation δV_g. The frequency of δV_g has to be chosen judiciously to keep the semiconductor in thermal equilibrium, which means that the time needed by the device to adjust $n(z)$ has to be far

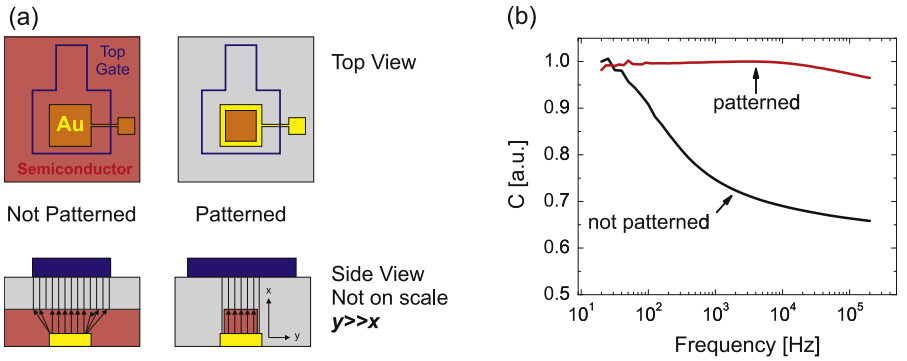

Fig. 3. Panel (a) shows top and side view of the MIS capacitor when the semiconductor is unpatterned and when it is patterned. The thin lines are a qualitative representation of the field lines in the insulator when the device is in accumulation. The black arrows are a qualitative representation of the path of charge carriers. Panel (b) shows the patterning effect on the CF characteristics of a P(NDI2OD-T2)-based MIS capacitor. When the semiconductor is unpatterned the low frequency plateau is almost indistinguishable (black curve). When the semiconductor is properly patterned the plateau extends up to few tens of kHz (red curve). CF curves have been measured in accumulation ($V_g = 35$ V) and normalized to the value in depletion ($V_g = -15$ V) in order to disentangle the frequency behavior of the accumulated channel from the frequency dependence of ε_{ins} (see Supplementary Material). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

smaller than the perturbation period. This can be verified by looking at the frequency dependence of the device impedance: at suitably low frequencies, the device is in quasi equilibrium and its impedance can be modeled as being purely capacitive; when the frequency is too high, the device is driven out of equilibrium and resistive contributions to the impedance are expected to appear. The frequency range where thermal equilibrium is ensured, which gives rise to a capacitive plateau in the Capacitance-Frequency (CF) characteristics, is maximized by patterning the semiconductor because the path to be traveled by carriers is minimized and made equal to the semiconductor thickness (few tens of nm). In contrast, in the unpatterned case the carriers have to laterally spread by few hundreds of μm [65–67]. Indeed in the case of P(NDI2OD-T2) the capacitive plateau is not discernible in the unpatterned case within the explored frequency range, whereas it extends up to few tens of kHz in the patterned case (Fig. 3(b)).

2.3. From the DOS to the TFT current

To show that the DOS width extracted by means of CV measurements is meaningful, we combine it with Extended Gaussian Disorder transport model (EGDM) [43] to fit experimental current–voltage (IV) measurements on TFTs.

In the EGDM the carrier-density and electric field dependent mobility is expressed as [68,69]:

$$\mu_n(n,\mathcal{E}) = \mu_{n,0}\; g_1(\mathcal{E})\; g_2(n), \tag{3}$$

where $\mu_{n,0}$ denotes the mobility in the low-field and low-charge-density regime, $\mathcal{E}$ the electric field, g_1 and g_2 the field enhancement and the density enhancement terms, respectively (see Supplementary Material). These latter two depend on σ, N_0, and the temperature T. Therefore, once the DOS width is known the carrier mobility is determined apart from the multiplicative coefficient of mobility $\mu_{n,0}$.

We focus on transfer characteristic curves of TFTs and we restrain our analysis to the linear regime ($V_g \gg V_d$, with V_d the applied drain to source voltage), so that $\mathcal{E}$ can be approximated as being constant from source to drain, viz. $\mathcal{E} = V_d/L$ where L is the channel length. The TFT current can be expressed as the product of V_d by the channel conductance G_{ch}. Within the gradual channel approximation [70] this is calculated by integrating the z-dependent conductivity $\Sigma(z)$ along the film thickness:

$$G_{ch} = \frac{W}{L}\int_0^{-t_{sc}} \Sigma(z)\; \mathrm{d}z = \frac{W}{L}\;\mu_{\mathrm{n,eff}}\;\mathrm{Q_{ch}}, \tag{4}$$

where we have introduced the *total accumulated charge* (per unit area)

$$\mathrm{Q_{ch}} := \int_0^{-t_{sc}} \mathrm{q}\; n(z)\mathrm{d}z, \tag{5}$$

and the *effective mobility*

$$\mu_{\mathrm{n,\ eff}} := \mu_{n,0}\; g_1(\bar{\mathcal{E}})\;\frac{\mathrm{q}}{\mathrm{Q_{ch}}}\int_0^{-t_{sc}} g_2(n(z))\; n(z)\mathrm{d}z. \tag{6}$$

3. Results and discussion

3.1. Sensitivity of CV curves to DOS width

For the sake of simplicity, we assume Φ_B to be *large*, which means that the bottom metal contact and the semiconductor reach thermal equilibrium with a negligible mutual exchange of electrons. This approximation is well suited for P(NDI2OD-T2) since $E_{\mathrm{LUMO}} = -4$ eV and for gold $E_{\mathrm{F}} = -5$ eV with respect to vacuum. The converse is true for PBTTT ($E_{\mathrm{HOMO}} = -5.1$ eV): this case is treated in Section 3.3.

In general, the gate effect in a MIS capacitor is to shift and bend E_{LUMO} thus bringing the DOS closer to E_{F} (see Fig. 2). At moderately positive gate voltages, E_{F} is still located well within the energy gap and far from the DOS, hence no carriers are present in the semiconductor. For

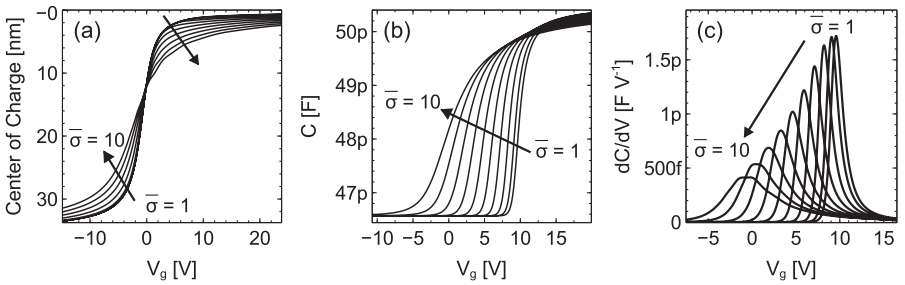

Fig. 4. Panel (a): Distance of the accumulated center of charge from the semiconductor/insulator interface as a function of V_g calculated for various values of disorder parameter $\overline{\sigma} = \sigma/k_BT$. In panel (b) and (c) the CV curves and their first derivatives are shown. Simulation parameters: $t_{sc} = 35$ nm, $t_{ins} = 445$ nm, $\varepsilon_{sc}/\varepsilon_0 = 2.9$, $\varepsilon_{ins}/\varepsilon_0 = 2.82$, $\Phi_B = 1$ eV, $N_0 = 10^{21}$ cm^{-3}, $T = 295$ K.

larger gate voltages, E_F starts sweeping the semiconductor DOS, thus determining an accumulation of electrons in the semiconductor which tend to peak close to semiconductor/insulator interface. The spatial distribution of accumulated charges is influenced by the DOS width: at a certain coordinate $\overline{z}$ in the semiconductor, for a given distance between E_F and $E_{LUMO}(\overline{z})$, a larger DOS width implies that more states are close to or even below E_F and hence are occupied, which results in a smoothing of the peak in $n(z)$.

Instead of directly probing $n(z)$, it is more convenient to probe $\delta n(z)$, the additional accumulation of carriers induced by superimposing to the DC gate voltage bias a small-signal δV_g, because information on $\delta n(z)$ can be obtained by means of a simple electrical measurement such as a CV. The MIS capacitor can be modeled as the series connection of the insulator capacitance and of the semiconductor capacitance. The former is a constant parallel plate capacitance, viz. $C_{ins} = A\varepsilon_{ins}/t_{ins}$, where A denotes the device area. As to the latter, which we denote by C_{sc}, it can be *thought as* a V_g-dependent parallel plate capacitance: one of the plates is permanently located at the semiconductor/insulator boundary, whereas the other one is represented by the center of charge of $\delta n(z)$, defined as $t_{CoC}(V_g) = \int_{-t_{sc}}^{0} \delta n(z)\, z\, dz / \int_{-t_{sc}}^{0} \delta n(z)\, dz$, so that $C_{sc} = A\varepsilon_{sc}/t_{CoC}$. For suitably small values of V_g, the center of charge resides on the back metal contact as no carriers are accumulated in the semiconductor, viz. $t_{CoC} \simeq t_{sc}$. The device is said to be *in depletion* and the MIS capacitance attains a value given by $\left(C_{ins}^{-1} + C_{sc\,dep}^{-1}\right)^{-1}$, where $C_{sc\,dep} = A\varepsilon_{sc}/t_{sc}$. Upon increasing V_g, the center of charge moves from the bottom metal towards the insulator, hence C_{sc} increases. For suitably large V_g, t_{CoC} approaches an asymptotic value which we denote $t_{CoC\,acc}$ (Fig. 4(a)), C_{sc} tends to $C_{sc\,acc} = A\varepsilon_{sc}/t_{CoC\,acc}$ and the MIS capacitance attains a value given by $\left(C_{ins}^{-1} + C_{sc\,acc}^{-1}\right)^{-1}$. It is apparent that the shape of C versus V_g curve is closely related to the DOS broadening, as shown in Fig. 4(b). The first noticeable effect is that, upon increasing disorder, the functional dependence of the center of charge on V_g becomes smoother, hence the CV curve becomes less steep. A second effect is that both the plot of t_{CoC} versus V_g and the plot of C versus V_g experience a shift towards more negative values of V_g. This may be understood by considering that, since the Fermi level is closer to energy regions where the DOS is sizable, a smaller gate voltage is needed to accumulate charges in the semiconductor. Finally, the asymptotic position of the center of charge at high V_g is moved away from the semiconductor/insulator interface, hence the broader the DOS the lower the asymptotic capacitance [55].[1]

The effects of disorder on the CV curve outlined above are reflected and somehow amplified if one looks at the first derivative of the CV curve with respect to V_g, shown in Fig. 4(c). The qualitative shape of the dC/dV_g versus V_g curve, for a Gaussian DOS, may be described as a function displaying a single peak and a non-symmetric slope on both sides of the peak itself. Upon increasing the disorder parameter σ, the dC/dV_g versus V_g curve becomes smoother, and its peak is lowered and shifted towards more negative V_g values.

3.2. Case study 1: P(NDI2OD-T2)

P(NDI2OD-T2) is a stable n-type organic semiconductor with high mobility that features trap-free electron conduction and good electron injection from stable electrodes such as gold [71,72]. The experimental CV curve (measured at 9283 Hz) is numerically fitted to extract σ according to an algorithm reported in Supplementary Material. Results are reported in Fig. 5. We extract for σ a value of about 78 meV. It is possible to appreciate that the single gaussian ansatz (Eq. (2)) for the DOS allows to obtain a very good fit. The DOS extracted from our CV measurements is expected to reflect an intrinsic material property hence it should not vary if other device physical parameters (such as dimensions, temperature, insulator etc.) are modified. To verify this, we exploit the frequency dependence of the insulator electrical permittivity (PMMA), that varies from $3.4\varepsilon_0$ to $2.7\varepsilon_0$ when the frequency goes from few tens of Hz to few tens of kHz (see Supplementary Material). By changing the measuring frequency we change the insulator permittivity without actually producing new devices, thus

[1] Thermal equilibrium within the semiconductor, viz. no net current condition, is reached because the drift flow of electrons towards the semiconductor/insulator interface is counterbalanced by an opposite diffusion flow, due to the electron concentration gradient. The DOS broadening enhances the diffusion coefficient [68,55], and consequently a smaller gradient in the electrons concentration – viz. a less peaked distribution – is needed for the diffusion flow to counterbalance the drift flow: this implies that t_{CoC} recedes from the semiconductor/insulator interface.

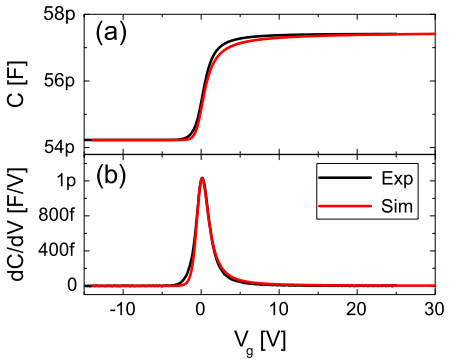

Fig. 5. Experimental and fitting curves for a P(NDI2OD-T2)-based MIS capacitor: (a) CV curve; (b) first derivative of CV curve. Measurement frequency 9283 Hz.

keeping the delicate physics and chemistry of the semiconductor/insulator interface fixed [73–75]. We performed CV measurements at three additional frequencies (namely 233 Hz, 2332 Hz and 23,318 Hz, all falling within the fre-quency plateau) and we fitted them using for σ the value extracted at 9283 Hz, obtaining very satisfactory fittings (Fig. 6): this validates our approach and corroborates the reliability of the extracted parameter.

After the DOS width extraction, we proceeded to simulate the MIS capacitor in DC (viz. using $\varepsilon_{ins} = 3.6\varepsilon_0$), which is the relevant case for fitting TFT IV curves (*vide infra*). Fig. 7(a) shows the LUMO level and the carrier density at $z = 0$. Around $V_g = 0$ V a strong accumulation regime sets in: the LUMO level enters in a region where the DOS is siz-able (about 0.2–0.3 eV below the maximum), and the sur-face carrier density starts growing in the range of 10^{19} cm^{-3}. A color map of the carrier density as function of the z coordinate and of V_g is reported in Fig. 7(b): once strong accumulation sets in, 90% of the accumulated charge is located within less than 2 nm from the semicon-ductor/insulator interface: we assume this value as an esti-mate of the channel depth.

Finally we fitted experimental linear transfer characteristic curves of P(NDI2OD-T2)-based TFT combining the extracted DOS width with the EGDM transport model (Section 2.3). Results, showing a very good match between experimental measurements and simulated curves, are reported in Fig. 8. The fitting was obtained by adjusting only one parameter, namely the mobility multiplicative coefficient $\mu_{n,0}$, which turned out to be 3.09×10^{-2} cm^2 V^{-1} s^{-1} ($g_1 \simeq 1$). Knowing the mobility, it is possible to study the TFT in the linear regime in detail. The 2D color map of Fig. 9(a) shows the carrier mobility as function of

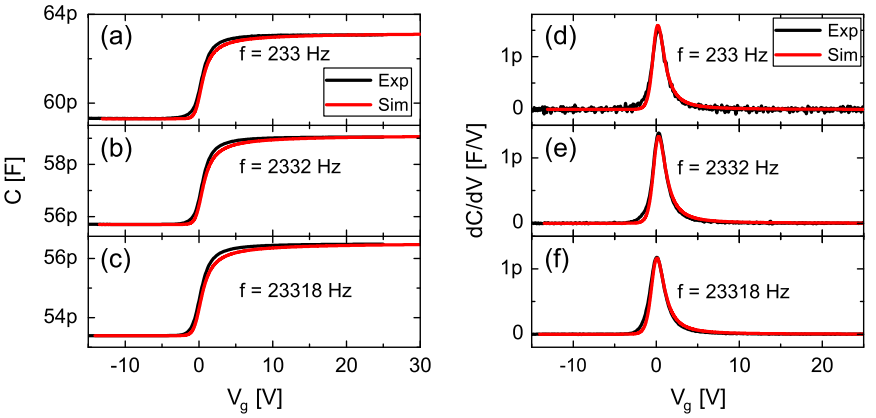

Fig. 6. Experimental and fitting CV curves at different values of insulator permittivity for a P(NDI2OD-T2)-based MIS capacitor: (a) $\varepsilon_{ins} = 3.12\varepsilon_0$ at 233 Hz, (b) $\varepsilon_{ins} = 2.9\varepsilon_0$ at 2332 Hz, (c) $\varepsilon_{ins} = 2.77\varepsilon_0$ at 23318 Hz. Panels (d), (e) and (f) shows the related dC/dV curves. To fit the curves, the DOS width extracted at $f = 9283$ Hz has been employed.

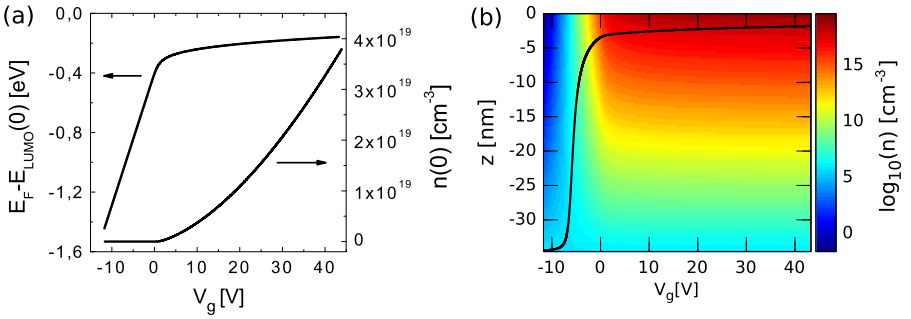

Fig. 7. Results of DC simulation of P(NDI2OD-T2)-based TFT. Panel (a): LUMO level and carrier density at the semiconductor/insulator interface as function of V_g. Panel (b): Charge carrier density as a function of position and applied voltage. The solid line represents the channel depth, defined as the locus of the points $(\hat{z}, \hat{V}_g)$ such that the region comprised between 0 and $\hat{z}$ contains the 90% of the whole accumulated charge density. The channel depth is as small as -1.8 nm for $V_g = 43$ *V*.

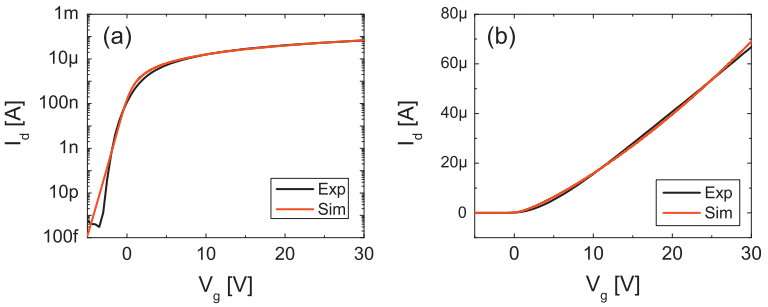

Fig. 8. Comparison of simulated (red lines) and measured (black lines) transfer characteristic curves of a P(NDI2OD-T2)-based TFT: (a) logarithmic scale and (b) linear scale. $W/L = 10000/10, V_d = 5$ V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

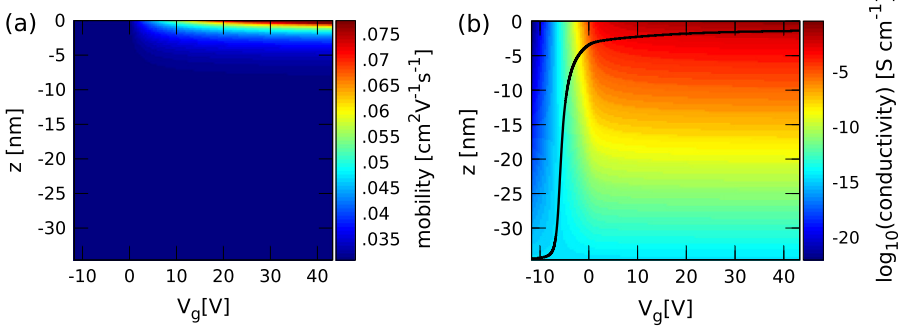

Fig. 9. Results of DC simulation of P(NDI2OD-T2)-based TFT Panel (a) shows the mobility as a function of position and applied voltage. Panel (b) shows conductivity as a function of position and applied voltage. The solid line in panel (b) line represents the current penetration depth, defined as the locus of the points $(\hat{z}, \hat{V_g})$ such that the region comprised between 0 and $\hat{z}$ has a conductance as large as the 90% of the conductance of the whole film. At $V_g = 43$ V the current depth is -1.37 nm.

V_g and z. Since the carrier density increases on going from $z = -t_{sc}$ to the semiconductor/insulator interface, so does the carrier mobility, according to the carrier-density enhancement factor $g_2 : g_2 \simeq 2.5$ at $z = 0$. Fig. 9(b) reports the 2D color map of the conductivity $\Sigma(V_g, z)$: once in deep accumulation, 90% of the conductance of the whole film is due to the region comprised between 0 nm and -1.37 nm: we take this value as an estimate of the current penetration depth. Due to the mobility enhancement along z, the channel and the current depth do not coincide, the latter being slightly smaller than the former.

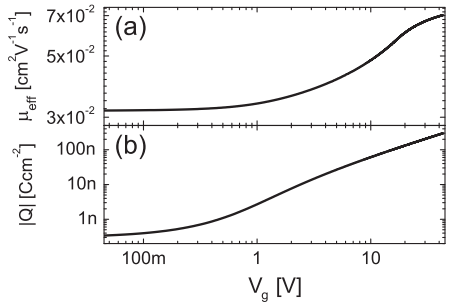

Fig. 10. Results of DC simulation of P(NDI2OD-T2)-based TFT. Panel (a) shows the effective mobility (see Eq. (6)), as a function of applied voltage. Panel (b) shows the total accumulated charge (see Eq. (5)), as a function of applied voltage.

Finally we calculate the two quantities which are of interest for experimentalists, viz. the total accumulated charge Q_{ch}(see Eq. (5)) and the *effective* mobility (see Eq. (6)). As shown in Fig. 10, $\mu_{n,eff}$ upon channel formation starts growing; it increases more steeply for low V_g, whereas for high V_g the V_g- dependence gets milder. The functional dependence on V_g appears to be hardly reproducible by means of simple relations (such as power law) over the explored voltage range. As to Q_{ch}, for V_g in excess of few volts it can be well approximated by a linear dependence on V_g (actually $Q_{ch} \propto V_g^{1.12}$). This suggests that the V_g-dependence of C_{sc} is negligible, in agreement with the fact that the channel depth is barely dependent on V_g in this voltage range (Fig. 7).

We conclude noting that in the literature, the DOS of P(NDI2OD-T2) has been extracted by fitting experimental space charge limited curves of unipolar metal/semiconductor/metal structures using numerical drift/diffusion model based on EGDM [22] obtaining $\sigma = 85$ meV, in relatively good agreement with our value of about 78 meV. Apart for the aforementioned entanglement of DOS and transport in transport-based DOS extraction methods, we observe that in Ref. [22], a range of parameters has to be explored in terms of applied voltages, temperature and, – most notably – layer thickness (which implies the production of a set of devices and the need to cope with data scattering). This has to be compared to our method, which more

simply consists of measurements on a single device at room temperature by varying the applied voltage and applied frequency.

3.3. The effect of small injection barriers at the metal/semiconductor interface

In the following we discuss the effect of small energetic barriers on CV curves. As this case is relevant for PBTTT, we fix ideas on a p-type semiconductor for which $\Phi_B = -E_{HOMO}(t_{sc})$. In Fig. 11 we plot CV curves and their first derivatives upon varying Φ_B from 1 eV down to 0 eV. As long as Φ_B is large, *i.e.*, larger than about 0.8 eV in this specific example, its reduction mainly results in an almost rigid shift of the CV curves and barely affects their shapes, due to the fact that the smaller the barrier, the closer the Fermi level is to the DOS when $V_g = 0$ V, the easier is to drive the device into accumulation. For Φ_B comprised between 0.4 eV and 0.6 eV, in addition to the curve shift, the CV curve shape is affected as well, becoming smoother (and its first derivative less peaked). For $\Phi_B < 0.2$ eV the depletion capacitance starts growing. These phenomena can be explained considering that the barrier height deter-mines the boundary carrier density at the metal–semicon-ductor interface. CV curve smoothing occurs because the carrier density at the bottom metal–semiconductor inter-face interferes with the gate attraction of the center of charge towards the semiconductor–insulator interface. As to the rise of the capacitance in depletion, the mentioned boundary condition maintains a non-negligible carrier density in the semiconductor irrespective of V_g; hence, the center of charge approaches but never reaches the bot-tom metal contact. These observations clearly illustrate that Φ_B can have a large influence on CV curves shape, thus possibly hindering a correct DOS extraction if not properly taken into account. Since Φ_B is difficult to predict and prone to depend on actual device processing [76], we devised a modification of our fitting algorithm to extract both σ and Φ_B (see Supplementary Material).

3.4. Case study 2: pBTTT

PBTTT is a stable p-type semiconductor displaying liquid crystalline features [77]. The PBTTT-based MIS capacitor has a frequency plateau extending beyond hundreds of kHz (see Supplementary Material). The experimental CV curve (measured at 9283 Hz) and the corresponding fitted numerical one, together with their first derivatives are reported in Fig. 12. We extract a value for σ of about 98 meV and for Φ_B of 0.42 eV (implying $n(-t_{sc}) = 8 \times 10^{16}$ cm^{-3}, see also Supplementary Material). Including Φ_B in the fitting procedure turns out to be very important to assess the DOS. In fact, if $n(-t_{sc})$ is assumed to be negligible, then the fitting returns a larger value for σ (about 173 meV), because the smoothness of the experimental CV curve is incorrectly traced back to the DOS disorder alone. Despite being generally regarded as a highly ordered material, the DOS width we extract is relatively large: this in qualitatively good agreement with recent studies on PBTTT [78], that show that disorder is low in the lamellar-stacking direction, yet it is relatively large in the π-stacking direction, which is the most relevant to the DOS. We verified that the DOS width extracted at 9283 Hz is robust, by fitting with it CV curves at additional frequencies (see Supplementary Material).

3.5. PBTTT channel conductance estimation: effect of small injection barriers

The boundary conditions to be considered at the bottom of the simulation domain, $z = -t_{sc}$, are, in principle, different in the case of the MIS capacitor and in the case of the TFT. In the former they are dictated by the bottom metal, but in the latter – focusing on our specific case of a staggered TFT – one should set to 0 the current in the z direction, and this would require an (at least) 2D simulation. Choosing an appropriate boundary condition to be set in a 1D simulation framework is non-trivial and, indeed, no consensus seems to exists in the literature regarding this issue: Simonetti and co-workers considered the Fermi level at its equilibrium position [54], whereas Xu and co-workers adopted a zero-field boundary condition [79].

In the case of P(NDI2OD-T2) where the injection barrier is large, we applied to the TFT the same boundary conditions of the MIS capacitor, as in both devices a negligible carrier density is expected at $z = -t_{sc}$, and the choice turned out to be effective (Fig. 8). In the case of PBTTT where barriers are smaller the same approach proves to be largely inaccurate: with the value obtained from MIS capacitor fitting (0.42 eV), TFT current is overestimated as shown in Fig. 14. Indeed a large carrier density exists close to the source/semiconductor and drain/semiconductor

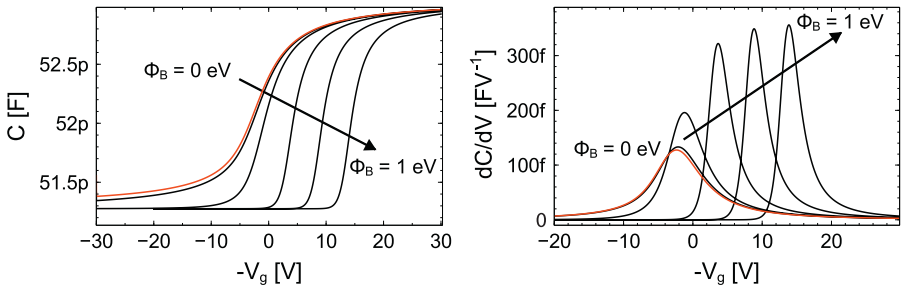

Fig. 11. Panel (a) and (b) show the simulated dependence of CV and dC/dV curves respectively on the energetic injection barrier Φ_B for a p-type semiconductor (Φ_B goes from 1 eV down to 0 eV in steps of 0.2 eV). Red curves refer to $\Phi_B = 0$ eV. Simulation parameters: $t_{sc} = 43$ nm, $t_{ins} = 477$ nm, $\varepsilon_{sc}/\varepsilon_0 = 5.8$, $\varepsilon_{ins}/\varepsilon_0 = 2.82$, $\sigma = 98$ meV, $N_0 = 10^{21}$ cm^{-3}, $T = 295$ K. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

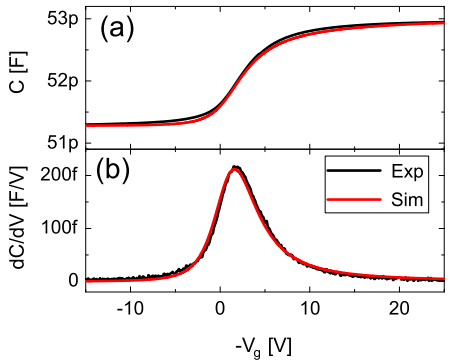

Fig. 12. Experimental and fitting curves for a PBTTT-based MIS capacitor: panel (a) and (b) show the CV curve and its first derivative respectively. Measurement frequency 9283 Hz.

interfaces, but it only *partially* spreads laterally in the channel. Forcing a very low carrier density at $z = -t_{sc}$ (by fixing the Fermi level in the midgap), results in an underestimation of the TFT current (not shown); imposing a Neumann boundary condition does not produce better results.

To cope with this issue without recurring to a 2D simulation, we resort to a separation-of-variables approach, *i.e.*, we perform a set of equilibrium simulations of 1D metal/semiconductor/metal structures with inter-electrode separation equal to the channel length of our TFT (10 μm), varying the metal/semiconductor barrier, as shown in Fig. 13. We consider a p-type semiconductor and we use the DOS parameters of PBTTT extracted in Section 3.4.

In case of *large* barriers ($\Phi_B > 0.7$ eV) carrier diffusion from metals is negligible and the potential is almost flat and it is fixed by the interface alignment of energetic levels. For barriers lower than 0.7 eV the situation changes: a non-negligible amount of charge diffuses from metals into the semiconductor and accumulates close to the metal/semiconductor interfaces. Farther from the contacts the HOMO level relaxes to a value of about 0.7eV below E_F, irrespective of the actual value of Φ_B, and consequently the carrier density tends to settle down to about 10^{12} cm^{-3}. Hence we assume 0.7 eV as the boundary condition for the TFT channel conductance calculation, and we actually find that this value gives the best fitting of the experimental IV curves, as shown in Fig. 14. The low density mobility of PBTTT turns out to be $\mu_{p,0} = 2.08 \times 10^{-2}$ cm^2 V^{-1} s^{-1} ($g_1 \simeq 1$).

We can now proceed to an in-depth analysis of PBTTT-based TFTs. Fig. 15 reports the distance between E_F and E_{HOMO} and the carrier density at the insulator/semiconductor interface. When in deep accumulation ($V_g < -40$ V) the former is about −0.24 eV and the latter attains about 10^{19} cm^{-3}. With respect to P(NDI2OD-T2), E_F in PBTTT remains farther from the gaussian center and consequently the surface charge density is lower (note that in P(NDI2OD-T2) at the interface $E_{LUMO} - E_F = -0.16$ eV and $n(0) \simeq 3.8 \times 10^{19}$ cm^{-3}). Fig. 15 also reports a 2D map of carrier density as a function of position and of V_g : the channel depth is 4.75 nm. Fig. 16 reports the 2D maps of mobility and conductivity. Carrier-density driven mobility enhancement is large in PBTTT: the mobility increases by a factor as large as 5 going from $z = -t_{sc}$ to 0. As to the con-ductance, also shown in Fig. 16, it can be noticed that the current penetration depth is of 2.78 nm. By comparing PBTTT and P(NDI2OD-T2) we can observe that due to the larger DOS width of the former: (i) PBTTT channel depth is more than twice as large as P(NDI2OD-T2); (ii) the PBTTT mobility enhancement is more than twice as large as P(NDI2OD-T2); (iii) because of (ii) the PBTTT current depth considerably shrinks with respect to the channel depth, being finally only 30% larger than P(NDI2OD-T2). The effective mobility $\mu_{p,\,eff}$ and the total accumulated charge Q_{ch} are reported in Fig. 17 as a function of V_g. For $V_g < -10$ V the former can be approximated as a power law of the gate voltage, viz. $\mu_{p,eff} \propto |V_g|^{0.79}$. The latter, in the same range, can be written as $Q_{ch} \propto |V_g|^{1.67}$: this is due to the fact that C_{sc} has a non-negligible dependence on V_g, in agreement with the fact that the channel depth has a sizable dependence on V_g, as shown in Fig. 15. Thus, the overall dependence of current on V_g is large, $I \propto |V_g|^{2.46}$, but this strong departure from the textbook expected linear dependence on V_g is due to the additive effect of *both* $\mu_{p,eff}$ and Q_{ch} being dependent on the gate voltage: while the former phenomenon is known in the literature, the latter is – to our knowledge – overlooked.

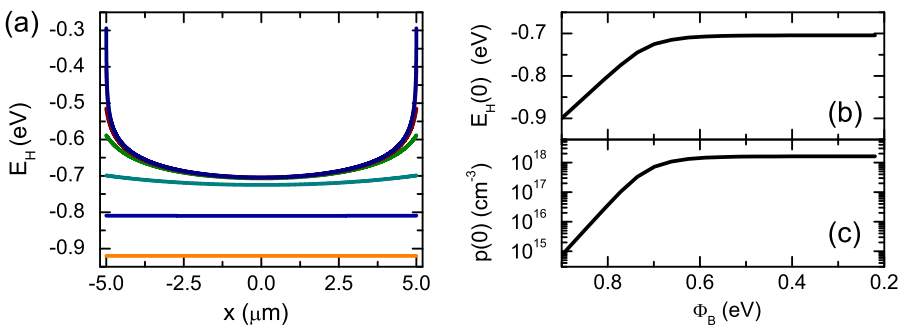

Fig. 13. Equilibrium simulations of 1D metal/semiconductor/metal structures (inter-electrode distance 10 μm). Panel (a) shows the HOMO level E_H as a function of space for various values of Φ_B (Φ_B values can be read as $= -E_H$ evaluated in $x = -5$ μm). Panel (b) and (c) shows the dependence of the HOMO level and of the carrier density at the mid point of the structure as a function of Φ_B respectively. The Fermi level has been set to 0 eV. Other simulation parameters: $\sigma = 98$ meV, $N_0 = 10^{21}$ cm^{-3}.

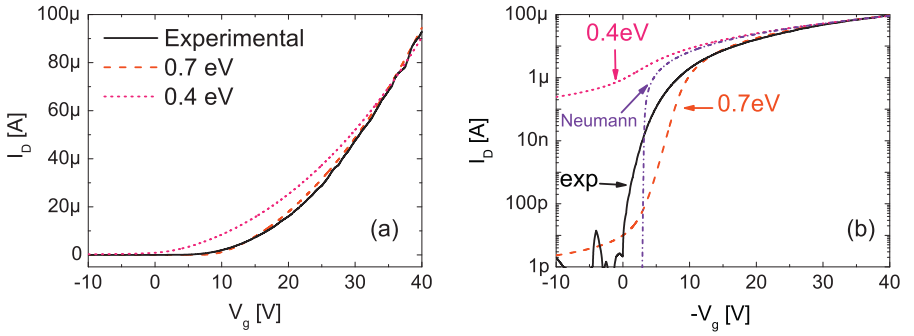

Fig. 14. Simulated and measured transfer characteristics curves of a PBTTT-based TFT: on linear scale in panel (a) and on logarithmic scale in panel (b). Using at the substrate/semiconductor interface the same boundary condition of the MIS capacitor, viz. $\Phi_B \simeq 0.4$ eV the current is overestimated and the subthreshold slope underestimated; using a Neumann boundary condition both the current in accumulation and the subthreshold slope are overestimated. By using $\Phi_B = 0.7$ eV, estimated from the simulation of 1D metal/semiconductor/metal structures, a very satisfactory fitting of experimental curves is obtained. Other simulation parameters: $\mu_0 = 2.08 \times 10^{-2}$ cm^{2}V^{-1}s^{-1}, $\sigma = 98$ meV, $N_0 = 10^{21}$ cm^{-3}.

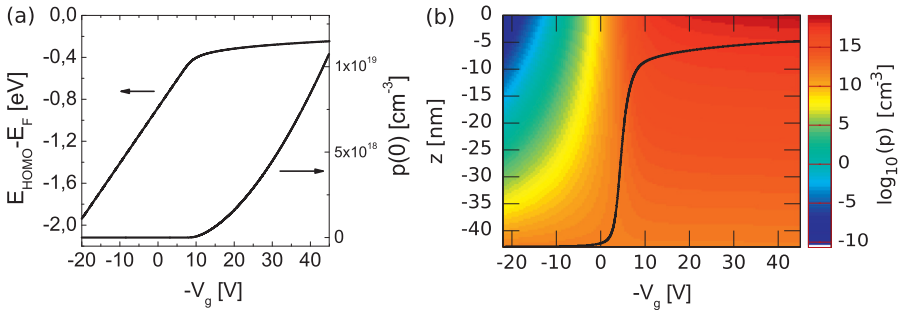

Fig. 15. Results of DC simulation of a PBTTT-based TFT. Panel (a) shows HOMO level and carrier density at the semiconductor/insulator interface as function of V_g. Panel (b) shows charge carrier density as a function of position and applied voltage; the solid line represents the channel depth, which is equal to -4.75 nm at $V_g = -45$ V.

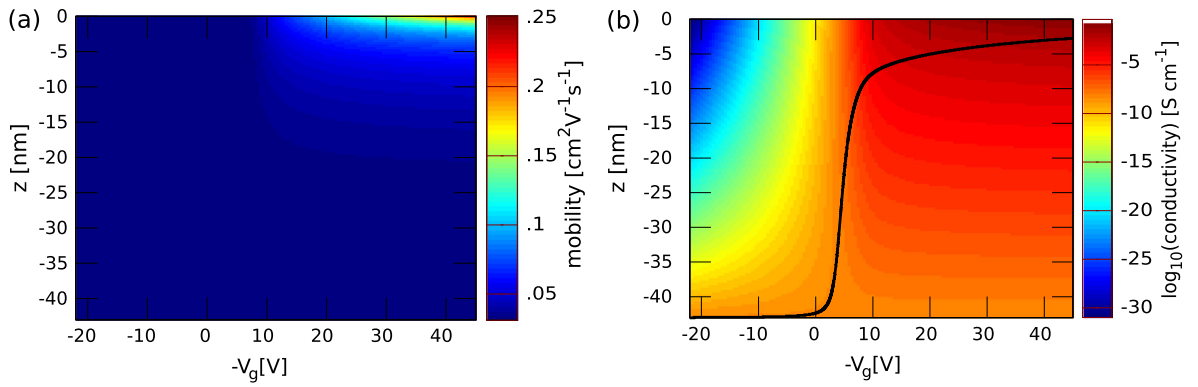

Fig. 16. Results of DC simulation of a PBTTT-based TFT. Panel (a) shows mobility as a function of position and applied voltage. Panel (b) shows conductivity as a function of position and applied voltage. The solid line in panel (b) represents the current depth, which is equal to -2.78 nm at $V_g = -45$ V.

From the PBTTT case we learn that the larger is the disorder, the larger is the dependence on V_g of both $\mu_{p,eff}$ and Q_{ch}. From the point of view of the experimentalist, a strong non-linearity in the transfer characteristic curve suggests that the semiconductor is disordered, but it would be wrong to assume that the origin of such non-linearity could be entirely and solely traced back to the mobility, as this would lead to an overestimation of the DOS disorder. This once again highlights that the deduction of the DOS from *transport* measurements can be an ill-defined approach.

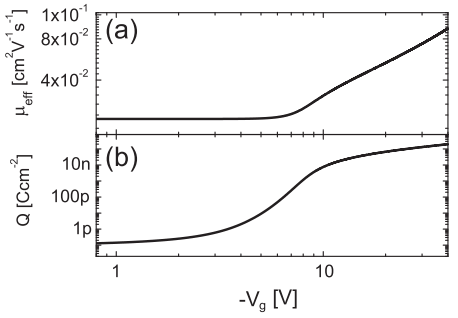

Fig. 17. Results of DC simulation of a PBTTT-based TFT: panel (a) shows effective mobility (see Eq. (6)), as a function of applied voltage; panel (b) shows total accumulated charge (see Eq. (5)) as a function of applied voltage.

4. Conclusions

Metal/Insulator/Semiconductor structures have been exploited as test beds to extract the DOS width. As an advantage with respect to other techniques based on electrical measurements, DOS extraction is completely disentangled from transport phenomena, thanks to the fact that the MIS capacitor is operated under quasi equilibrium conditions. By numerical fitting of experimental Capacitance–Voltage curves, we have extracted the DOS width under the hypothesis it has a Gaussian shape. Other functional forms recently suggested in the literature [8,16,80–82,39,83,38] will be the subject of future investigations, thanks to the fact that our approach is indeed general and not restricted to Gaussian functions.

We considered two paradigmatic case studies, the n-type polymer P(NDI2OD-T2) and the p-type polymer PBTTT, and we find that the Gaussian ansatz for the DOS leads to very satisfactory fittings. To validate our approach, we have varied the insulator electrical permittivity and we have verified that the extracted DOS widths are robust against variations of this parameter. We extract $\sigma \simeq 78$ meV for P(NDI2OD-T2) and $\sigma \simeq 98$ meV for PBTTT, despite the fact that the latter is generally considered to be far more ordered than the former from a structural point of view. Indeed, it has been recently underlined that PBTTT displays a remarkable crystallinity in the lamellar-stack direction, whereas along the π-stacking direction, which is mostly relevant to DOS and carrier transport, a sizable disorder is present [78]. The higher disorder of PBTTT results in a channel depth close to 5 nm (whereas it is less than 2 nm in P(NDI2OD-T2)), a value that is remarkably larger than what conventional wisdom suggests: with very few exceptions [84], the effect of disorder on the accumulated channel thickness is generally overlooked in the literature.

Finally, by plugging the extracted DOS width in the Extended Gaussian Disorder model for carrier transport, we successfully predict the functional dependence of transfer characteristic curves in the linear regime of P(NDI2OD-T2)- and PBTTT-based Thin Film Transistors. Interestingly enough, we observe that in the case of PBTTT, not only the dependence of the effective (viz. averaged across the film thickness) mobility is sizable, but also the dependence of the total accumulated charge on the gate voltage becomes non-negligible. These two effects sum up giving rise to a strong super-linearity in the TFT transfer characteristic curve, but they can be easily disentangled by independently assessing the DOS. By exploiting MIS structure as testbeds the DOS width can be reliably and accurately assessed with a relatively simple experimental setup.

Acknowledgments

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Appendix A. P(NDI2OD-T2): σ sensitivity to material parameters

A.1. Sensitivity to Φ_B

In Section 3.2 Φ_B has been assumed equal to 1 eV considering the nominal values for the LUMO level of P(NDI2OD-T2) (4 eV) and for Au work function (5 eV). Indeed these levels are affected by a certain degree of uncertainty: according to Ref. [36] the LUMO level is expected to be 3.8 ± 0.1 eV; according to Ref. [85] Au work function lies in the range 4.7–5.1 eV. By taking into account the reported uncertainties, a confident range for Φ_B is 0.8–1.4 eV.

To investigate the sensitivity of σ to Φ_B experimental CV curves of P(NDI2OD-T2)-based MIS capacitor have been fitted by varying Φ_B in the range 0.4–1.2 eV. Results are reported in Fig. A.1: for relatively large barriers ($\Phi_B \geqslant 0.7$ eV) σ is barely sensitive to Φ_B. For smaller barri-ers, viz. $\Phi_B \leqslant 0.7$ eV, the smoothness of the experimental curve is partially accounted for by the thermal carriers injected from the bottom metal contact, and the fitted σ

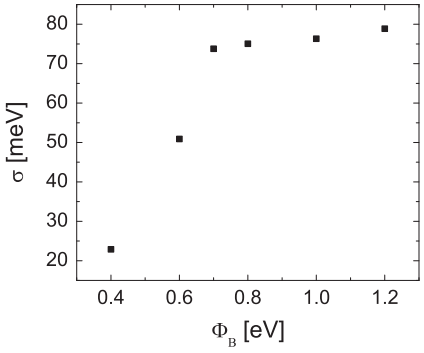

Fig. A.1. Sensitivity of σ to Φ_B for P(NDI2OD-T2)-based MIS capacitor. Measurement frequency 9283 Hz.

diminishes steeply. We note that the estimated range for Φ_B is in the regime where σ is barely influenced by Φ_B.

A.2. Sensitivity to N_0

In Section 3.2 N_0 has been assumed equal to 10^{21} cm^{-3}, a value commonly accepted as a rough estimation of N_0 for organic semiconductors. To investigate the sensitivity of σ to N_0 experimental CV curves of P(NDI2OD-T2)-based MIS capacitor have been fitted by varying N_0 in the range 10^{19}–10^{22} cm^{-3}, as shown in Fig. A.2. Fitted σ is an increas-ing function of N_0: the larger N_0 the steeper the DOS tail so that to account for experimental CV curves a larger σ is needed. Quantitatively speaking, the sensitivity of σ is relatively mild: by changing N_0 by three orders of magnitude σ grows from about 50 meV to 80 meV.

Indeed a more precise estimation for P(NDI2OD-T2) can be done. Considering that the density of P(NDI2OD-T2) is equal to 1.18 gcm^{-3}[86], the monomer weight is 937.39 gmol^{-1}, and assuming a maximum of one charge per monomer, we can estimate $N_0 = 7.58 \times 10^{20}$ cm^{-3}, indeed not far from the assumed 10^{21} cm^{-3}. With this value for N_0 the fitted σ diminishes by less than 4 meV.

A.3. Sensitivity to doping

In Section 3.2 P(NDI2OD-T2) has been assumed to be intrinsic. To evaluate the impact of unintentional doping (for example due to ambient contamination) on the extraction of σ, experimental CV curves have been fitted by modifying Poisson equation to take into account the presence of dopants. We assumed dopants to act as donors and to be completely ionized. Dopant concentration N_d in the range 10^{15} cm^{-3}–2×10^{17} cm^{-3} has been explored. Results are reported in Fig. A.3. We can identify three regimes: for a lightly doped film ($N_d \leqslant 10^{15}$ cm^{-3}) the best fitting value for σ is equal to the one obtained assuming $N_d = 0$ cm^{-3}; for an intermediate doping degree (5×10^{16} cm^{-3} $\leqslant N_d < 2 \times 10^{17}$ cm^{-3}) σ turns out to be a decreasing function of N_d; for a highly doped film ($N_d \geqslant 2 \times 10^{17}$ cm^{-3}) experimental CV curves cannot be fitted at all. We can therefore conclude that the extraction of σ is robust if doping is low or high: in the former case the doping level does not affect the value of σ, whereas in the latter case the assumed doping level leads to the failure of the fitting.

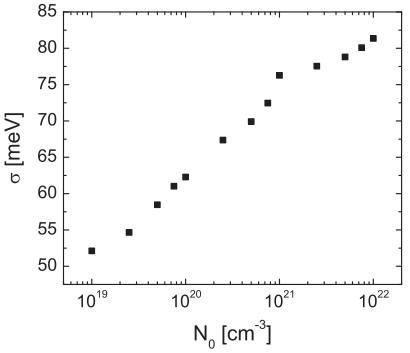

Fig. A.2. Sensitivity of σ to N_0 for P(NDI2OD-T2)-based MIS capacitor. Measurement frequency 9283 Hz.

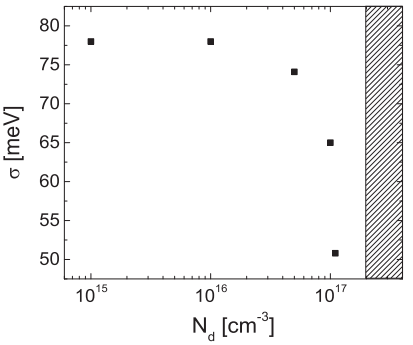

Fig. A.3. Sensitivity of σ to N_d for P(NDI2OD-T2)-based MIS capacitor. Measurement frequency 9283 Hz.

There remains an intermediate and relatively narrow region where σ is sensitive to N_d. The sensitivity of σ on N_d increases approaching the limit $N_d = 2 \times 10^{17}$ cm^{-3}. On the basis of CV measurements we exclude a doping density in excess of 2×10^{17} cm^{-3}. To further reduce the doping range compatible with experimental measurements, TFT transfer characteristic curves could be exploited. In fact doping-induced conduction is expected to affect TFT behavior especially at low V_g when the transistor channel is barely formed and current is predominantly carried through the whole film thickness. Preliminary fittings show that even a light doping such as 10^{15} cm^{-3} leads to a worse fitting of TFT curves, thus suggesting an actual film doping below 10^{15} cm^{-3} and corroborating the accuracy of σ extracted assuming doping to be negligible. The topic is beyond the current scope of the paper and will be the subject of future investigations.

A.4. DOS broadening effect induced by the insulator

The insulating dielectric layer in the MIS capacitor is an additional source of disorder for the semiconductor DOS, because of the potential landscape due to randomly oriented insulator permanent dipoles [87]. To evaluate the impact of this phenomenon on DOS extraction we have calculated the insulator-driven DOS broadening according to the model developed in Ref. [82] considering the dipole density and strength of PMMA (7×10^{21} cm^{-3} and 1.97 D respectively). Far from the semiconductor/insulator interface the DOS is unaffected by insulator dipoles: we assume its width to be 78 meV, as extracted in Section 3.2. Broadening becomes sizable close to the semiconductor/insulator interface, where σ approximately is doubled. But since the effect is confined within 1 nm from the interface (see Fig. A.4), CV curves obtained by simulation using this space-dependent DOS do not appreciably differ from those where the insulator broadening effect is neglected. We therefore conclude that, within the model developed in Ref. [82] and relatively to PMMA used as insulator, our approach is mostly sensitive to the bulk DOS.[2,3]

[2] Even doubling the insulator dipole strength or density does not produces effects on CV curves.

[3] As to the carrier mobility the converse is true, viz. the sensitivity to insulator-driven disorder is expected to be high since the DOS broadens just in the region carrying most of transistor current.

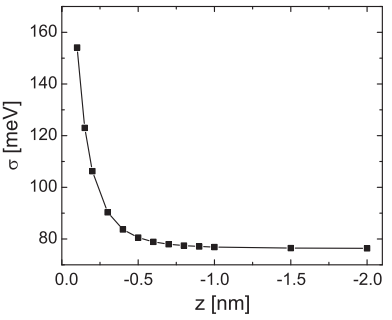

Fig. A.4. DOS broadening due to insulator dipoles as function of space, calculated according to the model developed in Ref. [82] for P(NDI2OD-T2)-based MIS capacitor.

Appendix B. Supplementary material

Supplementary data associated with this article can be found, in the online version.

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