# Editorial

It is with great pleasure that we introduce this special issue on Manufacturable and Dependable Multi-core Architectures at Nanoscale (MEDIAN) to the audience of Elsevier Microprocessors and Microsystems.

MEDIAN (http://www.median-project.eu/) is a funded COST Action (IC1103) of the framework of the European Science Foundation (ESF) aimed at creating a European network of competence and experts on all dependability aspects of future digital systems development, with a specific interest for multicore architectures. The Action has fostered workshops co-located with European conferences and symposium on related topics, and its second edition has been held in Avignon, co-located with the European Test Symposium 2013. This Special Issue includes some works from such an event, as well as other contributions tackling one of the topics of interest of the MEDIAN scenario.

Six papers have been selected for publication, covering from degradation processes to vulnerability analysis for guiding the designers in selecting the most appropriate hardening strategies, from arithmetic units to system level strategies including Network on Chip aspects.

While in the past dependability has attracted a lot of attention for safety- and mission-critical application environments, in the last decades it has become a fundamental aspect in most contexts, because of the widespread adoption of electronic devises in everyday life and our resilience upon them for a multitude of activities. More precisely, the quest for reliable computing resources has increased for the entire spectrum, from embedded systems to high-performance computing ones.

In this scenario, academia and industry are joining forces to find solutions enabling designers to (i) analyze the systems being designed with respect to the occurrence of faults either during the production process or while in field, and (ii) harden them in order to detect and possibly mitigate faults' effects.

These papers address both analysis and hardening issues, addressing several of the issues of interest for future multicore architectures.

Paper "A New Method for In-Situ Measurement of Parameters and Degradation Processes in Modern Nanoscale Programmable Devices" by Petr Pfeifer and Zdenek Pliva introduces a new approach for evaluating degradation processes in FPGAs, exploited as a reconfigurable platform for the implementation of multicore systems. The authors propose an in-situ low-cost method achieving interesting results with a limited implementation complexity.

At a higher abstraction level, paper "Bit Impact Factor: Towards Making Fair Vulnerability Comparison", by S. Zafer Can, G. Yalcin, O. Ergin, O. Unsal and A. Cristal still deals with analysis issues related to reliability, and in particular the authors propose an alternative metric to the well-known Architectural Vulnerability Factor, to take into account the impact level of each bit.

The paper "Fault-Tolerant Adaptive Routing under an Unconstrained Set of Node and Link Failures for Many-Core Systems-on-Chip" by M. G. Dimopoulos, Y. Gang, M. Benabdenbi, L. Anghel. N.-E. Zergainoh and M. Nicolaidis presents an online fault tolerant routing algorithm for 2D Mesh Networks-on-Chip. The idea behind this work is to combine an adaptive routing algorithm with the neighbor fault-awareness and with a new traffic-balancing metric. The proposed method is able to cope with an unconstrained number of various fault types (permanent, transient, and intermittent). The extensive set of simulations presented in the paper give to the reader useful insights on the efficiency of the proposed algorithm.

The paper "Multiple Detection Test Generation with Diversified Fault Partitioning Paths" by Stelios Neophytou and Maria K. Michael discusses a novel algorithm for vector test generation that is able to increase the fault coverage detecting each modeled faults multiple times. This technique has been proven to give high non-modeled fault coverage and, thus, higher test quality. The proposed algorithm introduces a new systematic test generation algorithm for multiple-detect test sets that increases the diversity of the fault propagation paths excited by the various tests per fault. The algorithm tries to identify different propagating paths (if such path exist) for each one of the multiple detections of the same fault. The paper reports a series of experimental results that shows the effectiveness of the approach compared to traditional n-detect test sets.

The paper "A fault-injection methodology for the system-level dependability analysis of multiprocessor embedded systems" by Antonio Miele deals with a framework for system-level dependability analysis based on fault injection. It features an error analysis approach offering the designer the possibility to specify custom monitoring and classification actions at both application and architecture levels. The proposed methodology has been automatically implemented within a state-of-the-art SystemC/TLM simulation platform for multiprocessor specifications provided with a fault injection engine and evaluations have been demonstrated for different test cases.

Last but not least, the paper "Exploiting Processor Features to Implement Error Detection in Reduced Precision Matrix Multiplications" by Pedro Reviriego, Serdar Zafer Can, Çağrı Eryılmaz, Juan Antonio Maestro and Oğuz Ergin presents a technique to implement error detection in matrix multiplications. The approach considers the implementation of reduced-precision matrix multiplication on a processor with extended precision arithmetic units. The paper shows that by using arithmetic residue codes it is possible to efficiently implement 100% fault detection in all

studied configurations. This technique is a starting point for the extension to other common computer applications that make an intensive use of the processors arithmetic units.

We take this opportunity to thank the MEDIAN community, a body of European researchers from the academic and industrial field, for the contribution and participation in this action, fostering research and networking.

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