Silicon algae with carbon topping as thin-film anodes for lithium-ion microbatteries by a two-step facile method

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Received 7 August 2014
Received in revised form
11 September 2014
Accepted 22 September 2014
Available online 7 October 2014

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1. Introduction

With rapid advances in the fields of microelectronic devices, microsensors, micromachines, RF-ID tags, MEMS, and drug delivery systems, the development of integrated power sources that enable the continued device operation is of great importance. To meet these demanding applications, microbatteries with high energy and power per unit area are urgently required and in this context lithium-ion technology is very promising. It is more important for microbatteries to achieve high capacity per footprint (mAh cm^{-2}) than per unit weight (mAh g^{-1}) or volume (mAh L^{-1}) [1,2]. In addition, the microbattery fabrication process should be compatible with state-of-the-art integrated circuit (IC) techniques, to lower the cost.

In order to further improve the areal capacity of microbatteries, three-dimensional (3D) nanostructured electrodes have been developed and investigated [3–8] which are generally realized by vacuum deposition or electroplating of active material onto a 3D metallic current collector, usually made of Ni or Ti, which are more expensive than conventional Al and Cu foils. In addition, 3D electrode fabrication usually involves wet chemistry, such as hydrothermal synthesis or etching, which is not compatible with the current IC technology. Therefore, when taking cost, complexity, and incompatibility into consideration, 3D nanostructured electrodes need more development to pitch into the microbattery market.

Besides the 3D concept, research is also heading for different materials with higher capacity. Silicon alloys with lithium up to $Li_{15}Si_4$ [9,10] at room temperature, this resulting in almost 10 times larger a capacity (3579 mAh g^{-1} for $Li_{15}Si_4$) than that of graphite (372 mAh g^{-1} [11]), which is the standard commercial material for negative electrodes. However, Slurry coating of Si-based anodes is mainly facing two drawbacks. First, they suffer from poor cycle life due to detrimental volume changes (i.e., theoretically up to 280% volume expansion [12]) of the host lattice upon alloying and de-alloying with Li. Extended fractures lead to a complete loss of electrical contact between active material and current collector and to pulverization. Second, the SEI layer formed by silicon in contact with common electrolytes is generally unstable and it detrimentally impacts the capacity retention [13,14].

At the state of the art, research works on strategies to cope with Si cracking, such as replacing bulk with porous materials [15], engineering the empty space [16], reducing amorphization-induced mechanical stresses by using non-crystalline silicon [9,17–19] or fabricating composite anodes where Si is mixed with other less-active materials that can buffer its volume expansion [20].

More in detail, nanoporous silicon has been investigated as a suitable material for enhancing LIB performances, for voids can effectively accommodate the volume expansion, as described by Wu and Cui [21]. Usually, porous silicon is obtained from bulk via electrochemical etching with hydrofluoric acid; the porous film is then used either as it is [15] or after ball-milling and mixing with other materials, such as C polymeric binders [22–26]. Recently, Liu et al. [27] adopted the strategy of covering Si nanoparticles with a thin C layer that acts as a stable interface towards the electrolyte; in addition, their pomegranate-inspired design aims to engineering some void space within the core–shell structure for Si to expand.

Combining Si with other less-lithium-active materials is introduced as an effective strategy [20]. Examples show that SiO_2 coating on Si improves capacity retention during cycling by buff-ering volume expansion and confining the detrimental activity of HF possibly evolving from electrolyte decomposition [28–30]. Even more promising is the route of composite anodes made of Si and C, whether they be in the form of mixed micrometrical-sized powders with C black and other additives [31–35], or in especially designed 3D nanostructures where C covers Si as a shell [21,36–40]. However, the sophisticated methodologies reported in these latter works generally require the use of expensive and extremely haz-ardous chemicals, such as HF or SiH_4 gas, and multistep treatments to tailor the anode nanostructure.

In alternative, physical vapour techniques are used to grow silicon nanostructures, as for example the Vapour–liquid–solid method for 1D-nanorods [38] or the Glancing Angle Deposition. This latter allows to grow porous silicon in the form of columnar films to enhance its electronic transport [41], introducing, though, limitation in its thickness (300–500 nm).

So far, silicon planar thin-film anodes for microbatteries can only be realized within sub-μm thickness [41–45], leading to low areal capacity. Therefore, it is of importance to develop Si thin film anodes with enhanced areal capacity compared to 3D nanostructured electrodes, meanwhile offering a long and stable lifetime by managing mechanical instability due to volume changes.

In this work, we address the two main drawbacks of silicon anodes in lithium ion microbatteries by a two-layer architecture obtained by a facile two-step method. We fabricated novel nanocomposite Si–C anodes by depositing nanostructured porous amorphous Si films by Pulsed Laser Deposition (PLD) at room temperature, followed by Chemical Vapour Deposition (CVD) of a thin carbon coating. The mesoporosity of the nanostructured Si films and its lack of crystallinity are expected to reduce the detrimental effects of volume variations and to avoid mechanical stressing due to amorphization in the first cycles. The thin CVD-grown carbon layer, then, is expected to promote the formation of a stable solid electrolyte interphase (SEI) layer and protect Si from direct contact with the electrolyte. Rather than covering the whole Si surface area with C, we propose an alternative anode structure where the formation of SEI is shifted away from the active silicon; this simple architecture allows for a straightforward two-step process that presents so far no upper limits to the obtainable film thickness.

2. Experimental

2.1. Film fabrication

In order to grow mesoporous hierarchical silicon films by PLD at room temperature, a rotating and translating monocrystalline <100>n + doped silicon wafer target was ablated by a KrF laser beam (λ = 248 nm, pulse energy 400 mJ, pulse duration 20 ns, repetition rate 20 Hz) with a fluence of ~5 J cm^{-2} and the ablated material was collected on copper discs (1.3 cm diameter).

As a background process gas, a mixture of Ar and H_2 (<3 vol.%) was inserted in the chamber while vacuum pumping, so to dynamically set the process gas pressure either at 60 Pa or 100 Pa, thus controlling the morphology of the grown film. The role of H_2 in the gas mixture is to passivate the Si surface.

Target-to-substrate distance was fixed to 50 mm and during deposition the substrate holder was rotated to widen uniformity over the deposition area. Deposition was carried out with the substrate at room temperature (see Table SI1 in supporting information for a summary of the investigated samples and their deposition conditions).

For CVD, the samples were loaded into a quartz tubular furnace where a mixture of H_2 and N_2 gas (6 sccm and 100 sccm, respectively) was fluxed while ramping the temperature up to 825 °C at the rate of 10 °C min^{-1}. After stabilization of the temperature (15 min), ethylene was added (20 sccm) during 5 min (or 7 min in the case of thicker sample) to the gas mixture, as a precursor for carbon deposition. After this time, the previous gas atmosphere of H_2 and N_2 was restored during the whole cooling down step. In addition to substrates previously covered by the Si film, some bare Cu substrates were also loaded into the furnace for the same coating process in the same conditions, so to get pure C(CVD) an-odes to be used in reference cells.

Process temperature for the CVD was chosen to be right above the threshold for the ethylene decomposition but low enough to avoid any possible effect of recrystallization of the amorphous Si layer underneath. As for the reaction time, it was adjusted so to

result in the formation of a continuous thin layer on top of the Si film as later shown in SEM pictures.

2.2. Cell assembling and electrochemical testing

Electrochemical measurements were carried out using an Arbin 2000 battery test station. All cells were assembled in an Ar-filled glove-box using the porous nanostructured Si and Si–C thin films as the working electrodes and lithium metal foil as the counter-electrode. The electrolyte was 1 M $LiPF_6$ dissolved in a 1:1 (volume ratio) mixture of ethylene carbonate (EC) and diethyl carbonate (DEC); the separator was a glass micro-fibre disc (Whatman GF/F), and the shell was a stainless steel CR2032 coin cell (VWR Inter.).

2.3. Electron microscopy (SEM, TEM) and energy-dispersive X-ray spectroscopy (EDS)

Thickness and morphology of the Si films were investigated by a Supra 40 Zeiss Scanning Electron Microscope (SEM, accelerating voltage 2–4 kV), before C deposition, for samples fabricated for this purpose on Si substrates previously coated by a 100 nm thick Al layer.

In order to evaluate the film morphology and composition after C deposition, before and after electrochemical testing, High Resolution Scanning Electron Microscopy (HRSEM) investigations were performed on [Si60 + C(CVD)] with a JEOL JSM-7500F instrument, equipped with a cold field emission gun source operating at 10 or 15 kV. Energy-Dispersive X-ray Spectroscopy (EDS) compositional analysis was carried out using an Oxford Instrument silicon drift detector (SDD) X-Max80 (80 mm^2 effective area of detecting device) mounted on the HRSEM instrument.

TEM analysis was performed on the same samples, which were scratched from the substrate by means of a diamond tip and dropped onto a commercial holey carbon-coated Cu grid. In case of the sample subjected to electrochemical testing, the preparation was carried out in a N_2-filled glove box, so as to limit the air exposure time to only few minutes before insertion into the TEM. The analyses were carried out with a JEOL JEM 2200FS instrument, operated at 200 kV, equipped with a Scanning TEM (STEM) unit. EDS compositional and spectral maps were recorded simultaneously with the acquisition of High Angle Annular Dark Field (HAADF-STEM) images, using a Bruker Quantax 400 system with a 60 mm^2 XFlash 6T SDD.

3. Results and discussion

Mesoporous hierarchical silicon films were grown by PLD at room temperature under two different background gas pressure conditions, namely 60 or 100 Pa, so to give different film morphologies. Some of the Si films were then subjected to covering by a carbon layer grown by CVD. For the reader's convenience, we use the notation [Si(xx)] or [Si(xx) + C(CVD)] to designate samples where Si is deposited by PLD at 'xx' pressure, without or with C coating by CVD, respectively.

Both [Si60] and [Si100] exhibit the typical morphology of hierarchically nanostructured mesoporous films, preferentially grown in the direction perpendicular to the substrate into an algae-like shape, as reported in a previous work [46]. The increase of processing gas pressure during the PLD process leads to an increase in the film porosity, with an estimated density of 0.92 g cm^{-3} for [Si60] and 0.36 g cm^{-3} for [Si100] [46].

Nominal thickness of Si films was set to 1 μm; in addition, for one chosen set of parameters, a thicker anode (2.5 μm) was also prepared with PLD silicon and CVD carbon layer, in order to prove the feasibility of increasing the anode capacity by increasing its thickness without any negative effects on the mechanical stability.

The electrochemical behaviour of the anodes was then studied in half-coin cell configuration with Li metal as counter electrode

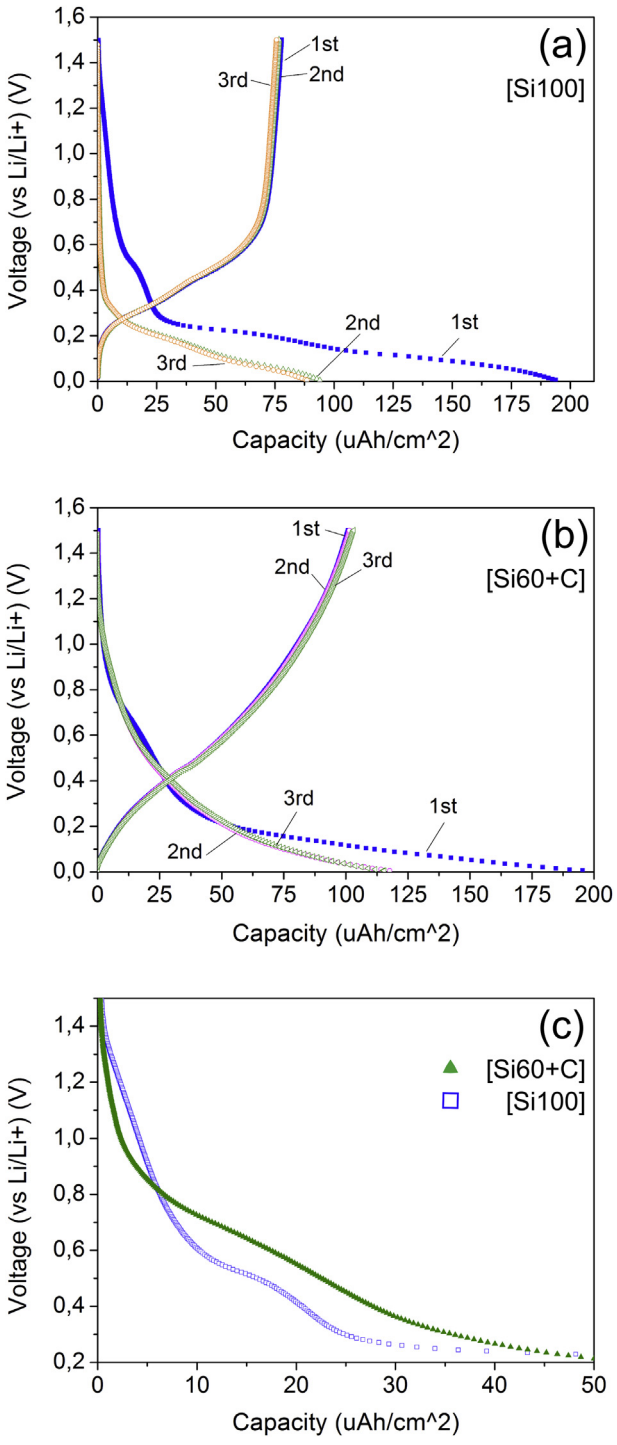

Fig. 1. First three cycles charge/discharge curves of samples (a) [Si100] and (b) [Si60(PLD) + C(CVD)]. In (a), the plateaus of amorphous silicon lithiation (discharge) and delithiation (charge) are clearly visible. In (b), the small plateau around 0.7 V in lithiation is attributed to the SEI formation at the C-electrolyte interface; 2nd delithiation curve completely overlaps to 1st delithiation curve. (c) Zoomed first lithiation curves of [Si100] and [Si60(PLD) + C(CVD)] in the voltage range of SEI formation (1.0 V–0.4 V). The difference in shape and slope of the two curves highlights a different mechanism of SEI formation in the two samples.

between 5 mV and 1.5 V or 50 mV and 1.5 V, under constant-current conditions. At the end of each delithiation, we applied a constant-voltage for 10 min.

The charge/discharge curves of the first three cycles, measured between 5 mV and 1.5 V versus Li/Li^+ at a current density of 54 μA cm^{-2}, are shown in Fig. 1(a, b) for samples [Si100] (pure silicon) and [Si60 + C(CVD)]. The first lithiation curve in Si[100](Fig. 1(a)) shows a rapid drop of the potential with two plateaus: the first one, around 0.5 V, can be related to the SEI formation, that concurs to irreversible capacity losses; the second one, around 0.3 V is attributed to lithiation of amorphous silicon. In delithiation curves, the two steps around 0.3 and 0.5 V are attributed to low and high voltage delithiation of amorphous silicon [47]. The first discharge capacity is about 195 μAh cm^{-2} with an initial coulombic efficiency of 42% (see Table 1).

In the lithiation curve of [Si60 + C(CVD)], (Fig. 1(b)), the small plateau around 0.7 V is related to the formation of the SEI layer on the carbonaceous electrode surface [48], while the change in slope around 0.3 V is associated to the lithiation of amorphous silicon, as in the previous case. Below 0.2 V also lithiation of carbon plays a role [49]. From the 2nd cycle on, no plateau is observed during lithiation, which is the typical voltage profile of Li insertion/extraction in amorphous structure materials without phase transformation. These observations are consistent with other works [50,51]. In delithiation profiles the smooth change in slope around 0.5 V can be ascribed to delithiation of a-Li_xSi to a-Si, as in the previous case. The first discharge capacity is about 195 μAh cm^{-2} with an initial coulombic efficiency of 55%, this value showing improvement as against pure Si sample (see Table 1). The charge and discharge capacities in the subsequent cycles at the same rate are highly reversible with a discharge capacity about 115 μAh cm^{-2}. Similar curves feature all the analysed C-coated Si samples (not shown).

For more clarity, data of coulombic efficiency and capacity fade (first 3 cycles) of the two samples are reported in Table 1.

In Fig. 1(c), 1st lithiation curves of [Si100] and [Si60 + C(CVD)] have been zoomed in the potential range from 1.4 V to 0.3 V, typical of SEI layer formation. The strong discrepancy in slope and shape of the two curves evidences that the mechanisms driving SEI formation in the first half-cycle are different, according to the material facing interaction with the electrolyte, either Si or C. The capability of C(CVD) of forming a stable SEI layer can be observed in the good overlap between 2nd and 3rd lithiation curves in Fig. 1(b), unlike the case of [Si100].

All this proves how the beneficial role of C layer be crucial for the formation of a stable and protective SEI layer, hence for a sensitive reduction of irreversible capacity losses.

In Fig. 2 cyclic charge/discharge curves of the anodes under analysis are presented under different testing conditions together with coulombic efficiency. Cycling was performed under constant-current density with step-increasing values every 15 cycles, so to test the rate capability. The voltage range was either limited to a cut-off voltage of 50 mV or extended to 5 mV.

Fig. 2(c) and (e) refer to sample [Si100 + C(CVD)] under different voltage range, while Fig. 2(d) and (f) refer to [Si60 + C(CVD)]. Fig. 2(a) shows the reference data of [Si100] without C layer, while data in Fig. 2(b) are recorded on the [ThickSi100 + C(CVD)] sample.

As from Fig. 2(a), the poorer performances of [Si100] are improved in terms of stability by the addition of C coating by CVD. The C layer dramatically enhances the capacity retention upon cycling, as evidenced by comparing the graphs in Fig. 2(a) and (c). The behaviour of an anode made of pure C(CVD) film, deposited under the same conditions of C(CVD) coatings, was also tested as reference (not shown) and gave capacity always below 10 μAh cm^{-2} for current densities in the same range.

In comparing the two kinds of anode with different Si morphology and CVD-deposited C (Fig. 2(c)–(d) or (e)–(f)), no significant difference is detected in their electrochemical behaviour.

When the cut-off voltage is limited to 50 mV, the carbon coated Si film shows exceptional stability at different current densities for both morphologies, grown either at 60 or 100 Pa. Its capacity at 1080 μA cm^{-2} still preserves ~67% of that at 54 μA cm^{-2}, indicating excellent rate capability. Even for cutoff voltage of 5 mV, carbon coated silicon still possesses excellent stability in capacity retention and mechanical integrity, as shown in Fig. 2(f), where a capacity of ~75 μAh cm^{-2} is maintained at 540 μA cm^{-2} for 1000 cycles.

The low cutoff voltage of 5 mV is in fact compatible with the formation of the crystalline lithiated phase c-$Li_{15}Si_4$, which takes place around 50 mV and gives the highest theoretical capacity but also the highest volume expansion (3579 mAh g^{-1} and 280%, respectively [12]). More in detail, during discharge, as recently described by Ogata et al. [52], Si alloys with Li into the amorphous phases a-Li_xSi with x increasing with decreasing voltage, up to the value of 3.75 at ~50 mV. Across this potential threshold, the crystalline c-$Li_{3.75}Si$ phase can start to form out of the amorphous counterpart, with a kinetics of nucleation and growth that depends on the discharge rate [53]. In general, below 50 mV c-$Li_{3.75}Si$ and a-$Li_{3.75}Si$ coexist, as well as underlithiated amorphous phases a-Li_xSi ($x = 2$–3.75). Phase change, volume expansion and mismatch between different phases can induce severe mechanical stress upon cycling. Hatchard and Dahn, though, observed that the formation of c-$Li_{3.75}Si$ is suppressed in solid films thinner than ~2.5 μm [53] and Graetz et al. [54] suggested that crack propagation cannot occur if Si particles are 300 nm or less in size. We think this is our case. If each of the Si clusters composing our mesostructure is considered a particle, its diameter is by far smaller than this critical size and we believe no crystalline lithiated phase is then formed, as confirmed by having no degradation at low cutoff voltages, and possibly no cracks propagate in our films.

Because of this reason, these mesoporous silicon-based films made of clusters, can be in principle grown up to films with thickness that overcomes the Hatchard and Dahn's threshold without inducing the formation of c-$Li_{3.75}Si$ phase. The anode capacity can be directly increased by increasing its thickness, without inducing any mechanical side-effect due to possible collapse of the porous nanostructure, as proven in Fig. 2(b) from good stability upon cycling. The highest discharge capacity of ~175 μAh cm^{-2} can be reached at a current density of 54 μA cm^{-2}.

These samples show in general excellent coulombic efficiency (>99%) when reaching stability, indicating that conformal carbon coating on top helps to reduce the contact between electrolyte and high-surface silicon, therefore leading to less SEI formation, i.e. reduced energy losses in side reactions. The initial efficiency is usually around 85% (average on first 5 cycles) and it does stabilize up to its higher value only after some cycles, due to the surface area

Table 1
Coulombic efficiency and irreversible capacity loss (discharge) of samples [Si100] and [Si60 + C] for the first 3 cycles, showing noticeable improvement in the samples topped by C.

Cycle	[Si100]	[Si60 + C]
Coulombic efficiency (%)		
1st	42.1	55.3
2nd	84.0	92.1
3rd	87.9	95.1
Irreversible capacity loss (%)		
After 2 cycles	50.9	39.8
After 3 cycles	54.1	40.9

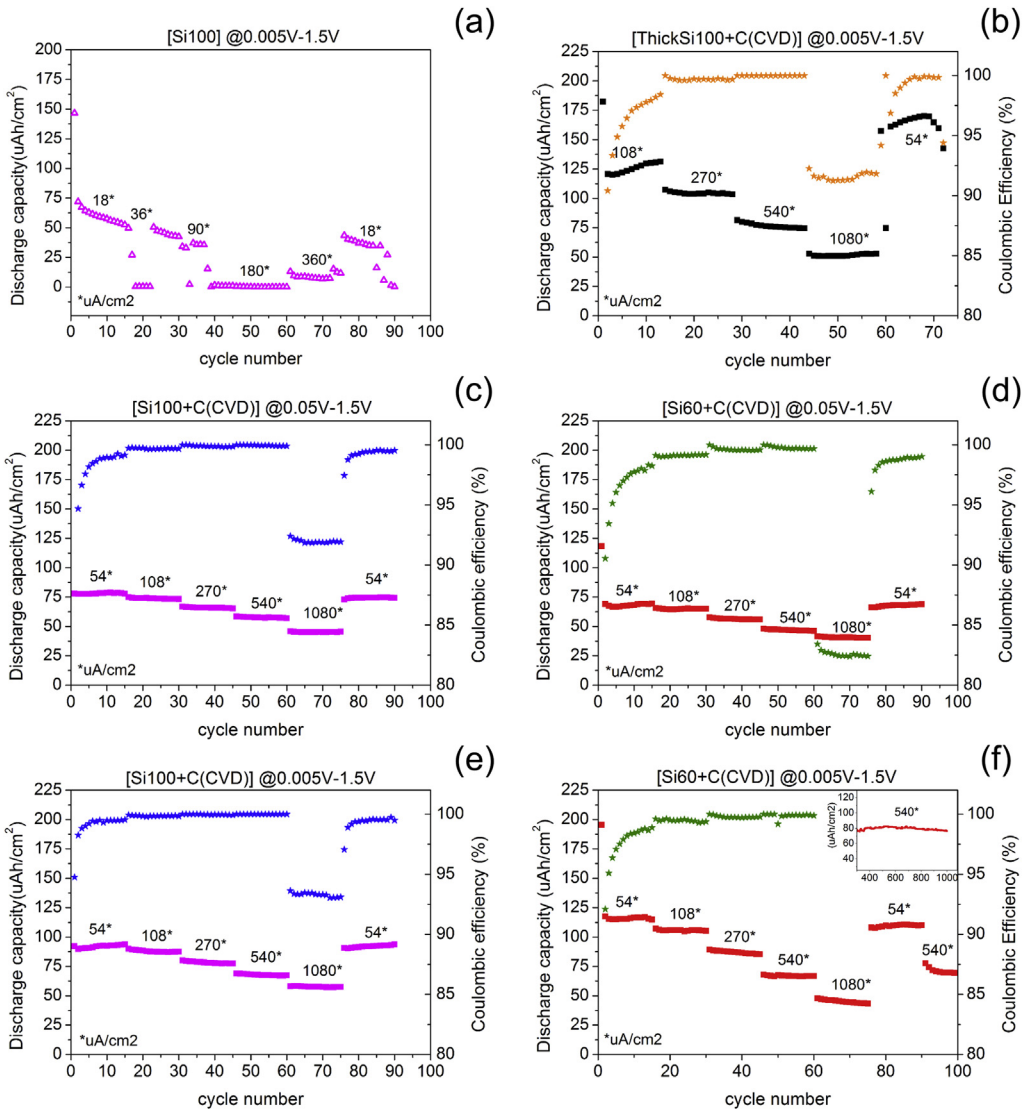

Fig. 2. Curves of discharge capacity (squares) and coulombic efficiency (star) of (a) [Si100] @5 mV; (b) [thick Si100 + C(CVD)] @5 mV; (c) [Si100 + C(CVD)] @50 mV; (d) [Si60 + C(CVD)] @50 mV; (e) [Si100 + C(CVD) @5 mV]; (f) [Si60 + C(CVD) @5 mV]. Integer numbers within the graphs correspond to the constant current density applied, in $\mu A\ cm^{-2}$. Inset in (f) shows long cycle life of [Si60 + C(CVD)] up to 1000 cycles with no capacity decay.

of the nanostructured composite material. Nanoporous silicon itself appears capable of tolerating volume change, as confirmed by the high coulombic efficiency during cycling. At high current density of 1080 $\mu A\ cm^{-2}$, a significant drop of coulombic efficiency is observed and we believe this is due to slow lithium diffusion in silicon not allowing for fast response. For application in microbatteries, however, power density is less critical for usage if compared to areal energy density and lifetime. When then current density is lowered

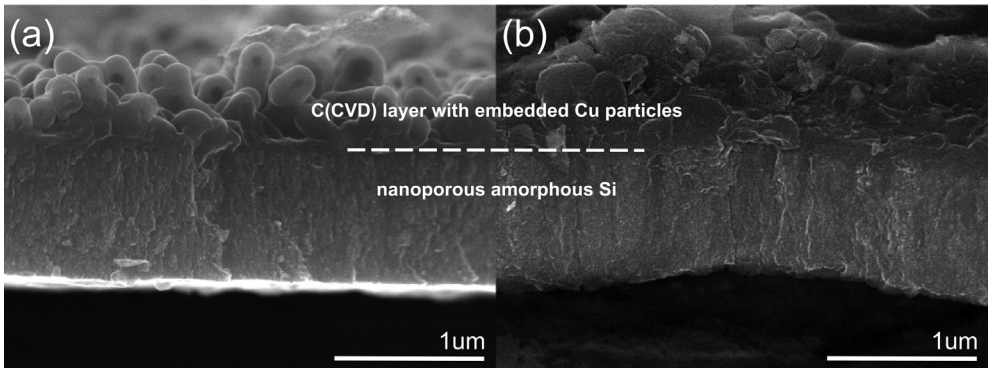

Fig. 3. SEM image of sample [Si60 + C(CVD)], (a) before and (b) after cycling (compare to Fig. 2(f)). The C layer covers the porous amorphous Si (1 μm thick) in a conformal way, without breaking the film continuity.

back again to its initial value, the anodes completely recover their previous capacity and coulombic efficiency, showing that no irreversible damage of the structure, such as cracking or pulverization, has occurred.

In Fig. 3(a) and (b) high-resolution SEM (HRSEM) images of the cross section of [Si60 + C(CVD)], before and after cycling with cutoff voltage of 5 mV, clearly show how CVD-deposited C covers the porous Si layer underneath (1 μm thick) in a conformal way, without any break in the film continuity or any voids separating the two layers.

Wave-shaped deformation in Fig. 3(b) is due to sample preparation, i.e. cell opening and anode separation after cycling. Comparison between Fig. 3(a) and (b) confirms that no trace of damage is induced in the film by testing under the harsher conditions of our analysis, i.e. charge and discharge for 1000 cycles, down to the low cutoff voltage of 5 mV, with current density up to 1080 μA cm^{-2} (see Fig. 2(f)). This can possibly relate to not overcoming the threshold size for cluster crack propagation described above and confirms once more the good robustness of our anodes.

HRSEM, high-resolution TEM (HRTEM) and energy-dispersive X-ray spectroscopy (EDS) analyses on the same samples do not evidence significant compositional, morphological or structural changes of the films between the pre-cycled and post-cycled state, thus allowing for non-separate discussion of the two cases. In particular, electron diffraction analyses, dark-field TEM imaging and HRTEM (not reported here) clearly show the amorphous nature of the Si films, as confirmed by Raman spectroscopic analysis (available in Supporting information).

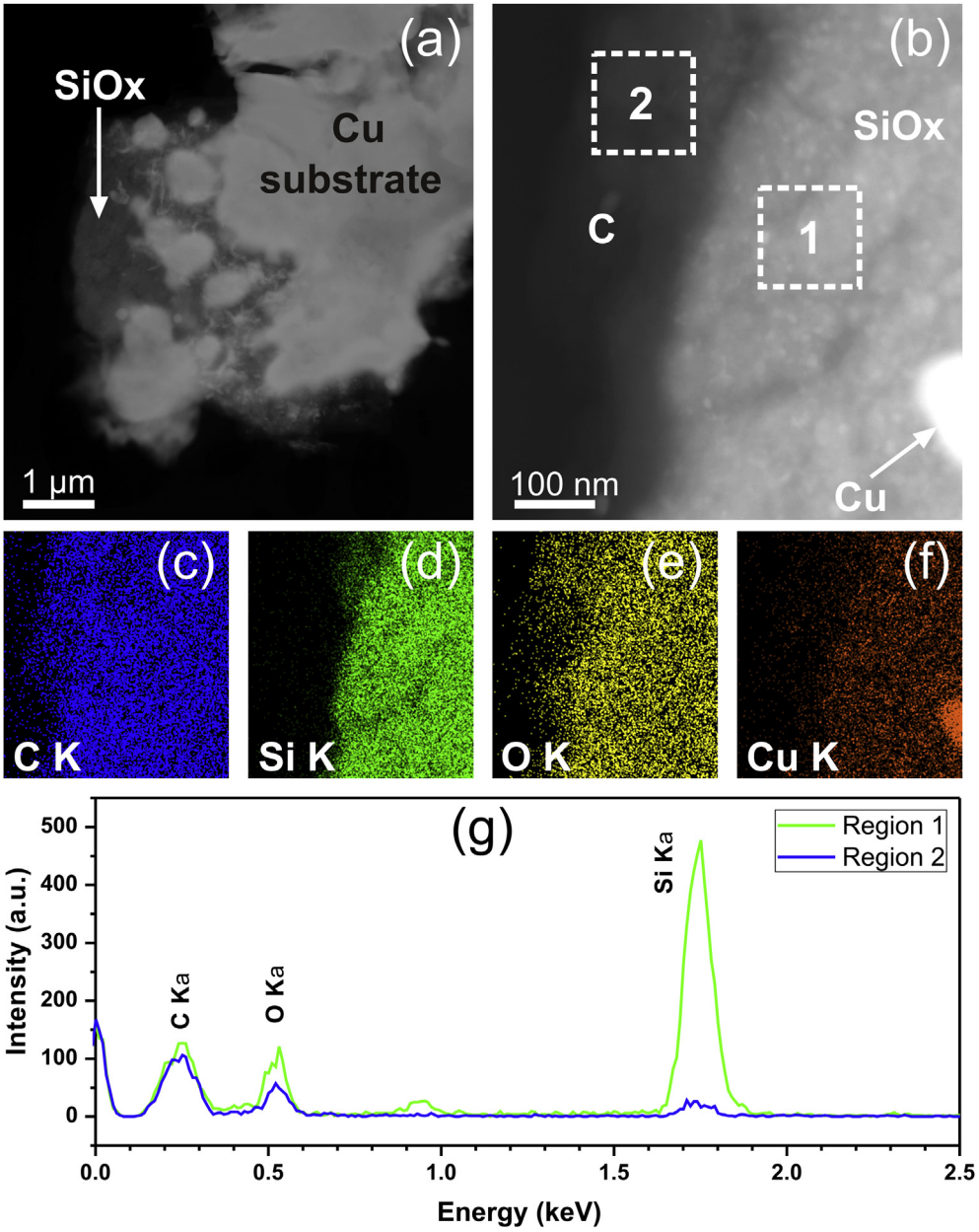

Fig. 4. (a) Low-magnification and (b) magnified HAADF-STEM images of a fragment of sample [Si60 + C(CVD)], lying in plane-view on the carbon support. Three overlapped layers are shown: Cu substrate, SiO_x intermediate layer, C covering layer, as shown by the corresponding (c–f) EDS maps of (c) C, (d) Si, (e) O and (f) Cu, all obtained by integration of the Kα peak. In (g), EDS spectra (not normalized) from regions 1 and 2 of (b), including overlapping of SiO_x with the C film and only the C film, respectively: while the C content is identical in the two regions (i.e., C has not deeply infiltrated the Si layer), the O content is higher in the Si film. Quantification inside the film, after subtracting the spectrum from the C area, results in the ratio Si/O = 3.6.

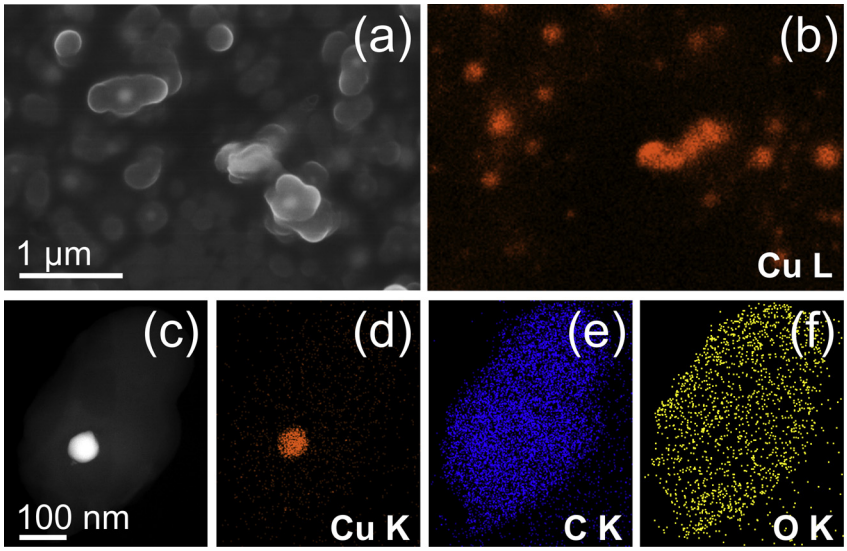

Fig. 5. (a) Top-view SEM image and (b) corresponding EDS map of Cu (integration of the signal in the Lα series) in the globular structures. (c) HAADF-STEM image of a fragment of the covering C film, which includes a ~60 nm diameter Cu particle, and corresponding EDS maps for (d) Cu, (e) C and (f) O (integration of the signal in the Kα peaks).

High-angle annular dark-field-scanning TEM (HAADF-STEM images in Fig. 4(a) and (b) and EDS maps (c–f), taken on the same area as (b), picture the three overlapped layers of: Cu current collector, nanostructured Si film featured by partial oxidation, and C top covering layer.

EDS maps evidence also the presence of nanometric copper grains in C-coated samples, both cycled and non-cycled (Fig. 5).

In order to estimate the oxygen content in the Si film, EDS spectra (Fig. 4(g)) have been recorded on two regions of identical dimension, selected from the area imaged in Fig. 4(b). One spectrum comes from a region where Si and C are overlapped, while the other one is taken on the region where only the upper C layer with no Si is visible. While the C content is identical in the two regions (i.e. the C contribution to the spectra comes only from the C layer rather than from C possibly infiltrated in the Si layer), the O content is higher in the Si film. Estimate of the O content inside Si film, after subtracting the spectrum from the C area, results in the atomic ratio Si/O = 4. This is meant to be an indication value rather than a precise quantification, due to the contribution of the SDD detector itself to the signal (see the low Si Kα peak in the blue (in the web version) spectrum in Fig. 4(g)).

To sum up: on the one hand, introducing a controlled degree of porosity at the nanometric scale in the Si film addresses the problem of volume expansion for silicon (~300%) upon lithiation by creating free space for expansion.

On the other hand, CVD carbon deposition is shown to enhance the mechanical stability of the final anode with respect to the simple Si anode, likely by forming a stable protective SEI layer. Moreover, the moderate temperature required by CVD can benefit the mechanical stability by internal stress relieving via annealing, as recently shown by Hassan et al. [55], and possibly by improving the adhesion of the Si film to the current collector via copper diffusion into Si.

Since from the SEM analysis there is no evident modification of the anode structure and integrity before and after cycling, we claim that the local stresses due to volume changes were not concentrated enough to overcome the threshold for cracking and pulverization. Therefore, we believe that the volume expansion of the Si film has been buffered by the presence of voids in its nanostructure.

The lack of a sharp interface (see Fig. 3) between C and Si, by the two layers being interpenetrated, allows for good electric contact and mechanical adhesion, which again contributes to overall mechanical stability. When C is deposited by CVD, it appears forming in fact a protective conformal layer on Si, which can provide a mechanical barrier to prevent the electrolyte from directly getting in contact with the Si layer underneath, this reducing SEI formation during silicon volume expansion/contraction.

Partial oxidation of Si film as emerges from EDS analysis is also thought to take an active part in the mechanical stability of the anode. As shown in the literature, a certain degree of oxidation can act as a buffer for volume expansion, yet not preventing Si from its alloying with Li in an effective way [56–61].

The presence of Cu within the film, as from EDS analysis, can be explained as a result of the thermal treatment during CVD, which is likely to allow for diffusion of Cu into Si and C [62–65] and then to strengthen the adhesion of Si film to the Cu substrate, to prevent, in principle, the loss of electrical contact between active material and current collector during cycling [66] and to buffer volume expansion of silicon due to its excellent elastic mechanical property [67,68].

4. Conclusions

In conclusion, nanostructured amorphous Si anodes have been produced by PLD in hierarchical mesoporous morphology and successively covered by a C layer deposited by CVD from ethylene. The nanometric porosity allowing for volume expansion and the crucial role of C in the formation of a solid SEI have been exploited by the novel approach we propose.

C top layer and the method to fabricate it have been engineered, so as to result in very promising electrochemical performances. Capacity retention and rate capability were dramatically improved with respect to bare Si anodes, revealing good stability and no decay for at least 1000 cycles (540 $\mu A\,cm^{-2}$). Moreover, the capacity of this anode architecture can be successfully increased by thick-ening the Si + C film without any negative impact on its mechanical stability. We proved an enhanced capacity of ~175 $\mu Ah\,cm^2$ (54 $\mu A\,cm^{-2}$) in anodes as thick as ~2.5 μm. Initial coulombic effi-ciency can be further increased by addition of a layer of alumina deposited by Atomic Layer Deposition, as shown recently [69,70] and/or by the use of additives to the electrolyte, such as Fluoro-ethylene carbonate and Vinylene carbonate, which has proven to promote the formation of a stable SEI and reduce the irreversible losses [71–73].

Thanks to the combination of PLD and CVD in a very simple two-step process, it was possible to realize a novel anode architecture, i.e. where C layer conformally covers and protects a porous Si nanostructure, and to achieve promising results in terms of lifetime and rate capability.

Perspective work will focus on increasing the value of capacity by optimizing the involved processes so to define an optimal morphology for the novel cell architecture proposed. Thanks to its versatility, PLD can be then effectively used to deposit both Si and C in one single processing step, as well as other Physical Vapour Deposition methods coupled to CVD, thus possibly opening the route to industrially-oriented upscaling.

Acknowledgements

E.B would like to express her gratitude to Mr. Marco Borgini (MEMC Electronic Materials SpA — a SunEdison Company, Novara, Italy) for the donation of silicon wafers used as target for pulsed laser deposition.

The work at the University of Colorado was supported by the Defense Advanced Research Project Agency (DARPA).

The authors declare no competing financial interests.

Appendix A. Supplementary data

Supplementary data related to this article can be found on line.

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