Large Area CMOS SPADs with very low Dark Counting Rate

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1. INTRODUCTION

Nowadays there are various applications such as Optical Time-Domain Reflectometry (OTDR) [1], Quantum Key Distribution (QKD) [2], quantum cryptography [3], fluorescence lifetime imaging (FLIM) [4], laser ranging [5] and many others, which demand low noise, high Photon Detection Efficiency (PDE) and narrow timing response. For these applications, one of the most suitable detectors is the Single-Photon Avalanche Diode (SPAD).

SPADs are solid-state devices that have been studied from decades and lately have garnered much attention because of their attractive features with respect to PMTs, MCPs, EMCCDs and linear-mode APDs; namely, being small and rugged devices with high quantum efficiency and insensitivity to magnetic fields. They could be produced with either custom or standard complementary metal-oxide-semiconductor processes.

Custom technologies allow the designer to modify the process parameters and conditions in order to fabricate optimized devices that set the state-of-the-art in terms of high efficiency, low noise, low afterpulsing probability and sharp timing response even over large area devices [6]. Nonetheless, dedicated processes are expensive and the monolithic integration of detector and electronics requires circuit components specifically designed in the detector technology [7], thus preventing the manufacturing of large SPAD arrays.

Standard technologies do not allow a tailored SPAD design but enable cost-effective production of complete SPAD-based systems, that integrate the sensor together with electronic for photon counting or photon timing [8]. One of the concerns with standard processes is that they could introduce defects, such as metal contaminants or dislocations in the lattice, acting like generation-recombination and afterpulsing centers, thus increasing thus increasing uncorrelated noise (i.e dark counting rate, DCR) and afterpulsing probability and no gettering techniques for cleaning these impurities are available [6]. This implies that SPAD with reasonable performances must have small area and should be operated at low excess bias voltage, which turns into a low efficiency and in a limitation of the maximum achievable fill-factor for SPAD-based arrays.

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Moreover, because the depleted region is accommodated in an n-doped well the avalanche is initiated by holes which have low triggering probability than electrons; hence, the PDE is reduced and timing jitter is worse compared to custom structured where p-doped silicon is used [9].

We present single-photon avalanche diodes fabricated in a 0.35 µm CMOS technology with very large active areas and DCR performances that represent the state-of-the-art for the CMOS SPADs.

The remainder of this paper is structured as follows: in the second section, we will describe the SPAD structures and working conditions; in the third section, we will show and comment the results of experimental characterization and finally we will draw some conclusions.

2. SINGLE-PHOTON AVALANCHE DIODE

The main process that determines the characteristic of a SPAD is the impact ionization mechanism; but, differently, from the avalanche photodiodes (APD), where the ionization mechanism is deployed to produce a linear amplification of the photocurrent, a SPAD produces, upon the absorption of a photon, a high current pulse (with a peak of some milliamps) with sub-nanosecond leading edge ensuring precise time-tagging of the photon arrival. This is a consequence of the fact that a SPAD is basically a p-n junction biased at a voltage V_{POL}, well above its breakdown voltage (Figure 1, point A); at such bias, the electric field in the depletion layer of the p-n junction is high enough that a single injected photo carrier is able to trigger a macroscopic self-sustaining avalanche current (Figure 1, point B). This operation mode is generally referred to as Geiger-mode, in analogy with the working principle of Geiger–Müller counters. After the ignition of the avalanche, the current keeps flowing until a proper front-end circuit lowers the bias voltage below the breakdown voltage (Figure 1, point C); in these conditions, none of the carriers crossing the high field region impact ionizes so the current cannot self-sustain any longer, and the avalanche is then quenched. The front-end circuit after a pre-set time (called hold-off time) swiftly restores the bias condition to allow the detection of another photon (Re-bias phase).

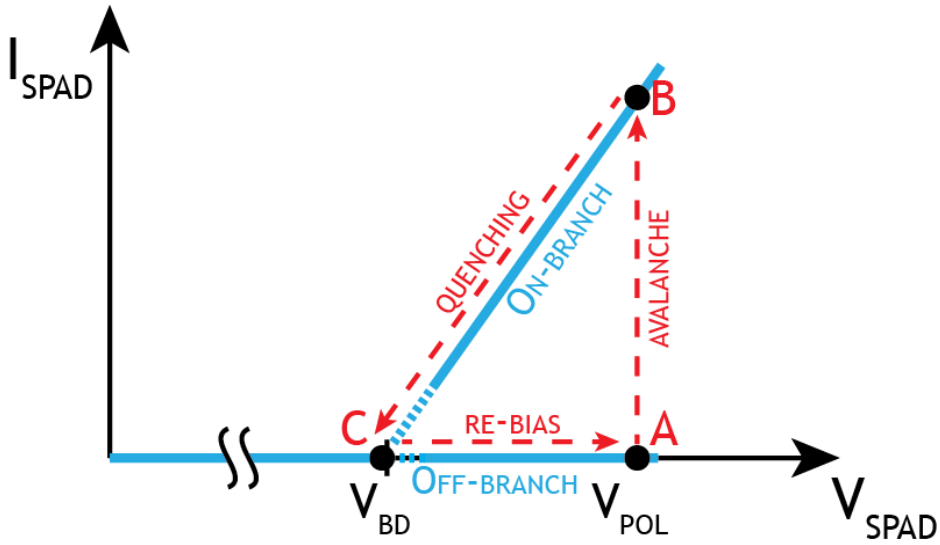

Figure 1. Typical bifurcated I-V characteristic of a SPAD (blue lines) and working operations during normal functioning (red lines). In the beginning, the SPAD is biased at V_{POL}, above the breakdown voltage (V_{BD}) and the I-V curve lies on the off-branch (A). When a photon is absorbed, the generated electron-hole pair triggers an avalanche and the characteristic moves on the on-branch (B). Once the avalanche current is sensed by the front-end circuit, it brings the voltage across the SPAD below V_{BD} (C). The detection of subsequent photons can occur only after the electronics restores the SPAD bias voltage.

2.1 Structure

We designed SPADs of different dimensions (from 50 µm to 500 µm active-area diameter). The devices were fabricated in a 0.35 µm high-voltage 2P-4M CMOS technology on 8-inch wafers with local-oxide silicon based (LOCOS) insulations and monolithically integrated with a front-end circuit optimized to reduce the avalanche charge, in order to minimize the detrimental effects of the afterpulses which, on large area devices, could severely impair the performances.

The structure of the detector is shown in Figure 2: a deep low-doped n-well forms the junction cathode and insulates the photoactive region of the SPAD from the shared substrate (a high quality p-epilayer); a p+ shallow implant, acting as the anode, and an enrichment diffusion (obtained with a low energy phosphorous implantation) define the high-field region in the active area; a p-doped guard-ring smoothes down the peripheral electric field, thus preventing edge breakdown.

Figure 2 also shows that a moderate electric field region is still present in the reverse-biased cathode-substrate junction, as a result of the integration of the front-end circuitry on the same substrate of the SPAD: for a correct functioning of the electronics, the substrate must be connected to ground so a reverse voltage equal to V_{POL} is applied between the substrate and the SPAD cathode and, because of the relative low doping of the cathode, a large portion of the parasitic junction is depleted, thus pinching off the neutral region of the SPAD. As a consequence, the available area for the current flow is reduced and the series resistance of the device is increased, thus exacerbating the space charge effects that lower the junction electric field and degrade the timing resolution. On the other hand, the diffusive effects on the timing response are minimized (i.e. exponential slow tails are shortened, as measured in [10]) thanks to the reduction of the neutral layer and to the fact that the cathode-substrate junction competes with the active junction in collecting the holes generated in the neutral layer [6],[9],[11].

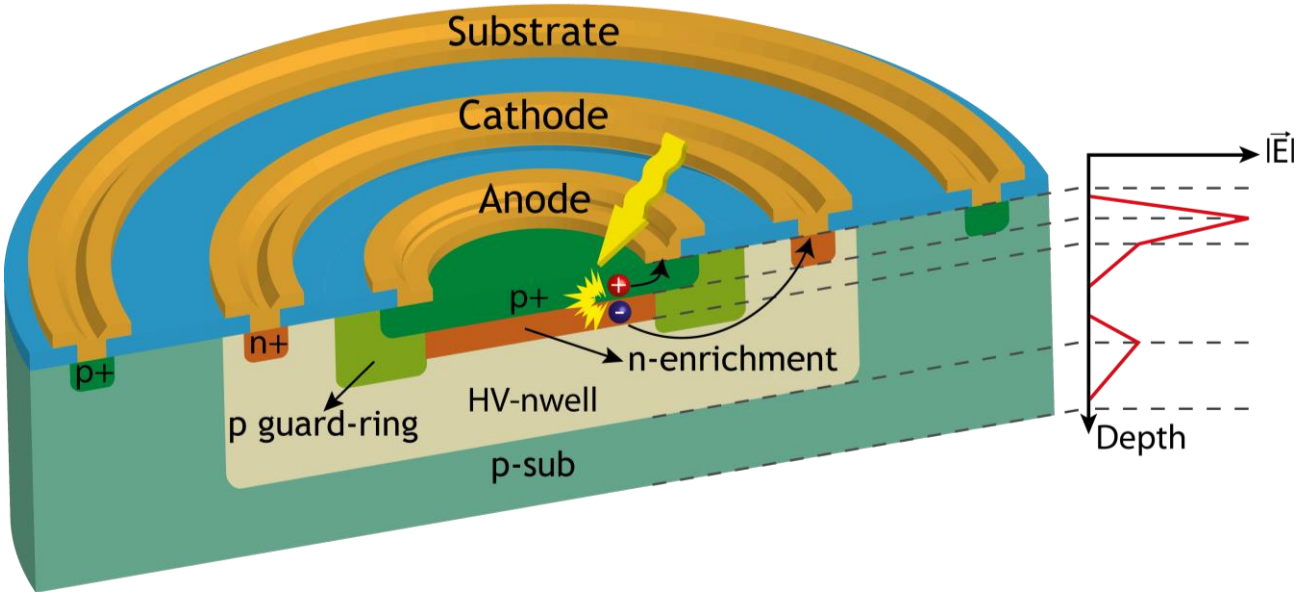

Figure 2. Three-dimensional cross-section of a SPAD fabricated in a 0.35 µm HV-CMOS technology and a simplified representation of the electric field magnitude across the device. The p+ shallow implant and the n-doped enrichment diffusion define the avalanche region; a deep low-doped n-well forms the cathode and separates the photoactive area from the substrate.

2.2 Integrated front-end circuit

Each SPAD is sided by the relative front-end circuit, namely the quenching circuit (QC) [9], which performs several tasks: it sets the above-breakdown quiescent condition, waiting for a photon; it senses the onset of the avalanche current; it tags the photon arrival time with a low-time jitter output pulse; it quenches the avalanches process, as soon as possible to prevent the heating of the detector; finally, it resets the SPAD by restoring the initial bias conditions. Moreover, the integration of the quenching circuit together with the detector is the most effective way to reduce stray capacitance and so also the charge that flows through the device, thus minimizing undesired afterpulsing effects [13],[14].

An optimized QC was designed with the aim of reducing the total amount of charge flowing through the SPAD, assuring a well-defined hold-off time and a fast reset of the device at the initial condition. In order to properly simulate circuit operation and minimize the quenching time, we employed the SPAD model reported in [15]. Figure 3 shows the cell schematics of the circuit. The number of transistors directly connected to the SPAD is three, in order to reduce the loading at the anode, and each device has different tasks: M_S senses the avalanche current and eventually quenches it; M_T flags the photon arrival and triggers the following electronics, while M_R is enabled only during the reset phase. The

ancillary electronics consists of only three logic ports which are deputed to turn on the reset transistor M_R, after the hold-off time that can be adjusted from 20 ns to infinite by means of an external voltage .

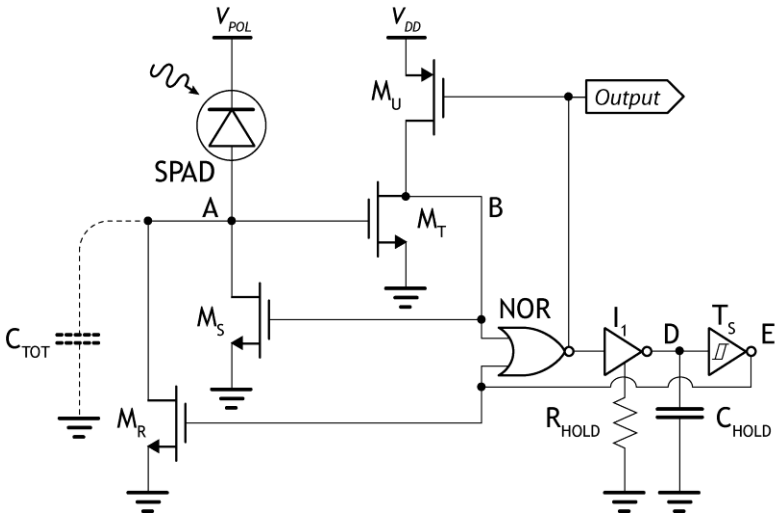

Figure 3. SPAD front-end. The stray capacitance C_A includes also the anode-to-ground and anode-to-cathode SPAD intrinsic capacitances.

3. EXPERIMENTAL CHARACTERIZATION

We performed the dark counting rate (DCR) measurements for four circular SPADs with active-area diameters of 50 µm, 100 µm, 200 µm and 500 µm. The breakdown voltage V_{BD} of the devices is 25.5 V ± 0.1 V. The DCR was measured at room temperature (RT) as a function of the excess bias voltage ($V_{EX} = V_{POL} - V_{BD}$) and of the hold-off time (T_{OFF}).

3.1 DCR vs. Excess Bias Voltage

Figure 4 shows the results of the DCR vs. V_{EX} measurements, performed with 800 ns hold-off time to greatly reduce undesired afterpulsing effects. The novel SPAD structures with 50 µm, 100 µm, 200 µm and 500 µm diameters exhibit respectively DCR of 100 cps, 2 kcps, 20 kcps and 100 kcps, with minor fluctuations at different excess biases, resulting from variations of the avalanche triggering probability [9].

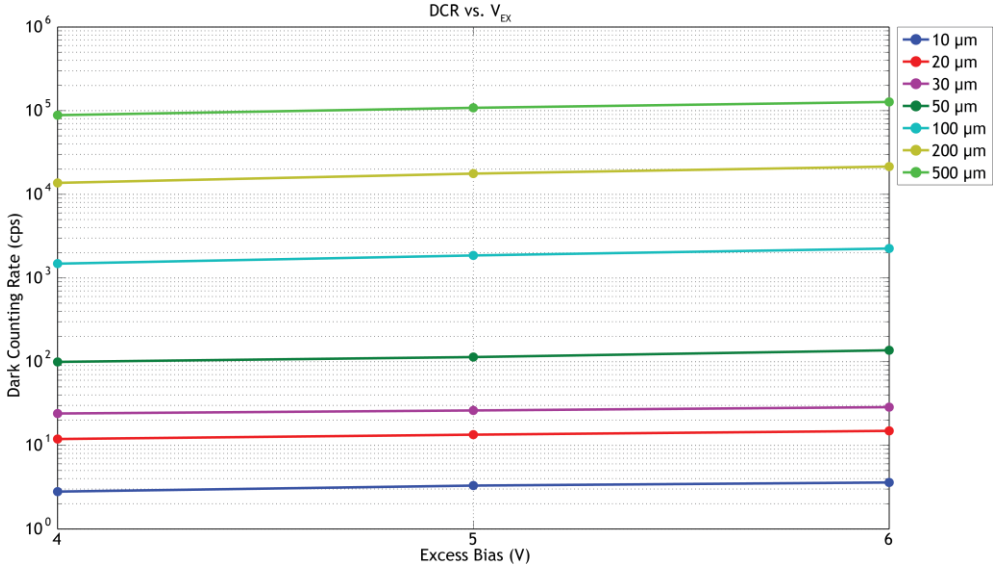

Figure 4. Dark counting rate at different excess bias voltage for the novel SPAD structures.The smallest structures (10 to 30 µm) were presented in [10].

Differently from small SPADs fabricated in the same technology [10], bigger structures show a more than quadratic DCR growth with increasing area (Figure 5.a), as a consequence of the fact that on big devices the defect density is higher; and this could turn into a low yield. To support this assertion, Figure 5.b shows the inverse DCR cumulative distribution function (CDF) for the 30 µm, 50 µm and 100 µm structures: although the number of tested 50 µm devices is scarce (32 SPADs), we can state that their DCR distribution tends to resemble the one measured from the 30 µm structure DCR, with only 5% of hot SPADs; conversely, the 100 µm devices clearly exhibit a dissimilar distribution with almost 30% of noisy devices. Nonetheless, the median DCR value and the percentage of noisy SPADs are even better than those of other devices with smaller area (10-20 µm diameter), fabricated in a 0.35 µm CMOS technology [16]-[18].

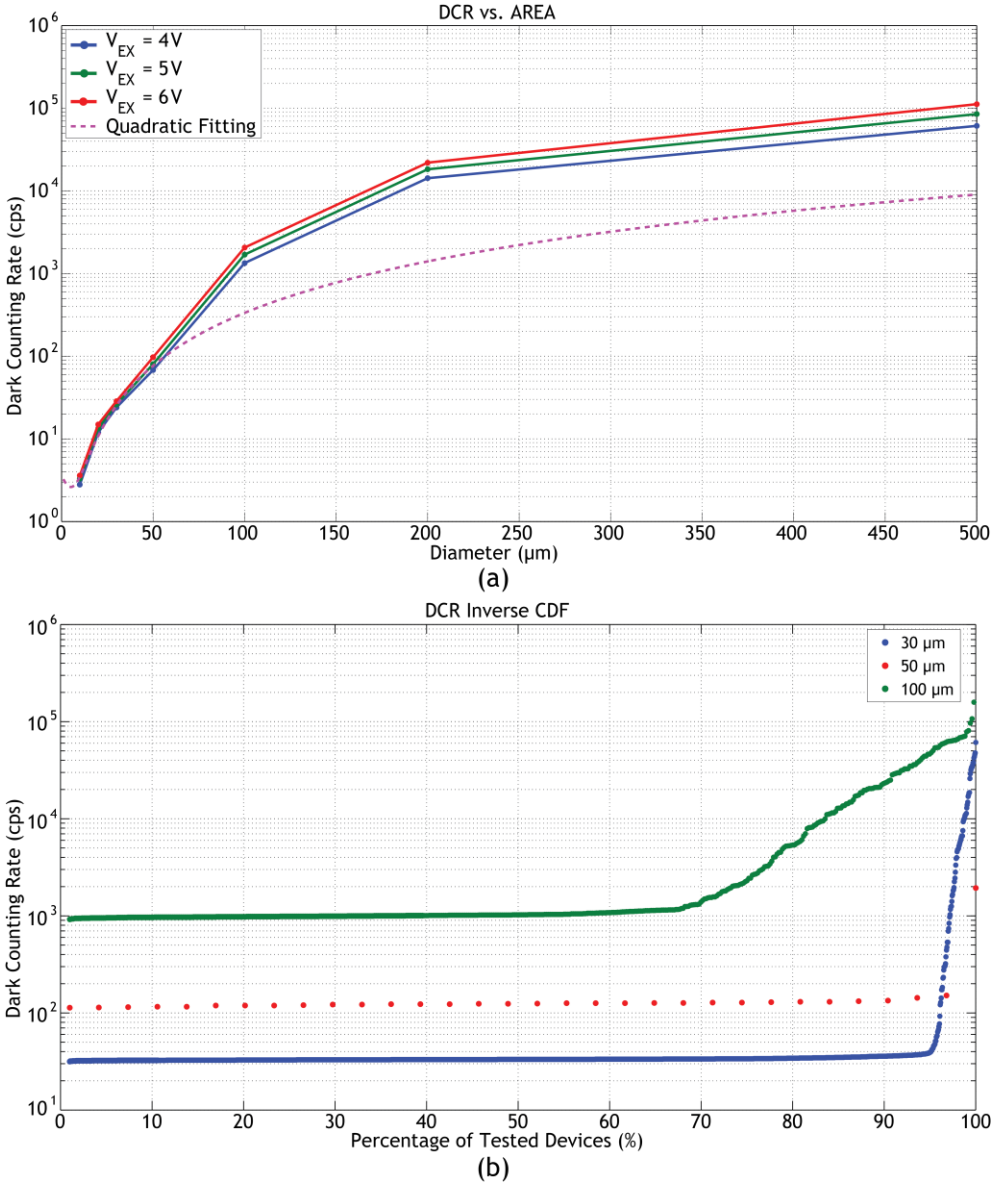

Figure 5. a) Dark counting rate plotted as a function of the diameter. The 10 µm, 20 µm, 30 µm and 50 µm structures have DCRs that increase according to a quadratic relationship; whereas, the 100 µm, 200 µm and 500 µm devices contain a higher number of impurities, such that the DCR increment cannot be fitted by a quadratic curve. b) DCR inverse cumulative distribution function (CDF) showing how the SPAD area negatively affects the yield (i.e. the percentage of noisy devices).

3.2 DCR vs. Hold-off Time

Another issue related with a high defect density is the correlated noise, commonly referred to as afterpulsing [9]. Although an accurate characterization of this noise source can be performed solely with the time-correlated carrier counting (TCCC) technique [19], we preliminarily investigated how afterpulsing directly affects the DCR, by measuring the dark counts at different hold-off times and different excess biases, thus obtaining more accessible graphs from a user standpoint. The data from the four structures are plotted in Figure 6: as the hold-off time decreases, the DCR stays constant until a critical value is reached; below this value, the dark counts exponentially increase because of afterpulsing effects. Considering that this critical value is the minimum hold-off time at which the SPAD can be operated without significant performances degradation, it is indicated in Figure 6 as T_{MIN}. In agreement with the considerations made in the previous subsection, because on very large area devices a higher number of impurities is present, T_{MIN} varies from 40 ns for the 50 µm SPAD, to 80 ns for the 100 µm and 200 µm SPADs, up to 100 ns for the 500 µm SPAD. Compared with other works, the minimum operative hold-off time (T_{MIN}) is better than the values reported for smaller detectors fabricated in 0.35 µm CMOS technology, also thanks to the optimized integrated front-end; for instance, [17] reports a T_{MIN} equal to 500 ns for a 20 µm square SPAD; whereas in [18] a value of 300 ns for a 20 µm circular SPAD is reported; also in a 0.13 µm CMOS technology operative hold-off times of 100 ns, 180 ns and 450 ns are reported respectively for an 8 µm [20], 9 µm [21] and 10 µm [22] SPADs.

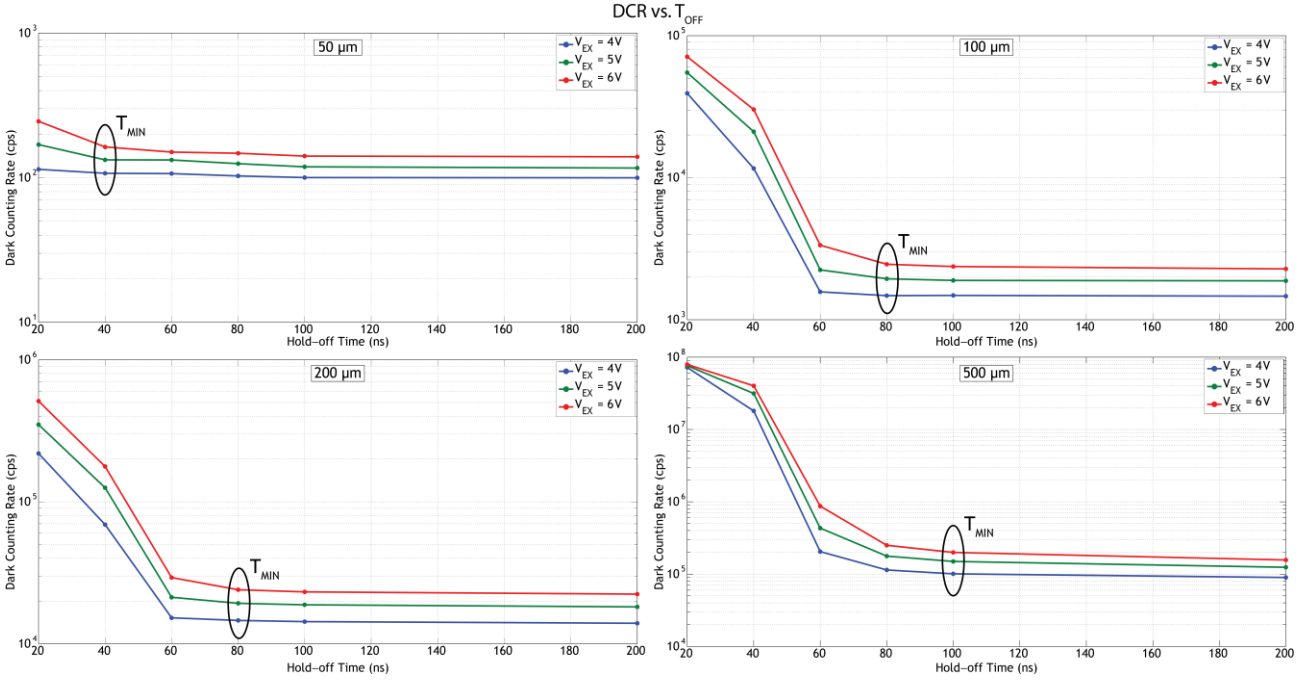

Figure 6. Dark counting rate as a function of the hold-off time, showing the minimun hold-off time (T_{MIN}) at which a SPAD can be operated without degrading the performances. As the diameter increases, T_{MIN} gets longer because of the higher number of defects that contribute in generating afterpulses.

4. CONCLUSIONS

In this paper we presented the noise characterization of four SPAD structures (circular devices with active area of 50 µm, 100 µm, 200 µm and 500 µm diameter) fabricated in a high-voltage 0.35µm CMOS technology. The 50 µm and 100 µm devices exhibit, at room temperature, low dark count rates especially if compared to devices with smaller area fabricated in similar technologies. The 200 µm and 500 µm SPADs show reasonably higher DCRs (20 kcps and 100 kcps) because of higher defect density. Nevertheless, it is possible to take advantage of their large photoactive area by performing gated-mode operations or by cooling them. We also investigated the influence of the afterpulsing on the noise performance, and we showed that it is possible to operate even the largest SPAD with a hold-off time as short as 100 ns, which is still a favorable value even if compared to the nominal operating hold-off times reported in the literature for

smaller area SPAD structures fabricated in 0.13 µm and 0.35 µm CMOS technologies. In the future, an extensive characterization of the presented devices (photon detection efficiency, temperature behavior, TCCC) will be performed.

ACKNOLEDGMENT

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