# Analysis and Design of Low-Jitter Digital Bang-Bang Phase-Locked Loops

Giovanni Marucci, *Student Member, IEEE*, Salvatore Levantino, *Member, IEEE*, Paolo Maffezzoni, *Member, IEEE*, and Carlo Samori, *Senior Member, IEEE*

## I. Introduction

DIGITAL phase-locked loops (DPLL) are recently finding new applications into high-demanding contexts such as frequency synthesis for communications and clock generation for data converters, where their performances may become competitive against those of their analog counterparts [1]–[5]. DPLLs entail the advantage of smaller area occupation thanks to their digital loop filter which scales down with new technology nodes and whose hardware can be easily adapted to different needs by soft programming. The bottleneck of DPLLs is typically represented by design complexity and power consumption of time/digital converters (TDCs), needed as phase detectors. This limitation can be overcome by borrowing the use of single-bit (or bang-bang) phase detection from the field of clock-and-data-recovery applications [6].

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The authors are with Dipartimento di Elettronica e Informazione, Politecnico di Milano, I-20133 Milano, Italy.

The strong nonlinearity of the phase detector complicates significantly the analysis and design of bang-bang PLLs (BB-PLLs). The oscillation period of the output signal is affected by a quantization error introduced by the concurrent presence of the bang-bang coarse quantization and the finite resolution of the digitally-controlled oscillator (DCO). When period quantization is much larger than random-noise fluctuations, the BBPLL variables tend to describe periodic or quasi-periodic orbits in the state space. This behavior results into unwanted spur tones of relevant peaking that deteriorate the output spectrum and increase output jitter [7]–[10]. In principle, spur tones can be reduced or eliminated at all by progressively increasing the DCO resolution and then exploiting some noise source of the PLL as dithering signal. This concept has been quantitatively analyzed in [11], where the $1/f^2$ component of DCO phase noise was considered as dithering source.

However, achieving such a fine DCO period (or frequency) resolution is extremely critical in practice and is paid heavily in terms of larger area occupation, higher power consumption and worse linearity. A more effective approach consists in relaxing DCO granularity and adding a down-scaling factor and a quantizer (typically a $\Delta\Sigma$ modulator) between the loop filter and the DCO. This digital operation allows reducing the jitter induced by the bang-bang coarse quantization, but it introduces a second source of quantization noise. Although conventionally adopted in the design of digital PLLs [12], the impact of this solution on the generation of limit cycles in a bang-bang digital PLL has never been analyzed. The analysis conducted in [10], which accounts for both sources of quantization, allows predicting the frequency of the limit cycle, but it is not suitable to estimate its magnitude.

A second issue is related to the spectral content of DCO phase noise. Accounting for just the $1/f^2$ component of phase noise as in [11] is not realistic since especially in scaled CMOS processes it exhibits a large $1/f^3$ spectral component which is due to the up conversion of flicker noise sources. An analysis of jitter which accounts for the actual shape of DCO phase noise is lacking.

To address these gaps in the state-of-the-art theory of BB-PLLs, we present in this paper a comprehensive jitter analysis that, for the first time, considers (i) the presence of the additional quantization of the DCO and (ii) the actual spectral shape of DCO phase noise. Thus, the following novel contributions are provided over existing literature: (i) the derivation of closed-form expressions for the quantization-induced jitter under multiple quantizations; (ii) the evaluation of random-noise-induced jitter including flicker noise; (iii) the proof that an optimal set-

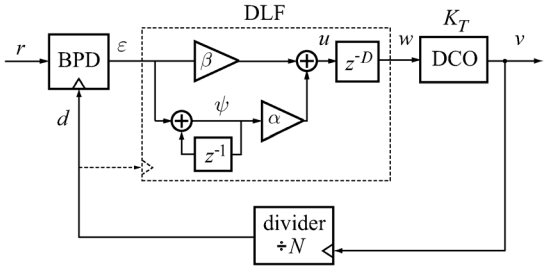


Fig. 1. Block diagram of a second-order digital bang-bang PLL.

ting of the loop parameters exists that eliminates spur tones while minimizing total jitter; (iv) the demonstration of the proposed design methodology in a practical BBPLL, fabricated in a 65-nm CMOS process.

What remains of this paper is organized as follows: In Section II, the analysis of quantization noise in first- and second-order BBPLLs is first recalled, then extended to loops with additional quantizations and relaxed DCO resolutions and validated via numerical simulations. The presence of random noise within the loop is taken into account in Section III, where a closed-form expression of total jitter as a function of noise and loop parameters is provided. Jitter minimization is elucidated in Section IV, while Section V shows the practical application of the proposed theory to the design of a 320-MHz bang-bang PLL. The measured performance of the designed PLL is reported in Section VI. Finally, conclusions are drawn in Section VII.

## II. Quantization-Induced Jitter

In the first subsection, we shortly review the basic results on BBPLLs, whereas we present the novel analysis accounting for DCO quantization in the remainder of this section.

### *A. Second-Order Digital Bang-Bang PLL*

The block diagram of a second-order BBPLL in its simplest form is shown in Fig. 1. The distinct feature of BBPLLs over conventional digital PLLs [12] is the use of the binary phase detector (BPD), which provides an indication of the phase difference between the reference clock and the feedback clock in a binary form or in other words with 1-bit resolution.

In practice, the BPD compares the rising edges of the reference clock (whose time instants can referred to as $t_r$) with those of the divided clock (whose time instants can be referred to as $t_d$) and produces a binary time-error information $\epsilon$. If the divided clock leads the reference, $\epsilon$ is mapped to a $+1$, otherwise it is mapped to a $-1$. Mathematically, $\epsilon$ is given by $\mathrm{sign}(\Delta t)$, where the time error is $\Delta t = t_r - t_d$. The hard nonlinearity introduced by the BPD makes the loop behavior inevitably nonlinear.

The BPD output is fed to a digital loop filter (DLF), which consists of a proportional and of an integral path with gain coefficient $\beta$ and $\alpha$, respectively. Pipeline stages that may be introduced in the actual implementation of the filter are modeled by the $z^{-D}$ block, being $D$ the number of reference clock delays. Loop stability necessitates that the proportional path has a much higher gain than the integral path (i.e., $(\beta/\alpha) \gg 1$) and that, as loop latency is increased, the ratio $(\beta/\alpha)$ must be increased. As it will be derived in the following, a value of $(\beta/\alpha)$ equal to 32 guarantees good stability margin for loop latency $D \leq 1$.

The filter output $w$ controls the frequency of a digitally-controlled oscillator (DCO); this frequency is divided by $N$ and the resulting $d$ signal is fed back to the BPD. The DCO can be modeled as a linear block that provides a clock signal with a period $T_v$ which is given by

$$T_v = T_{v0} + K_T \cdot w, \tag{1}$$

where $T_{v0}$ is free-running period of the DCO and $K_T$ is the sensitivity of the DCO period.

In practice, being the DCO a digital-to-analog converter from its input digital word $w$ to its period $T_v$, $K_T$ is the weight of the least-significant bit (LSB) of the converter. In order to prevent the DCO to add another quantization error into the loop, the parameters of the loop filter ($\alpha$ and $\beta$) must be chosen so that the minimum increment/decrement of the DCO input word $w$ is $\pm 1$. This occurs for $\alpha = 0.5$ and $\beta \geq \beta_0$, where $\beta_0 \approx 16$ guarantees $\beta/\alpha \geq 32$ thus stable loop for latency $D \leq 1$.

At the $k$-th reference cycle, the time occurrence $t_v$ of the DCO rising edges is the accumulation of the period $T_v$ or it is equivalently given by the following finite-difference equation

$$t_v[k+1] - t_v[k] = N \cdot T_v[k] \tag{2}$$

where $N$ is the division factor of the feedback divider.

Assuming no latency of the frequency divider, the time occurrence of the rising edges of the divider output $t_d$ is identical to $t_v$. Hence, the time error at the BPD input is given by

$$\Delta t[k+1] - \Delta t[k] = T_0 - NK_T \cdot w[k] \tag{3}$$

where $T_0 = T_r - NT_{v0}$ is the difference between the reference clock period and the DCO free-running period multiplied by $N$.

In this system, we are interested in deriving the expression of the absolute jitter $J$, which is given by the standard deviation of the time occurrences $t_v$ of the output edges with respect to those of an ideal clock. Neglecting the jitter of the reference clock, this jitter coincides with the standard deviation of the delay $\Delta t$ between the two inputs of the BPD, i.e.,

$$J = \sigma_{\Delta t} \tag{4}$$

In the ideal case of no random noise source in the system, the time error $\Delta t$ varies periodically or in other words the BBPLL exhibits a limit cycle, as it happens in any quantized system.

This phenomenon can be described easily in the case of a first-order system (i.e., $\alpha = 0$), with a zero-latency loop filter (i.e., $D = 0$) [9]. In this case, $w[k]$ has only two possible values $\pm\beta$, and, in order for the PLL to reach lock, $T_0$ must be chosen in the interval $0 < T_0 < N\beta K_T$. If $\Delta t < 0$, the filter output $w$ is equal to $-\beta$ and the increment of the time error $\Delta t$ given by (3) is $(T_0 + N\beta K_T)$. Thus, $\Delta t$ reaches its maximum value $\Delta t_{max} = (T_0 + N\beta K_T)$ at $(k+1)$ when $\Delta t[k] = 0^-$.

Similarly, the minimum (negative) value $\Delta t_{min}$ is equal to $(T_0 - N\beta K_T)$, which is reached at $(k+1)$ when $\Delta t[k] = 0^+$. The resulting peak-to-peak value of $\Delta t$ is therefore given by

$$\Delta t_{pp} = \Delta t_{max} - \Delta t_{min} = 2N\beta K_T. \tag{5}$$

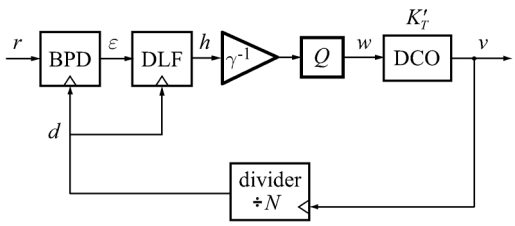


Fig. 2. Second-order bang-bang PLL with down-scaling of the digital filter output and quantization.

If the ratio $x_0 = T_0/(N\beta K_T)$ is assumed to be irrational, $\Delta t$ is uniformly distributed over the $[\Delta t_{min}, \Delta t_{max}]$ interval. Thus, the standard deviation of $\Delta t$ and in turn the PLL jitter component $J_q$ associated to quantization are given by

$$J_q = \sigma_{\Delta t} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{N\beta K_T}{\sqrt{3}}. \tag{6}$$

The latter result can be extended to the second-order BBPLL for any latency $D$. Assuming $(\beta/\alpha) \gg 1$ and taking an irrational $x_0$, it can be shown that the peak-to-peak value of the time error is equal to $\Delta t_{pp} = (1+D)\cdot 2N\beta K_T$ and its standard deviation is [9]

$$J_q = \sigma_{\Delta t} \approx \frac{(1+D)}{\sqrt{3}} \cdot N\beta K_T. \tag{7}$$

Equation (7) reveals that DCO frequency granularity produces quantization noise and that the larger is the LSB of the DCO ($K_T$), the larger is the standard deviation of the resulting quantization noise at the input of the BPD and at the output of the PLL. Additionally, (7) suggests that quantization noise increases as $\beta$, a parameter which cannot be reduced below a certain value $\beta_0$ for loop stability. Thus, the minimum achievable jitter $J_0$ related to quantization noise is obtained by substituting $\beta$ with $\beta_0$ in (7).

### *B. BBPLL With Down-Scaling and Quantizer*

The BBPLL schematic in Fig. 2 relaxes DCO resolution while maintaining same jitter $J_0$ and stability margin (i.e., same $\beta_0$). The LSB of the DCO is scaled up by a factor $\gamma > 1$ with respect to the standard BBPLL in Fig. 1. This new value of the LSB can be denoted as $K'_T = \gamma K_T$. Concurrently, the filter output is scaled down by $\gamma^{-1}$ via a digital shift operation and quantized by means of a quantizer $Q$, so that the minimum increment/decrement of the DCO input word $w$ is still $\pm 1$.

For analogy to the quantization introduced by the BPD, the block $Q$ can be implemented as a *mid-rise quantizer*, whose input/output relationship is

$$Q(x) = \begin{cases} \dots \\ -1.5 & \text{for } -2 \le x < -1 \\ -0.5 & \text{for } -1 \le x < 0 \\ +0.5 & \text{for } 0 \le x < 1 \\ +1.5 & \text{for } 1 \le x < 2 \\ \dots \end{cases} \tag{8}$$

Starting our analysis from the first-order-loop case ($\alpha = 0$) with zero latency ($D = 0$), the quantizer input toggles between two possible values, i.e. $\pm\beta/\gamma$.

If we first consider the case for $\beta/\gamma < 1$, the quantizer output given from (8) will toggle between $+0.5$ and $-0.5$ (or between two adjacent output levels, in a second-order loop). The peak-to-peak $\Delta t$ in this case can be derived, following the same reasoning used previously in the plain loop, i.e.,

$$\Delta t_{pp} = NK'_T. \tag{9}$$

For a uniformly-distributed $\Delta t$, the standard deviation is given by

$$\sigma_{\Delta t,Q} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{NK'_T}{\sqrt{12}}. \tag{10}$$

Similarly to the previous case, the latter result can be extended to the general case of the second-order loop and with any loop latency $D$ by modifying the expression of the peak-to-peak deviation to

$$\Delta t_{pp} = (1+D)\cdot NK'_T, \tag{11}$$

and the resulting output jitter is therefore

$$\sigma_{\Delta t,Q} \approx \frac{(1+D)}{\sqrt{12}} \cdot NK'_T. \tag{12}$$

If we now consider the other case for $\beta/\gamma > 1$, the quantizer output will span over a range wider than $\pm 0.5$. Therefore, for very large values of $\beta/\gamma$, the presence of the quantization block $Q$ can be neglected, thus falling back to the case of the plain system. The standard deviation of $\Delta t$ associated to the quantization of the DCO can be therefore approximated as

$$\sigma_{\Delta t,dco} \approx \frac{1+D}{\sqrt{3}} \cdot \frac{N\beta K'_T}{\gamma}. \tag{13}$$

In general, for any $\beta/\gamma$ value, the jitter will be given summing quadratically the two contributions in (12) and (13), i.e.,

$$J'_q = \sigma_{\Delta t} = \sqrt{\sigma^2_{\Delta t,Q} + \sigma^2_{\Delta t,dco}}. \tag{14}$$

The modified and the plain loops can be compared each other by calculating the ratio of the jitter $J'_q$ of the modified system given by (14), (12), (13) and the minimum jitter $J_0$ of the plain BBPLL given by (7) with $\beta = \beta_0$, i.e.,

$$\frac{J'_q}{J_0} \approx \sqrt{1 + \left(\frac{\gamma}{2\beta_0}\right)^2}. \tag{15}$$

The latter equation shows that the same absolute jitter as in the plain case can be achieved, if the second term in (15) is negligible, i.e. if $\gamma \ll 2\beta_0$. For instance, if $\beta_0 = 16$ and if the DCO LSB is increased by a factor $\gamma = 15$, $J'_q$ worsens by only 10% over $J_0$. Thus, a negligible degradation of jitter allows us to save up to about 4 equivalent bits in the DCO.

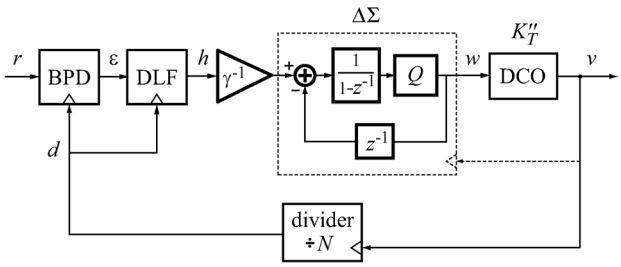


Fig. 3. Second-order digital bang-bang PLL with down-scaling of the digital filter output and first-order $\Delta\Sigma$ modulator.

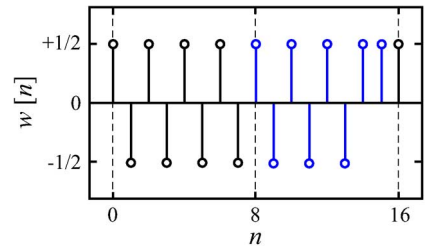


Fig. 4. Output of $\Delta\Sigma$ modulator over two reference clock periods.

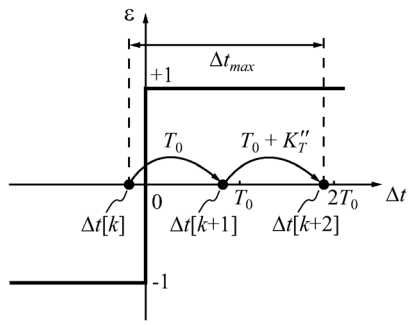


Fig. 5. BPD characteristic and evolution of the time error $\Delta t$ at BPD input over two reference clock periods starting from $\Delta t[k] < 0$.

### C. BBPLL With Down-Scaling and $\Delta\Sigma$ Modulator

A second modified scheme of BBPLL which allows us to further relax DCO intrinsic resolution is shown in Fig. 3. It is obtained by employing an up-sampled first-order $\Delta\Sigma$ modulator in place of the mid-rise quantizer used in the previous case. The up-sampling of the modulator input is performed at the maximum rate available in the system, that is the output clock rate. The quantizer block $Q$ within the $\Delta\Sigma$ modulator is assumed to have the same characteristic as in (8).

Similarly to the previous case, the weight of the LSB of the DCO $K_T''$ is scaled up by $\gamma > 1$, with respect to the DCO LSB of the plain system, i.e. $K_T'' = \gamma K_T$. At the same time, the filter output is scaled down by the same factor $\gamma^{-1}$ and quantized by means of the digital $\Delta\Sigma$, so that the minimum increment/decrement of the DCO input word $w$ is $\pm 1$.

In this system, the finite-difference equation in (3) is modified as follows

$$\Delta t[k+1] - \Delta t[k] = T_0 - K_T'' \cdot \sum_{n=k}^{k+N-1} w[n] \qquad (16)$$

to take into account the accumulation of the up-sampled $w[n]$ performed by the DCO. The main implication of (16) is that the time delay measured by the BPD after one reference-clock cycle $k$ depends on the decimated moving average of the $\Delta\Sigma$ modulator output [13]. This operation is also known as accumulate-and-dump.

If we first consider the case for $\beta/\gamma \geq 1/N$, we fall again back to the case of the plain loop system. In fact, under this condition, the output of the $\Delta\Sigma$ modulator averaged over the $k$-th reference cycle (i.e. $N$ samples of $\Delta\Sigma$ output)

$$\langle w[n] \rangle_k = \frac{1}{N} \sum_{n=k}^{k+N-1} w[n], \qquad (17)$$

is equal to its input, that is $\beta/\gamma$. Thus, following the same reasoning of the case of the plain loop, we obtain the following expression of the peak-to-peak $\Delta t$ component associated to DCO quantization

$$\Delta t_{pp} = \frac{2N\beta K_T''}{\gamma}, \qquad (18)$$

and its standard deviation

$$\sigma_{\Delta t,dco} \approx \frac{(1+D)}{\sqrt{3}} \cdot \frac{N\beta K_T''}{\gamma}. \qquad (19)$$

If we now consider the case for $\beta/\gamma < 1/N$, the output of the $\Delta\Sigma$ modulator averaged over a single reference cycle $\langle w[n] \rangle_k$ cannot equal its input. It equals the input value $\beta/\gamma$, only if it is averaged over a certain number of reference cycles or, in other words, if the average is extended to a multiple number of $N$ samples.

Let us consider, for instance, the case $\beta = 16$, $\gamma = 256$ and $N = 8$. The sequence $w[n]$ which is schematically shown in Fig. 4 has zero average over the first reference cycle. By contrast, the average is equal to 1/8 over the second cycle. In practice, the $\Delta\Sigma$ output is equal to its input $\beta/\gamma = 1/16$, only if the average is extended over two consecutive reference cycles.

On the basis of this consideration, we can apply to this example the same argument used above in the plain loop for the determination of the maximum value for $\Delta t$. With the help of Fig. 5, if we start from a negative time error $\Delta t[k] < 0$, the BPD output $\epsilon$ is $-1$, therefore the $\Delta\Sigma$ input is equal to $-\beta/\gamma$ and the first increment of $\Delta t$ given by (16) is $T_0$ being nil the sum in (16). The increment of $\Delta t$ becomes instead $(T_0 + K_T'')$ in the subsequent cycle at $(k+1)$, since the sum in (16) is equal to 1. Thus, the time error reaches its maximum value $\Delta t_{max} = (2T_0 + K_T'')$ at $(k+2)$ starting from $\Delta t[k] = 0^-$.

To extend the latter result to any $\beta/\gamma$ value lower than $1/N$, we should note that the averaged output of the first-order $\Delta\Sigma$ modulator over the $k$-th cycle $\langle w[n] \rangle_k$ is always equal to 0 for $[\gamma/(\beta N) - 1]$ consecutive cycles (where $\gamma/(\beta N)$ is an integer number), and it is equal to $1/N$ during the subsequent cycle. In this way, the average over $\gamma/(\beta N)$ consecutive cycles will be equal to the $\Delta\Sigma$ input $\beta/\gamma$, as expected.

Hence, on the basis of (16), we can derive maximum and minimum values of the time error, i.e.,

$$\Delta t_{max} = T_0 \cdot \left( \frac{\gamma}{N\beta} \right) + K_T'', \qquad (20)$$

$$\Delta t_{min} = T_0 \cdot \left(\frac{\gamma}{N\beta}\right) - K_T'', \tag{21}$$

and the resulting peak-to-peak value of $\Delta t$ is therefore given by

$$\Delta t_{pp} = \Delta t_{max} - \Delta t_{min} = 2K_T''. \tag{22}$$

For a uniform distribution of $\Delta t$, the standard deviation of $\Delta t$ associated to $\Delta\Sigma$ modulator is still given by

$$\sigma_{\Delta t,\delta\sigma} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{K_T''}{\sqrt{3}}. \tag{23}$$

Then, summing quadratically the contribution arising from DCO quantization in (19) and the one arising from $\Delta\Sigma$ quantization in (23), we get the total quantization-induced jitter

$$J_q'' = \sqrt{\sigma^2_{\Delta t,dco} + \sigma^2_{\Delta t,\delta\sigma}}. \tag{24}$$

To get a quantitative comparison between this BBPLL with first-order $\Delta\Sigma$ and the plain BBPLL, we compute the ratio between the jitter expression in (24) and the minimum jitter of the plain loop in (7) for $\beta = \beta_0$, i.e.

$$\frac{J_q''}{J_0} \approx \sqrt{1 + \left[\frac{1}{N(1+D)} \cdot \frac{\gamma}{\beta_0}\right]^2}. \tag{25}$$

Thus, same absolute jitter can be achieved in the two systems, if the second term in (25) is negligible, i.e. if $\gamma \ll N\beta_0(1+D)$. For instance, for $N = 8$, $\beta_0 = 16$, $D = 1$, if the DCO LSB is increased by a factor of $\gamma = 117$, jitter $J_q''$ worsens by only 10% compared to $J_0$. Thus, in this case, accepting a negligible degradation of jitter, we can save up to about 7 equivalent bits of the DCO. The improvement increases to about 8 equivalent bits if the loop latency $D$ is zero.

### *D. Simulation Results*

To assess the theoretical results so far achieved, the equations describing the three schemes of BBPLL have been numerically solved for different values of loop parameters.

Fig. 6 shows the normalized jitter $J_q''/K_T''$ of the BBPLL in Fig. 3 as a function of $\beta/\gamma$ values for loop latencies: $D = 0$ and $D = 1$, when $N = 8$. The theoretical results given by (24), (19), (23), represented as solid lines, agree very well with simulation results (shown as circular and square dots).

Fig. 7 shows a plot of the normalized jitter $J_q'/J_0$ given by (15) for the quantizer-based BBPLL and $J_q''/J_0$ given by (25) for the $\Delta\Sigma$-based BBPLL (solid lines), with $N = 8$, $\beta_0 = 16$, $D = 1$. The dots in the same plot obtained from numerical simulations of the two systems for different values of $\gamma$ closely match theoretical estimations.

For very large values of $\gamma$, the jitter of the modified BBPLLs compared to the plain loop worsens, since DCO resolution is proportionally relaxed. However, for lower values of $\gamma$, both modified systems can reach the same jitter of the plain system with relaxed DCO-resolution requirement. Employing the first-order $\Delta\Sigma$ modulator in place of the mid-rise quantizer allows a larger reduction of DCO resolution, since its jitter is practically

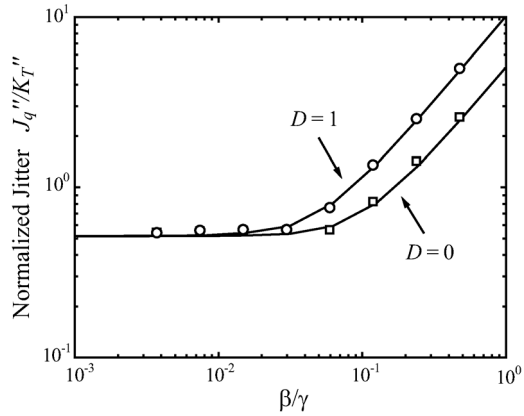


Fig. 6. Quantization-induced jitter (normalized to DCO LSB $K_T''$) of the improved BBPLL with $\Delta\Sigma$ modulator as a function of $\beta/\gamma$: from simulations (markers) and Eq. (24) (solid lines).

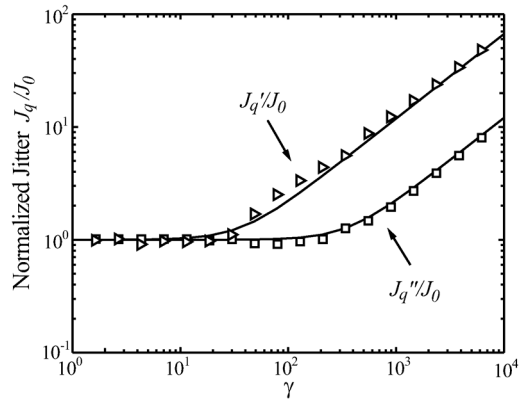


Fig. 7. Jitter of the two improved systems $J_q'$ and $J_q''$ (normalized to jitter of plain system $J_0$) as a function of $\gamma$: from simulations (triangles for the system with quantizer and squares for the system with $\Delta\Sigma$ modulator) and from Eqs. (15) and (25) (solid lines).

identical to that of the plain system $J_0$ for $\gamma$ values up to about a decade higher.

Further reduction of DCO resolution while maintaining same output jitter is possible by cascading a reconstruction filter to the $\Delta\Sigma$ modulator. For instance, considering a low-pass filter with a single pole at about one 30-th of the PLL output frequency and $N = 8$, same jitter can be obtained even choosing $\gamma = 512$.

## III. Random-Noise-Induced Jitter

We have so far analyzed the plain BBPLL and the improved versions neglecting the presence of any random noise source. We intend to consider now the presence of noise arising from physical thermal and flicker sources.

With regard to the system in Fig. 3, in the presence of a random component of the time error $\Delta t$ larger than the quantization-induced one, the loop works in the so-called *random-noise regime* [5], [11] and the analysis can rely on the linearized equivalent model shown in Fig. 8 [14]. For input signals $\Delta t$ around its threshold, the BPD can be modeled as a block of gain $K_{bpd}$ plus an additive quantization error $t_{bpd}$ [15]. Note, however, that the BPD gain $K_{bpd}(\Delta t)$ dependents itself on the distribution of its input variable and thus the system in Fig. 8 is actually *nonlinear*

in that it does not satisfy superposition principle. Under the hypothesis of Gaussian distribution of $\Delta t$, the gain $K_{bpd}$ results to be [16]

$$K_{bpd} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}}. \tag{26}$$

The other blocks of the loop are ideally linear and thus they can be described in the frequency domain, as reviewed in Appendix A. Combining those results and assuming that the loop is properly designed to have safe stability margin, the open-loop gain can be well approximated by

$$G_{loop}(f) \approx \frac{f_u}{jf} \tag{27}$$

where

$$f_u \approx \frac{K_{bpd}}{2\pi T_{dco}} \cdot \beta K_T \tag{28}$$

is the unity-gain frequency, whereas $T_{dco} = T_r/N$ and $K_T = K_T''/\gamma$ are the oscillation period and the period sensitivity of the DCO, respectively.

In our analysis, we account for the DCO phase noise originating from white and flicker physical noise sources. In general, the power spectral density (PSD) of the output-referred DCO noise can be therefore written as [17], [18]

$$S_{t_v}(f) = \frac{1}{(2\pi f)^2} \cdot \left( K_W + \frac{K_F}{f} \right), \tag{29}$$

where $K_W$ and $K_F$ are proper noise coefficients.[1]

The injection of this noise source into the loop induces noise at BPD input. Relying on the linear loop model in Fig. 8, the spectrum of the time error $\Delta t$ is given by

$$S_{\Delta t}(f) = \frac{S_{t_v}(f)}{|1 + G_{loop}(f)|^2}, \tag{30}$$

and its variance reads

$$\sigma_{\Delta t}^2 = 2 \cdot \int_0^\infty S_{\Delta t}(f) df. \tag{31}$$

We note here that the quantization noise term $t_{bpd}$ has not been accounted for in the calculation of $\sigma_{\Delta t}$ in the random-noise regime, since its contribution to $\Delta t$ is low-pass filtered by the loop, and the resulting contribution to $\sigma_{\Delta t}$ is negligible.

Hence, in view of (27), the integral in (31) transforms to:

$$\sigma_{\Delta t}^2 \approx 2 \int_{f_z}^\infty \frac{S_{t_v}(f)}{1 + \left(\frac{f_u}{f}\right)^2} \mathrm{d}f \tag{32}$$

where $f_z = (\alpha/\beta)(f_r/2\pi)$ with $f_r = 1/T_r$, is the zero of DLF transfer function described in Appendix A. Substituting (29) in (32) and following the derivations reported in Appendix B, we are able to achieve a closed-form expression for the variance of $\Delta t$, i.e.

$$\sigma_{\Delta t}^2 \approx \frac{K_W}{4\pi f_u} + \frac{K_F \ln(\delta)}{2\pi^2 f_u^2}, \tag{33}$$

where the parameter $\delta = f_u/f_z$ (with $\delta \gg 1$) is set by the loop-stability margin.

The latter result leads us to the conclusion that the variance of the random component of jitter at BPD input (or in turn at PLL output if we neglect the presence of reference noise) increases as the unity-gain frequency of the loop, which is roughly equal to loop bandwidth, is reduced. Besides, as loop bandwidth is narrowed, the contribution of the DCO $1/f^3$ noise component on BPD input jitter increases faster than the contribution of the $1/f^2$ component.

Finally, plugging the expression of $f_u$ in (28) and the expression of $K_{bpd}$ in (26) into (33), we get the following equation

$$\sigma_{\Delta t}^2 \approx \sqrt{\frac{\pi}{8}} \cdot \frac{K_W T_{dco}}{\beta K_T} \cdot \sigma_{\Delta t} + \frac{\pi K_F T_{dco}^2 \ln(\delta)}{\beta^2 K_T^2} \cdot \sigma_{\Delta t}^2, \tag{34}$$

which can be solved for the $\sigma_{\Delta t}$ variable.

Being the standard deviation of a random variable $\sigma_{\Delta t} > 0$, the resulting closed-form expression of the BBPLL random-noise-induced jitter in the presence of $1/f^3$ and $1/f^2$ noise of the DCO is therefore given by

$$J_{rn} = \sigma_{\Delta t} \approx \sqrt{\frac{\pi}{8}} \cdot \frac{K_W T_{dco}}{\beta^2 K_T^2 - \pi K_F T_{dco}^2 \ln(\delta)} \cdot \beta K_T, \tag{35}$$

with $\beta^2 K_T^2 > \pi K_F T_{dco}^2 \ln(\delta)$.

We end this section by showing how the analysis of noise-induced jitter (35) and that of quantization-induced jitter (24) provided in previous section can be joined together to achieve a comprehensive description. To this aim, the nonlinear difference equations describing the digital BBPLL in Fig. 3 are simulated numerically. In simulations we assume the loop parameters $\alpha = 0.5$, $\beta = 16$, $D = 1$, $T_{dco} = 3.125$ ns and $N = 8$ while the DCO noise model has constants $K_W = 2 \cdot 10^{-15}$ s and $K_F = 8 \cdot 10^{-11}$.

The jitter values obtained from simulations for different values of $\beta K_T$ are shown as circles in Fig. 9. In this plot, the quantization-induced-jitter expressions in (24) and the noise-induced-jitter (35) (dash-dotted and dashed lines, respectively) are also reported along with their sum (solid line). The following observations are in order. Closed-form expressions (24) and (35) match with good accuracy simulated jitter in deep limit-cycle regime and deep random-noise regime, respectively. Most importantly, the sum of the two theoretical contributions matches closely the simulated total jitter over all regimes and leads us to the following expression for the total absolute jitter[2]:

$$J_{tot} = \sigma_{\Delta t} \approx J_{rn} + J_q''. \tag{36}$$

[1]The PSD of DCO *time* noise associated to $t_v$ is related to the typical oscillator *phase* noise as follows: $\mathcal{L}(f) = 2\pi^2 f_{dco}^2 \cdot S_{t_v}(f)$, where $f_{dco} = 1/T_{dco}$.

[2]Jitter variance is not obtained by summation of the variances of the two processes [11].

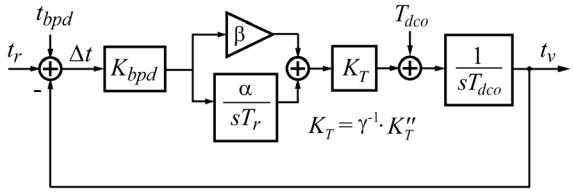


Fig. 8. Linearized model of the digital BBPLL.

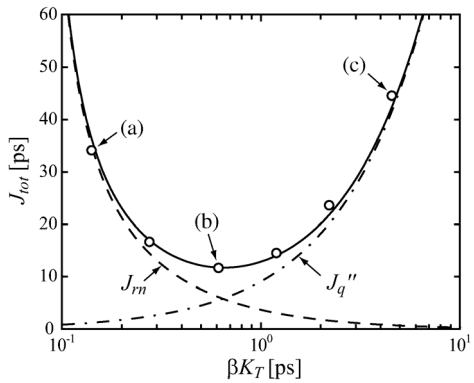


Fig. 9. Quantization-induced component $J_q''$ from (24) (dash-dotted line), noise-induced component $J_{rn}$ from (35) (dashed line) and sum of the two latter terms (solid line). Simulated output jitter $J_{tot}$ as a function of $\beta K_T$ (circles). Settings (a) and (c) correspond to deep random-noise and limit-cycle regimes, respectively, while setting (b) corresponds to an intermediate regime.

This final equation in combination with (24) and (35) provides an estimation of the total output jitter as a function of the loop parameter $\beta K_T$ and DCO phase noise.

## IV. Optimization of Total Jitter

While quantization-induced jitter $J_q''$ grows as the loop parameter $\beta K_T$, the noise-induced jitter $J_{rn}$ decreases as $\beta K_T$. As a result, the total jitter given by (36) exhibits a minimum. Thus, an optimum $\beta K_T$ exists and it can be calculated from the previous closed-form equations.

The optimum $\beta K_T$ is found when the two terms on the right hand side of (36) are equal, or in other words when the jitter induced by quantization equals the jitter induced by random noise, i.e.,

$$(\beta K_T)_0 \approx \sqrt{\frac{K_W T_{dco}}{N(1+D)} + \pi K_F T_{dco}^2 \ln(\delta)}, \qquad (37)$$

where $\gamma$ is chosen to be low enough for the term $\sigma^2_{\Delta t, \delta\sigma}$ in (24) to be negligible.

The minimum total jitter is found from (36) substituting $\beta K_T$ with the expression of $(\beta K_T)_0$ and it is

$$J_{tot,0} = \frac{2N(1+D)}{\sqrt{3}} \cdot \sqrt{\frac{K_W T_{dco}}{N(1+D)} + \pi K_F T_{dco}^2 \ln(\delta)}. \quad (38)$$

For the optimal design setting (37), noise-induced jitter is expected to destroy the periodicity which underlies limit cycles so that the output power spectrum will be cleaned by unwanted spur tones. We verify this point by simulations. Fig. 10 reports the simulated output spectra and trajectories in the $\Delta t, \psi$ state plane for the three parameter settings (a), (b) and (c) which correspond to random-noise regime, optimal design, and limit-cycle regime, respectively (already highlighted in Fig. 9). For setting (c), the trajectory tends to describe closed orbits in the state plane (i.e. limit cycles) which correspond to unwanted spur tones in the output spectrum. By contrast, both settings (a) and (b) are able to eliminate spur tones but only parameter setting (b) allows us to do that while achieving minimum jitter.

We end this section by evaluating the relative weight between $1/f^2$ and $1/f^3$ DCO spectral component on the output jitter. This can be outlined by recasting (38) as a function of the corner frequency of DCO spectrum $f_c \triangleq K_F/K_W$, i.e.,

$$J_{tot,0} = \frac{2N(1+D)\sqrt{K_W}}{\sqrt{3}} \cdot \sqrt{\frac{T_{dco}}{N(1+D)} + \pi f_c T_{dco}^2 \ln(\delta)}. \qquad (39)$$

Fig. 11 shows the BBPLL minimum output jitter $J_{tot,0}$ as a function of the DCO corner frequency $f_c$ for different values of the noise parameter $K_W$. The right vertical axis also reports the corresponding values of the optimum gain $(\beta K_T)_0$. The solid lines given from (39) closely match the circular markers obtained from numerical simulations, assuming $\alpha = 0.5$, $\beta = 16$, $D = 1$, $T_{dco} = 3.125$ ns, $N = 8$. This result confirms the validity of the proposed analysis. In the same figure, with broken lines we also report the minimum jitter values predicted with the analysis in [11] which did not include DCO flicker noise. We see how jitter values predicted with [11] become unrealistic as corner frequency increases.

The optimum value of $\beta K_T$ parameter given by (37) corresponds also to an optimum value of the unity-gain frequency, and in turn of loop bandwidth, which minimizes total jitter. This value obtained from (28) after imposing (37) and (38) is

$$f_{u,0} \approx \sqrt{\frac{3}{8\pi^3}} \cdot \frac{1}{1+D} \cdot f_r, \qquad (40)$$

which results to be equal to about $f_r/9$ for $D = 0$ and $f_r/18$ for $D = 1$ (being $f_r = 1/T_r$).

The expression of $f_{u,0}$ permits us to find the parameter $\delta$ to be used into (37)–(39), i.e.,

$$\delta = \frac{f_{u,0}}{f_z} = \sqrt{\frac{3}{2\pi}} \cdot \frac{1}{1+D} \cdot \frac{\beta}{\alpha}. \qquad (41)$$

Once the optimum $\beta K_T$ product has been determined, we need to know how to set the two parameters individually. If we choose the lowest acceptable value of $\beta$, we relax the requirement on the DCO LSB $K_T$. However, a minimum value of $\beta$ is dictated by loop stability.

Referring to the model in Fig. 8 [11] and imposing the phase margin $\varphi_{m0}$, we find

$$\frac{\beta}{\alpha} = \frac{\tan(2\pi f_u T_r D + \varphi_{m0})}{2\pi f_u T_r}. \qquad (42)$$

Substituting the expression of the optimum unity-gain frequency (40) into (42), we derive the minimum $\beta$ which guarantees the given phase margin, i.e.

$$\beta_0 = \sqrt{\frac{\pi}{6}} \cdot (1+D) \cdot \tan\left(\sqrt{\frac{3}{2\pi}} \cdot \frac{D}{1+D} + \varphi_{m0}\right). \qquad (43)$$

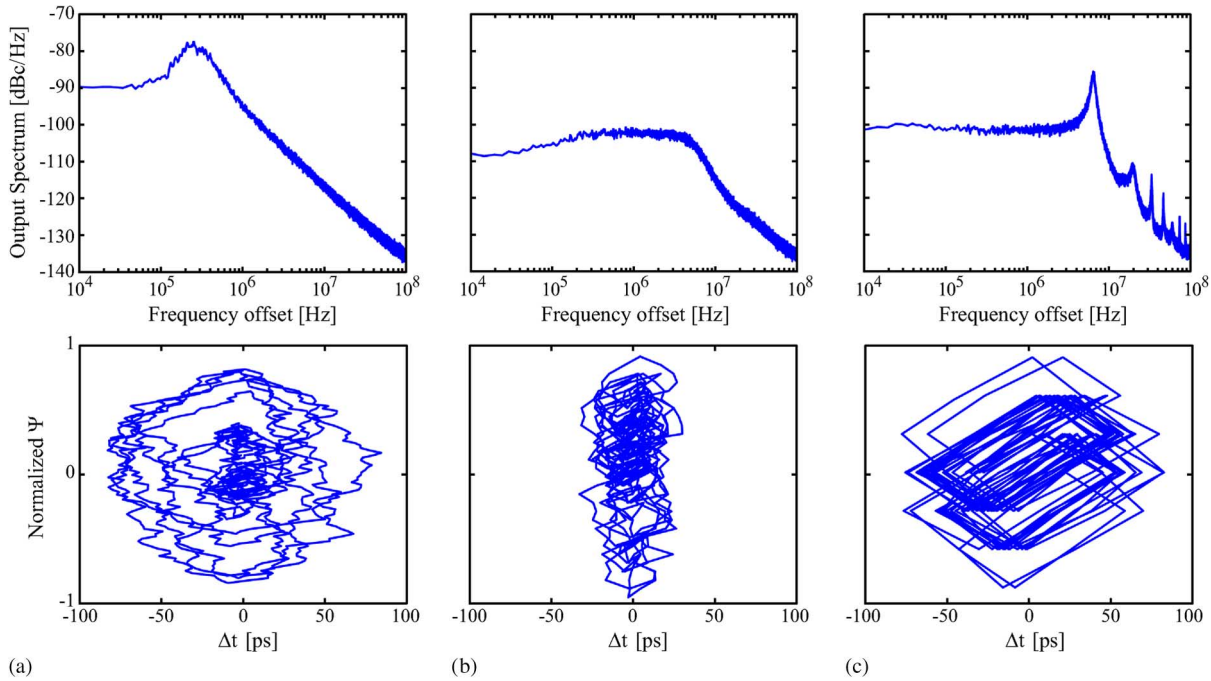


Fig. 10. Simulated spectra and orbits for $\beta = 4$ (random noise), $\beta = 16$ (optimum resolution) and $\beta = 128$ (limit cycle).

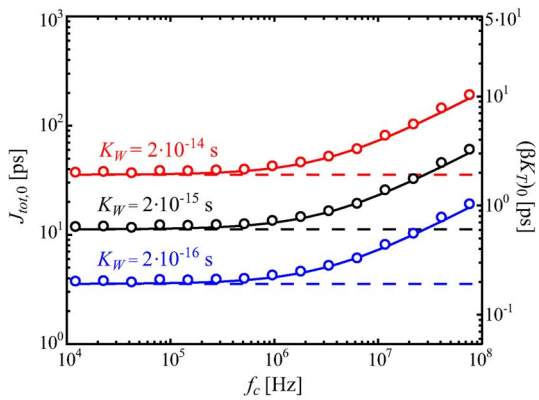


Fig. 11. Minimum output jitter $J_{tot,0}$ and corresponding gain $(\beta K_T)_0$ as a function of the noise corner $f_c$ for different values of $K_W$ noise parameter: simulated dots (circles) and theoretical results from (39) and (37).

For $D = 1$, $\beta_0 = 16$ guarantees 66-deg phase margin and the $\delta$ from (41) is equal to about 10.

## V. PLL Design

In this section, we show how to design a PLL following the results of the proposed analysis. The PLL is intended to synthesize a 320-MHz clock from a 40-MHz reference crystal oscillator, with a targeted absolute jitter $J$ of about 11 ps. On the basis of these values, the division factor of the divider is $N = 8$ and the DCO period is $T_{dco} = 3.125$ ns. We adopt the PLL block schematic with the $\Delta\Sigma$ modulator, shown in Fig. 3. The implementation of the DLF block together with the gain block $\gamma^{-1}$ and the first-order $\Delta\Sigma$ in standard-cell digital logic introduces one-cycle latency into the loop. Thus, the parameter $D$ is equal to 1.

The setting of the loop parameters will be based on the following procedure:

- *Stability*: imposing phase margin $\varphi_{m,0}$ of 60 deg in (43) and taking the next power of 2 of the result lead to $\beta = \beta_0 = 16$.
- *Jitter*: when the minimum jitter value of $J_{tot,0} = 11$ ps is imposed in (39), an equation containing the two unknowns $K_W$ and $f_c$ is obtained. If we set $f_c$ so that the second term in (39) is negligible compared to the first term (for instance, only 10%), i.e.,

$$f_c = \frac{f_{dco}}{72 \cdot N(1+D)} = 280 \text{ kHz}, \tag{44}$$

we can solve the equation for $K_W$, i.e.,

$$K_W = \frac{3}{4} \cdot \frac{J_{tot,0}^2}{N(1+D)} \cdot f_{dco} = 1.7 \text{ fs}. \tag{45}$$

or equivalently $\mathcal{L} = -100$ dBc/Hz at 1 MHz.
- *DCO period sensitivity*: Substituting the value of $K_W$ and $\beta$ in (37) and neglecting the second term, we get the parameter $K_T \approx 38$ fs.
- *DCO quantization*: imposing that the $\Delta\Sigma$ quantization [i.e., second term in (25)] is only 10% of the quantization of the bang-bang PD [i.e., first term in (25)], we get $\gamma = 128$. This can be increased to $\gamma = 512$ inserting a pole at $f_{dco}/30 \approx 10$ MHz between $\Delta\Sigma$ and DCO, as discussed in Section II-D. In practice, the period sensitivity of the DCO can be set to $K_T'' = \gamma \cdot K_T = 19$ ps, or equivalently its frequency sensitivity to $\Delta f_{dco} = K_T'' \cdot T_{dco}^{-2} = 1.86$ MHz/bit.

Adopting this parameter setting, the BBPLL jitter estimated by (36) is plotted as a function of $\beta K_T$ in Fig. 13 (solid line). The absolute RMS jitter is minimum at $\beta = 16$ and it is $J_{tot,0} \approx 11.3$ ps, as expected.

Based on the specifications so far derived, the DCO is designed as a ring-type voltage-controlled oscillator (VCO) driven by a passive DAC. The delay stages of the ring oscillator have

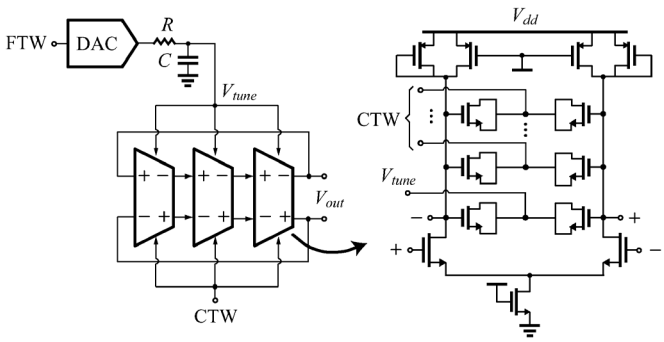


Fig. 12. Schematic of the ring-type VCO.


Fig. 14. Die photograph.

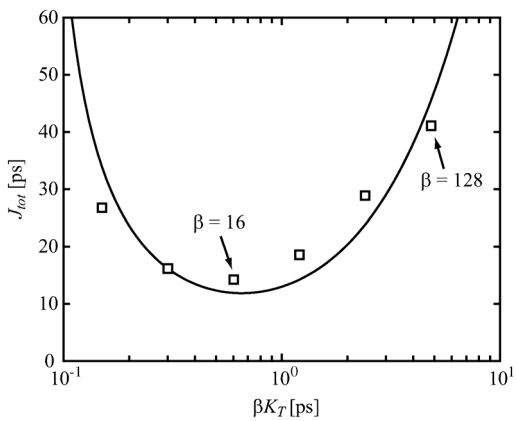


Fig. 13. BBPLL output jitter as function of $\beta K_T$ from eq. (36) (solid line) and from measurements (squares).

a differential topology (also shown in Fig. 12 which provides better immunity to supply disturbances and their delay is regulated by means of MOS varactors. Coarse tuning is obtained by driving a bank of varactors by means of a digital word CTW. Instead, fine tuning is achieved by means of a single couple of varactors controlled by the DAC through a low-pass RC filter.

## VI. Experimental Results

In order to verify experimentally the closed-form expressions and the jitter minimization method proposed in this paper, the BBPLL designed in the previous section is fabricated in a 65-nm CMOS process. The die photo of the chip is shown in Fig. 14.

The phase noise spectra of the PLL is measured at different settings of $\beta$ and the absolute jitter are calculated as the integral of the measured spectra from 1 kHz to 10 MHz. The jitter values are plotted as square dots in the same graph in Fig. 13. Measurements follow closely the theoretical curve and confirm

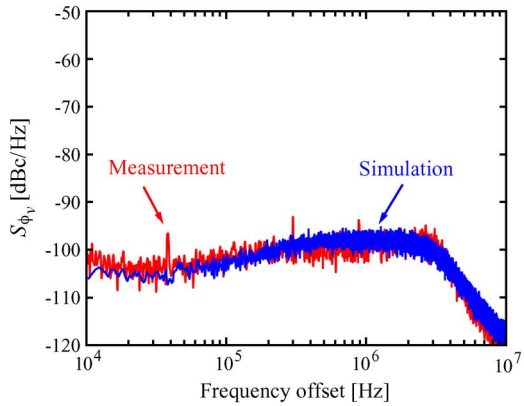


Fig. 15. Simulated and measured phase-noise spectra for optimum design ($\beta = 16$).

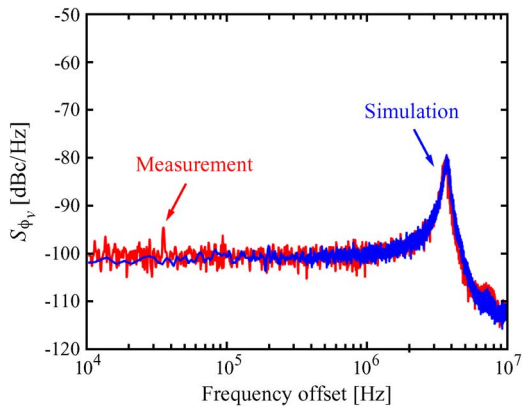


Fig. 16. Simulated and measured phase-noise spectra when the limit cycle dominates over random noise ($\beta = 128$).

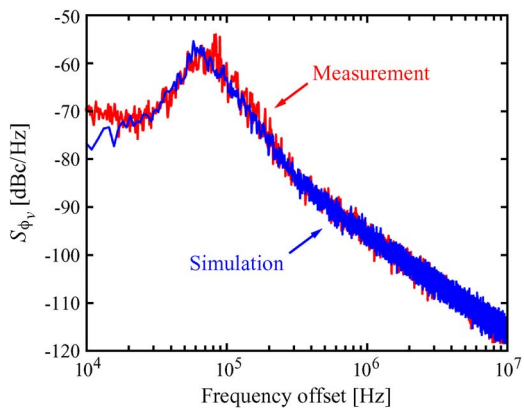


Fig. 17. Simulated and measured phase-noise spectra when random noise dominates over the limit cycle ($\beta = 4, \gamma = 2048$).

the existence of a minimum jitter. The measured minimum jitter is 13.5 ps, which is very close to the estimated value.

The measured spectra relative to $\beta = 128$, $\beta = 16$, and $\beta = 4$ are shown in 15, Figs. 16, and 17, respectively. The close matching of measured spectra to those obtained from numerical simulations and shown in the same plots demonstrates the accuracy of the BBPLL model adopted in simulations and confirms the validity of the theory provided in this paper.

## VII. Conclusion

In this paper, we have provided an analytical expression for the output jitter of a digital BBPLL as a function of the loop parameters and of the thermal and flicker noise sources. The analysis has taken into account typical variants of the plain BBPLL loop, in which the DCO resolution is relaxed by means of additional quantizers. The jitter analysis revealed the existence of a minimum, suggesting an optimum design criterion. This property has been demonstrated in a 320 MHz PLL fabricated in 65 nm CMOS.

## Appendix A

In this Appendix, we derive the frequency responses for the blocks in the linearized model shown in Fig. 8 as in [11]. The DLF is described in the z-transform domain by the transfer function

$$H(z) = \left[\beta + \alpha/(1 - z^{-1})\right] z^{-D} \tag{46}$$

and its frequency response can be derived by using the variable substitution $z = e^{j\omega T_r}$

$$H(\omega) = \left(\beta + \frac{\alpha}{1 - e^{-j\omega T_r}}\right) \cdot e^{-j\omega T_r D}. \tag{47}$$

Assuming that $\alpha \ll \beta$, which is valid in almost any practical case to guarantee loop stability, the resulting expression can be found

$$H(\omega) \approx \left(\beta + \frac{\alpha}{j\omega T_r}\right) \cdot e^{-j\omega T_r D}, \tag{48}$$

which holds within the $[0, \omega_r/2]$ range (i.e. up to Nyquist frequency).

The first-order $\Delta\Sigma$ modulator following the DLF has a unitary signal transfer function and it can be modeled as a unitary gain block. The DCO acts as a sampled integrator, whose rate is different from that of the loop filter and it is given by the DCO frequency $f_{dco} = 1/T_{dco}$. Its transfer function is $H_{dco}(z') = K_T/(z' - 1)$, where $K_T = K_T''/\gamma$. The frequency response can be obtained by substituting $z'$ with $e^{j\omega T_{dco}}$ and by approximating for $\omega \ll 2\pi/T_{dco}$

$$H_{dco}(\omega) \approx \frac{K_T}{j\omega T_{dco}}. \tag{49}$$

The open-loop gain is thus found to be

$$G_{loop}(f) = K_{bpd} \cdot H(f) \cdot \frac{K_T}{j2\pi f T_{dco}}. \tag{50}$$

For frequencies higher than the frequency of the zero of $H(\omega)$ located at $f_z = (\alpha/\beta)(f_r/2\pi)$ with $f_r = 1/T_r$, the loop filter response can be approximated as the proportional gain $\beta$. Thus, since loop stability demands for a unity-gain frequency $f_u$ greater than $f_z$, the loop filter response at $f_u$, can be considered $|H(f_u)| \approx \beta$. After imposing $|G_{loop}(f_u)| = 1$, the unity-gain frequency can be obtained:

$$f_u \approx \frac{K_{bpd}}{2\pi T_{dco}} \cdot \beta K_T. \tag{51}$$

If the loop is designed to have safe stability margin, the open-loop gain $G_{loop}(f)$ for frequencies higher than $f_z$ can be approximated as in (27).

## Appendix B

In this Appendix, we derive (33) starting from (32) that we repeat here for the reader's convenience,

$$\sigma_{\Delta t}^2 \approx 2 \int_{f_z}^{\infty} \frac{S_{t_v}(f)}{1 + \left(\frac{f_u}{f}\right)^2} \mathrm{d}f, \tag{52}$$

Exploiting the linearity of the integral operator in (52), we split the variance into the two following contributions

$$\sigma_{\Delta t}^2 = \int_{f_z}^{\infty} \frac{2K_W}{(2\pi f)^2} \cdot \frac{1}{1 + \left(\frac{f_u}{f}\right)^2} \mathrm{d}f + \int_{f_z}^{\infty} \frac{2K_F}{f(2\pi f)^2} \cdot \frac{1}{1 + \left(\frac{f_u}{f}\right)^2} \mathrm{d}f. \tag{53}$$

The first integral in (53) gives

$$\frac{K_W}{2\pi^2 f_u} \left[\arctan \frac{f_z}{f_u}\right]_{f_z}^{\infty} = \frac{K_W}{2\pi^2 f_u} \left(\frac{\pi}{2} - \arctan \frac{f_z}{f_u}\right). \tag{54}$$

Similarly, the second integral in (53) gives

$$\begin{aligned} &\frac{K_F}{2\pi^2 f_u^2} \left( \int_{f_z}^{\infty} \frac{1}{f} \mathrm{d}f - \int_{f_z}^{\infty} \frac{f}{f^2 + f_u^2} \mathrm{d}f \right) \\ &= \frac{K_F}{2\pi^2} \frac{1}{f_u^2} \left[\ln f - \frac{1}{2} \ln\left(f^2 + f_u^2\right)\right]_{f_z}^{\infty} \\ &= \frac{K_F}{2\pi^2} \cdot \frac{1}{2f_u^2} \ln\left(1 + \frac{f_u^2}{f_z^2}\right) \end{aligned} \tag{55}$$

An insightful closed-form expression for $\sigma_{\Delta t}^2$ can be derived making a reasonable hypothesis on the ratio $\delta = f_u/f_z$. Loop stability demands that the unity-gain frequency $f_u$ is much greater than the frequency $f_z$ of the zero (i.e. $\delta \gg 1$). In such a case, we can neglect the inverse tangent term in (54) and approximate the logarithm in (55) as $2 \cdot \ln(\delta)$. Thus, rewriting the full expression of the variance, we get

$$\sigma_{\Delta t}^2 \approx \frac{K_W}{4\pi f_u} + \frac{K_F \ln(\delta)}{2\pi^2 f_u^2}, \tag{56}$$

where $\delta$ is set by the required loop-stability margin.

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