A 10-MHz Three-Level Buck Converter with Dual-Loop Time-Based Control and Flying Capacitor Voltage-Balance for Fast DVS

Gabriele Magni†, Paolo Melillo†, Alessandro Bertolini*, Mauro Leoncini†, Massimo Ghioni†
Email: mauro.leoncini@polimi.it
† Politecnico di Milano, DEIB, Milan, Italy
* STMicroelectronics, AMG R&D, Milan

***Abstract*—High efficiency, small footprint and fast dynamic response are the key parameters of power management integrated circuits for portable applications. In this context, the three-level buck converter (TLBC) emerges as a practical solution, as it doubles the switching frequency and reduces the voltage swing at the switching node, compared to a conventional buck converter. As results, a small volume inductor can be employed, and high bandwidth can be achieved without compromising the converter's efficiency. However, precise regulation of the flying capacitor voltage at half the input supply is mandatory to ensure the reliable operation of the converter. This paper presents a dual-loop time-based control for a 10-MHz 2.8∼3.6-V input and 0.6∼1.2-V output TLBC. The proposed time-based controller merges the flying capacitor and the output voltage regulation in a single structure, thus minimizing the area occupation. The controller was designed in a 180-nm BCD technology. Simulations in SIMetrix/SIMPLIS demonstrates the efficacy and the robustness of the proposed control.**

***Index Terms*—Three-Level Buck Converter, Flying Capacitance, Time-Based Control, Voltage-balance.**

I. Introduction

Portable devices and IoT applications require small footprints and efficient power management. The three-level buck converter, whose schematic is reported in Fig. 1, brings a considerable improvement since it introduces an intermediate voltage level to minimize the size of the passive component and reduce the voltage stress across the power MOS switches. This reduction is accomplished by introducing an extra flying capacitance that enables the use of low-voltage devices, thus enhancing the overall efficiency [1, 2]. Simultaneously, the effective switching frequency of the output filter is doubled, providing an opportunity to reduce the inductor's size for the same output voltage ripple. However, managing the voltage on the flying capacitor is crucial to ensure the reliable operation of the converter [3, 4]. To further minimize the die area, the compensator design plays a key role. To this aim, time-based signal processing proved to be a valuable alternative to conventional voltage-based and digital control, as it removes the power hungry error-amplifier (EA) and the pulse-width modulator (PWM) [5–8]. At high switching frequencies, these components set a limitation to the converter's bandwidth and to the minimum on-time. Time-based control encodes the information between two time events, i.e., the rising/falling edges of square-wave signals, generated by voltage-controlled oscillators and delay lines. Similarly to digital controls, only logical *high* or *low* are present inside the compensator, but no quantization error is introduced. Essentially, time-based control takes the full advantage of processing CMOS-level signals while maintaining the accuracy of a conventional voltage-based control.

979-8-3503-8630-1/24/$31.00 ©2024 IEEE

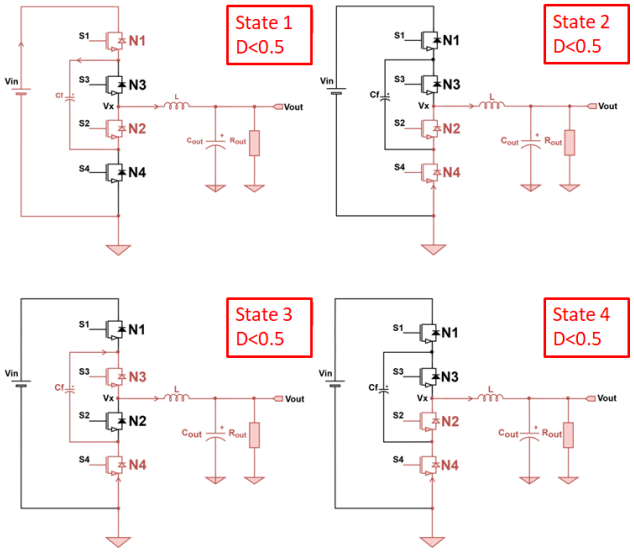

Fig. 1. Simplified schematic view of converter operating states for D<0.5. In the circuit diagram, the components highlighted in red indicate the areas directly affected by the flow of current.

In this paper, a novel flying capacitor voltage-balance (FCVB) control is presented, which exploits the same building blocks of a time-based proportional-integral-derivative (PID) compensator. The proposed controller enables a wide-bandwidth control of both the flying capacitance and the output voltage, making it suitable for dynamic voltage scaling (DVS) applications. This work is organized as follows: Sec. II provides an overview of the time-based control strategy. The proposed time-based controller with flying capacitor voltage balance is described in Sec. III. Sec. IV shows the transistor-level im-

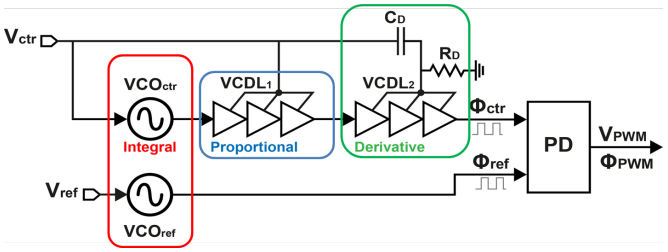

Fig. 2. Simplified block diagram of a time-based PID compensator.

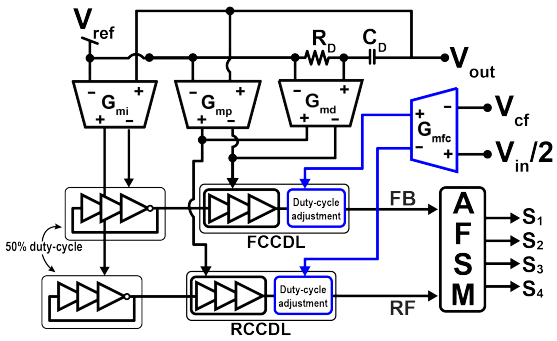

Fig. 3. Simplified block diagram of the proposed time-based PID controller with flying capacitor voltage balance.

plementation of the building blocks exploited in the controller and Sec. V reports the transient response simulation results. Conclusions are drawn in Sec. VI.

II. Time-based Control Basics

The control-to-output transfer function of a three-level converter, $G_{od}(s)$, shows a pair of complex conjugate poles. A PID compensator is chosen to regulate the output voltage and provide the maximum achievable loop crossover frequency. As shown in Fig. 2, the implementation exploits a time-based approach, where the system essentially operates as a phase-locked loop. It is composed of two voltage-controlled oscillators (VCOs), responsible for the integral action, and a voltage-controlled delay line (VCDL) which implements the proportional and the derivative actions. The VCO implements the voltage-to-time conversion and the integration of the error voltage $v_e = v_{ctrl} - v_{ref}$, with gain

$$G_i(s) = \frac{\Phi_{\text{VCO}}}{v_e} = \frac{K_{\text{VCO}}}{s}, \tag{1}$$

where Φ_{VCO} is the VCO phase, and K_{VCO} is the VCO gain, expressed in rad/(V·s). The VCDL adds a phase shift proportional to v_e, and to its derivative, obtained via a simple high-pass filter. The proportional gain, $G_p(s)$, and the derivative gain, $G_d(s)$ can be expressed as:

$$G_p(s) = \frac{\Phi_{\text{VCDL}}}{v_e} = K_{\text{VCDL}}, \tag{2}$$

$$G_d(s) = \frac{\Phi_{\text{VCDL}}}{dv_e/dt} = \frac{\frac{s}{\omega_{\text{D}}} \cdot K_{\text{VCDL}}}{1 + \frac{s}{\omega_{\text{D}}}}, \tag{3}$$

where Φ_{VCDL} is the phase of the VCDL output signal, K_{VCDL} is the VCDL gain expressed in rad/s, and $\omega_{\text{D}} = 1/(C_{\text{D}}R_{\text{D}})$ is the angular frequency of the pole introduced by the high-pass filter. Since this pole can be designed to have a frequency much higher than the loop crossover frequency, it will be neglected. The compensator transfer function, $G_{\text{T-PID}(s)}$, can be written as the sum of the integral, proportional and derivative gain as follows:

$$G_{\text{T-PID}}(s) = \frac{K_{\text{VCO}}}{s} + K_{\text{VCDL}} + s \cdot \frac{K_{\text{VCDL}}}{\omega_{\text{D}}}. \tag{4}$$

The phase detector (PD in Fig.2), which can be modeled with a block having a gain $G_{\text{PD}} = 1/2\pi$, detects the phase difference between Φ_{ctr} and Φ_{ref} to generate the driving signal of the power MOS switches.

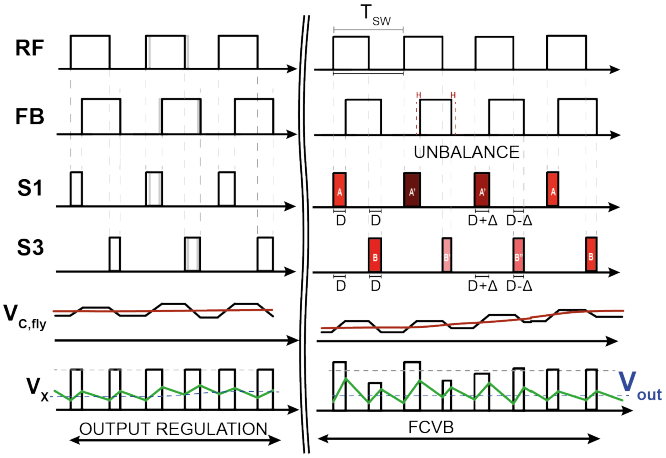

Fig. 4. Timing diagram of relevant waveforms: (left) output voltage regulation; (right) flying capacitor voltage balancing.

Starting from the T-PID, we developed a time-based flying capacitor voltage-balance (FCVB) control, as discussed in the next Section.

III. Proposed FCVB Time-Based Control

Figure 3 illustrates the proposed time-based PID with flying capacitor voltage regulation, where the phase detector is replaced by an asynchronous-finite-state-machine (AFSM). Since different control loops share the same path, it is crucial to ensure no interaction between, in order to avoid detrimental effects on the system stability and dynamic performance. The schematic waveforms of the signal $S1$ and $S3$ are shown in Fig. 4, whereas the signals $S4$ and $S2$ are selected such that $S4(t) = \overline{S1}(t)$ and $S2(t) = \overline{S3}(t)$. By increasing the duty-cycle of $S1$ and $S3$ in a common-mode fashion, the average output voltage across the output LC filter is increased with a consequent increase of the output voltage, as shown in the timing diagram in Fig. 4 (left). Conversely, the amount of charge injected in the flying capacitance in a single cycle is unchanged. The output voltage is regulated with the T-PID controller, i.e., by the circuit highlighted in black in Fig. 3. The T-PID includes a VCO and a VCDL implemented as cascade of transconductors and current-controlled-oscillators/-

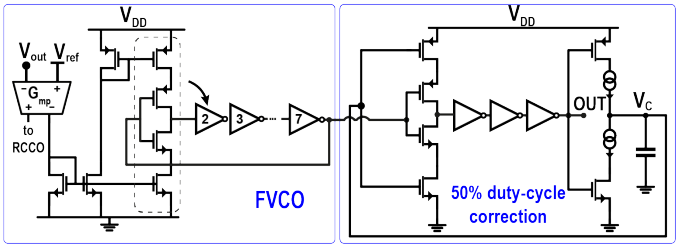

Fig. 5. Simplified schematic diagram of (left) voltage-controlled oscillator and (right) duty-cycle adjustment circuit.

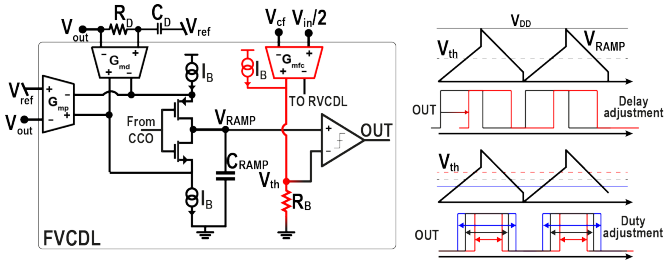

Fig. 6. Schematic illustration of the current-mode proportional and derivative control implemented in the converter using a time-based approach.

delay lines.

Figure 4 (right) illustrates the proposed control strategy for the regulation of the flying capacitance voltage. By changing the duty-cycle of $S1(t)$ and $S3(t)$ in a differential way, the average voltage across the inductor remains unchanged over a switching period. As a consequence, no perturbation is induced on the output voltage to the first order. At the same time, this mechanism affects the average current flowing in the flying capacitance, either charging or discharging it. Following this approach, the small signal transfer function, G_{df}, between a differential duty-cycle perturbation (Δ in Fig. 4) and the flying capacitance voltage, can be derived as:

$$G_{df}(s) = \frac{2I_L}{sC_f}. \tag{5}$$

This means that the FCVB is characterized by a single pole transfer function that can be regulated using the simple proportional control highlighted in blue in Fig. 3. The transconductor G_{mfc}, which takes as inputs the flying capacitance voltage V_{cf}, and $V_{in}/2$, modulates the duty-cycle using an additional path of the CCDL. In the end, the duty-cycle will be adjusted such that $V_{cf} = V_{in}/2$.

IV. Transistor-Level Implementation

In this section, the transistor-level design of the main building blocks is described. The proposed time-based compensator has been designed in a 180-nm BCD process. The case-study TLBC has a switching frequency f_{sw}=10MHz, an input voltage ranging from 2.8V to 3.6V, and an output voltage adjustable from 0.6V to 1.2V.

A. Voltage-Controlled Oscillator

The VCO, depicted in Fig. 5 (left), is designed as the cascade between a transconductor, G_{mi}, and two current-controlled oscillators (CCOs) with gain K_{CCO}. The transconductor is a simple differential pair, while the CCO includes 7 current starved inverters closed in a ring configuration. The differential structure is used to improve linearity [5]. The VCO provides an integral gain (see (1)) given by:

$$G_i(s) = \frac{G_{mi}K_{\text{CCO}}}{s}. \tag{6}$$

Since the proposed FCVB regulation requires signals with 50% duty-cycle, the output of the CCO is connected to the duty-cyle adjustment circuit reported in Fig. 5 (right). The square-wave input signal drives a charge-pump, which sets the capacitance voltage V_c. This voltage changes the rising/falling edge delay by modulating the resistance of the input inverter until a 50 % duty-cycle is reached. The inclusion of this stage has a negligible impact on the overall power consumption of the VCOs, resulting in a total loss of 153 μW accounting for both oscillators and inverters chains.

B. Voltage Controlled Delay Line

The schematic of the VCDL is depicted in Fig. 6 (left). It is composed of two transconductors G_{mp} and G_{md}, for the proportional and derivative gain respectively, a ramp voltage generator, obtained by injecting a current on a capacitor C_{RAMP} and a comparator. At every rising or falling edge of the VCDL input, the voltage V_{RAMP} is reset to V_{DD} or ground, respectively, as depicted in Fig. 6 (right). The derivative and proportional gain in (2) and (3), required for the output voltage regulation, can be computed as

$$G_p(s) + G_d(s) \simeq K_{\text{CCDL}}(G_{mp} + sG_{md}C_{\text{D}}R_{\text{D}}), \tag{7}$$

with $K_{\text{CCDL}} \simeq \frac{V_{th}C_{\text{RAMP}}f_{sw}}{I_{\text{B}}^2}$.

The flying capacitance regulation is instead achieved by changing in a differential manner the threshold voltage of the comparators, V_{th}, using the transconductor, G_{mfc}. This modifies differentially the duty-cycles of the *FB* and *RF* square waves in Fig. 3. Using this configuration, the proportional gain of the FCVB regulation, G_{VCBF}, is

$$G_{\text{VCFB}} = \frac{\Phi_{\text{CCDL}}}{v_{e,cf}} = \frac{C_{\text{RAMP}}f_{sw}R_{\text{B}}G_{mfc}}{I_{\text{B}}}, \tag{8}$$

where $v_{e,cf} = v_{cf} - v_{in}/2$ is the error signal of the flying capacitance regulation loop, and R_B is the bias resistance. The voltage across the flying capacitance is sensed with a sample and hold circuit that acquires the voltage at the phase node V_X once a period, during *state-1*. The overall power consumption, considering two delay lines, two comparators, and three transconductors, is estimated to be 650μW.

V. Simulations Results

In this section, the effectiveness of the controller is verified using SIMPLIS simulations. The controller parameters are extracted from transistor-level simulations, also accounting for process-related variations.

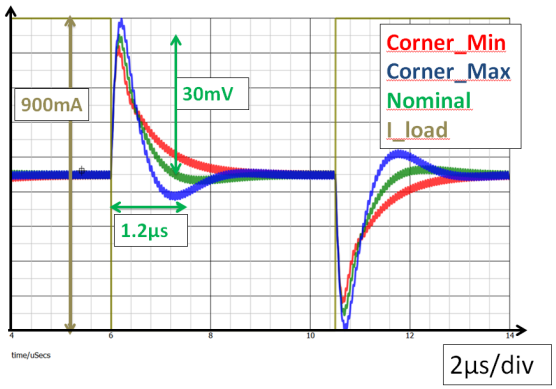

Fig. 7. Output voltage transient during a load step of 900 mA considering in different corner conditions when the input voltage is 3.3 V

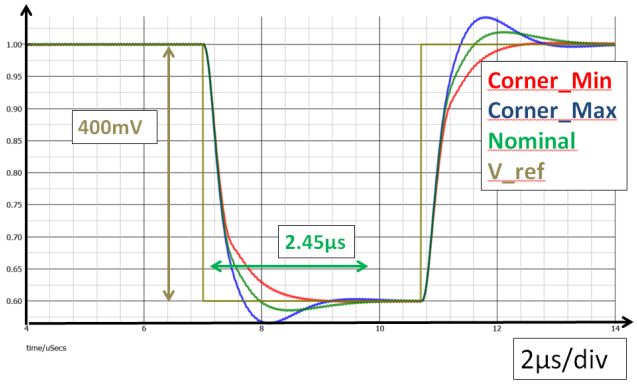

Fig. 9. Output voltage transient after a 400 mV variation of the reference voltage in different corner conditions when the input voltage is 3.3 V.

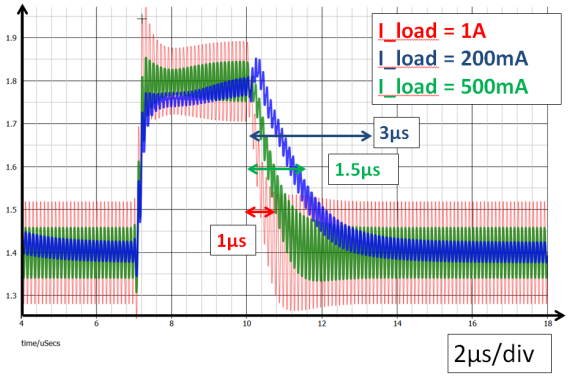

Fig. 8. Flying capacitance voltage transient after a 2.8 V to 3.6 V variation of the input voltage in different load current conditions.

Figure 7 shows the simulated transient response to a load variation. The results obtained for the typical, minimum, and maximum technology corner/mismatch, are compared. The system showcases a settling time of 1.2 μs for a step load current variation of 900 mA and a voltage overshoot/undershoot of 30 mV in the nominal conditions. The settling time and voltage variation in the corner-cases is below, 2.4 μs, and 40mV, respectively, demonstrating the robustness of the design.

Figure 8 shows the flying capacitance voltage during a step input voltage variation from 2.8 V to 3.6 V and vice-versa. The voltage quickly settles to half the input voltage within a few microseconds, thus ensuring a safe operation for each MOSFET. Although the bandwidth of the flying capacitance control loop depends on the load current (as demonstrated in Sect. III), the settling time is always small, comparable with the one of the output voltage loop.

Figure 9 shows the transient response to a 400 mV step variation of the reference voltage, for different corner conditions. The settling time in the nominal corner is 2.45 μs, demonstrating the effectiveness in DVS applications.

VI. Conclusions

In this work, a novel time-based control strategy for a 10 MHz three-level buck converter, comprising two feedback loops was presented. The controller is designed in a 180-nm BCD technology and exploits a time-based architecture which allows to share oscillators and delay lines between the two loops, thus reducing the area occupation. With the proposed control, the output voltage settles in about 1 μs in response to load transients, while the flying capacitor voltage recover its steady state in about 2 μs. This is possible thanks to the negligible interaction between the two loops. Dynamic voltage scaling is achieved within 2.5 μs for a 40% variation in the reference voltage.

References

[1] X. Ruan, B. Li, and Q. Chen, "Three-level converters-a new approach for high voltage and high power dc-to-dc conversion," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, vol. 2, pp. 663–668 vol.2, 2002.

[2] X. Liu, P. K. T. Mok, J. Jiang, and W.-H. Ki, "Analysis and design considerations of integrated 3-level buck converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 5, pp. 671–682, 2016.

[3] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-dvs," *IEEE J. of Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, 2018.

[4] W. Jung, S.-U. Shin, S.-W. Hong, S.-M. Yoo, T.-H. Kong, J.-H. Yang, S.-H. Kim, M. Choi, J. Shin, and H.-M. Lee, "Dual-path three-level buck converter with loop-free autocalibration for flying capacitor self-balancing," *IEEE Trans. on Power Electronics*, vol. 36, no. 1, pp. 51–55, 2021.

[5] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High frequency buck converter design using time-based control techniques," *IEEE J. of Solid-State Circuits*, vol. 50, no. 4, pp. 990–1001, 2015.

[6] M. Leoncini, A. Dago, A. Bertolini, A. Gasparini, S. Levantino, and M. Ghioni, "A compact high-efficiency boost converter with time-based control, rhp zero-elimination, and tracking error compensation," *IEEE Trans. on Power Electronics*, vol. 38, no. 3, pp. 3100–3113, 2023.

[7] P. Melillo, S. Zaffin, M. Leoncini, A. Brunero, A. Gasparini, S. Levantino, and M. Ghioni, "A wide-input-range time-based buck converter with adaptive gain and continuous phase preset for seamless pfm/pwm transitions," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1–12, 2024.

[8] A. Bertolini, M. Leoncini, P. Melillo, A. Gasparini, S. Levantino, and M. Ghioni, "A 1-a 90% peak efficiency 5–36v input voltage time-based buck converter with adaptive gain compensation and controlled-skip operation," *IEEE Trans. on Power Electronics*, vol. 39, no. 1, pp. 973–984, 2024.