Guest Editorial: Defect and Fault Tolerance in VLSI and Nanotechnology Systems

1 Introduction

The increasing versatility, performance, compactness and power efficiency of today's electronic systems is achieved by pushing technology to its physical limits: systems are increasing in size and complexity, comprising thousands of subsystems made of billions of devices. The devices themselves have become smaller and smaller and have reached the atomic scale, which leads to stochastic variations when fabricating them and variations caused by environmental phenomena, such as radiation, extreme temperatures, electrical fields or other kinds of disturbances. This makes components noisier and unreliable, such that designing reliable systems is extremely challenging.

In response to the growing complexity of digital systems and their increasingly challenging reliability requirements, it is imperative to consider reliability as a primary driver in electronic system design and, consequently, to employ design and analysis methods from the early phases of the design process. Reliability threats have to be analysed and identified at an early design stage and appropriate fault tolerance techniques have to be applied to overcome the occurrence of faults and to slow-down ageing effects.

This Special Issue aimed at continuing the discussion about the research activities and related findings carried out the 30th IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT 2017) held in Cambridge, UK, October 23-25th 2017. Therefore the Special Issue focuses on fundamental issues related with all aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation.

2 Topics of the Special Issue

This special issue comprises 14 articles selected after a rigorous review process from 25 initial submissions, either extended versions of papers presented at DFT 2017 or novel contributions. Accepted articles covers various aspects of reliability in integrated circuits (e.g. fault vulnerability, fault tolerance techniques or fault simulation), various architectures and devices (memory caches, GPUs or FPGAs), and focusing at different at different levels of abstraction (from circuit level to system/software level).

(i) Paper "Probabilistic Timing Analysis of Random Caches with Fault Detection Mechanisms" by Chao Chen et al proposes a novel method for static probabilistic timing analysis of random caches. The approach which uses a a state-space modelling

technique is able to account for the presence of faults and possibly-available fault detection mechanisms.

(ii) Paper “Design of Reliable Memories with Self-Error-Correction by Group Testing Based Non-Binary Codes” by Lake Bu et al present a novel cost-effective approach for the design of reliable memories by means of a class of group-testing-based error correcting codes. Together with theoretical proof, the paper also provides a detailed analysis on the hardware architecture of the reliable memories based on these codes

(iii) Paper “Scheduling Configuration Error Checks to Improve the Reliability of FPGA-based Systems” by Tran Huu Nguyen Nguyen et al defined a design-time optimization strategy for the hardening of FPGA systems by means of the combined application of Triple Modular Redundancy (TMR) and Module-based configuration memory Error Recovery (MER).

(iv) Paper “A Fluid-level Synthesis Unifying Reliability, Contamination-Avoidance, and Capacity-Wastage-aware Washing for Droplet-based Microfluidic Biochips” by Arpan Chakraborty et al presents a complete synthesis flow for microfluidic biochips considering Reliability, Contamination-Avoidance, and Capacity-Wastage-aware Washing all together in a holistic way.

(v) Paper “Kernel and Layer Vulnerability Factor to Evaluate Object Detection Reliability in GPUs” by Fernando Fernandes dos Santos et al proposes two novel metrics to analyze the fault vulnerability of applications running on GPUs, namely Kernel Vulnerability Factor (KVF) and Layer Vulnerability Factor (LVF). They indicate the probability of faults in a kernel or a layer, respectively, to affect the overall computation of an image processing application.

(vi) Paper “Removing Constant-induced Errors in Stochastic Circuits” by Paishun Ting et al proposes a systematic algorithm (CEASE) to eliminate constant-inducing random fluctuation errors degrading stochastic computing systems by introducing memory elements into the target circuits.

(vii) Paper “HASTI: Hardware-assisted Functional Testing of Embedded Processors in Idle Times” by Arezoo Kamran proposes software based self test (SBST) method that introduces the concept of modular test, where the test program is partitioned into separate modules to allow time multiplexed testing of embedded processor. Test performance is further improved by introducing memory for storing test programs.

HASTI improves utilization of idle times by executing part of full SBST program in available idle slot.

(viii) Paper “RASSS: A Hijack-resistant Confidential Information Management Scheme for Distributed Systems” by Lake Bu et al presents the design and the implementation of a secure and robust secret sharing scheme, called RASSS, to enable a more resilient sharing of confidential information in distributed system.

(ix) Paper “Study of the Monte-Carlo Fault Injection Simulator to measure a fault de-rating” by Lee and Na presents an accelerated monte-carlo fault injection method for simulating soft error rate in combinational and sequential circuits. This is achieved with the help of Verilog procedural interface and achieves more than 20-times speed improvement when compared with available statistical method.

(x) Paper “Design of An Extended 2D Mesh Network-on-Chip and Development of A Fault-Tolerant Routing Method” by Yota Kurokawa et al proposes an extension to two-dimensional mesh Network-on-Chip architecture to provide region-based fault-tolerant routing methodologies.

(xi) Paper “Soft-Error Reliable Architecture for Future Microprocessors” by Shoba Gopalakrishnan et al combines the features of space and time redundancy for improved fault-tolerance. Two proposed approaches, REMO and REMORA, are developed to provide high fault coverage with minimum overheads in hardware.

(xii) Paper “SUBHDIP: Process Variations Tolerant Subthreshold Darlington Pair Based NBTI Sensor Circuit” by Santosh Kumar Vishvakarma et al presents a novel subthreshold Darlington pair-based negative bias temperature instability (NBTI) degradation sensor for on-chip reliability measurements in very-large-scale integration (VLSI) designs.

(xiii) Paper “Leveraging Design Diversity to Counteract Process Variation: Theory, Method, and FPGA Toolchain to Increase Yield and Resilience In-sit” by Ahmad A. Alzahrani et al utilizes a pre-emptive design approach based on graph theory, which generates diverse physical implementations circumventing device resources most affected by variability or reliability issues, to produce optimal designs on FPGA.

(xiv) Paper “Yield Modeling and Analysis of Bundled Data and Ring-Oscillator Based Designs” by Yang Zhang et al proposes a mathematical model of the yield of bundled data and ring oscillator-based circuits and compares its performance to that of

comparable, traditionally used synchronous designs. The model shows that bundled data and ring oscillator-based circuits can achieve an over 50% greater yield.

3 Conclusions

All of the papers selected for this Special Issue represent world-leading current research into reliability-aware design approaches for computing systems and provide interesting and valuable insights into current and future trends and issues within these areas. We hope you will enjoy reading the papers and find them a source of inspiration for your own work.

Guest Editor Biographies

Antonio Miele is an Assistant Professor at the Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, Milano, Italy. He received his Ph.D. in Information Technology in 2010 from the same institution where he worked as postdoc research assistant from 2010 to 2014. During his doctoral studies he spent a 4-month period at European Space Agency - ESTEC in Nordwjik, Netherlands. Previously, he received the M.Sc. and the B.Sc. in Computer Science Engineering from Politecnico di Milano in 2006 and 2003 respectively. In 2006 he also got the M.Sc. in Computer Science at the University of Illinois at Chicago, USA.

His main research interests are related to the definition of design and analysis methodologies for embedded computing systems, in particular focusing on fault tolerance and reliability issues, runtime resource management in heterogeneous multi-/many-core systems and FPGA-based systems design.

Dr. Miele is co-author of more than 60 scientific publications in international peer-reviewed conference proceedings and journals. Moreover, he served as program co-chair for the DFT symposium in 2016 and in 2017, and he is part of the technical program committees of various conferences (DATE, DFT, FPL, IOLTS, ARC, DSD).

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Dr. Martin A. Trefzer is Senior Lecturer in the Department of Electronic Engineering at York. His research interests include variability-aware analogue and digital hardware design, biologically motivated models of hardware design, evolutionary computation, and autonomous fault-tolerance. He is co-investigator on 3 currently running EPSRC / DSTL projects: Spin Inspired Representations (EP/R032823/1), Platform Grant - Bio-inspired Adaptive Architectures and Systems (EP/K040820/1) and Complex In-materio Computation for Robust Dynamical Control, and the previous EPSRC projects PAnDA (EP/I005838/1) and Graceful (EP/L000563/1) [5]. He is a senior member of the IEEE, co-chair of the International Conference on Evolvable Systems (ICES), and chair of the IEEE Task Force on Evolvable Hardware.

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Dr Saqib Khursheed is currently working as a lecturer (Assistant Professor) with Department of Electrical Engineering and Electronics, University of Liverpool, UK. In 2010, he received his PhD degree in Electronics and Electrical Engineering from University of Southampton, UK. After completing his PhD, he worked as a Senior Research Fellow at the University of Southampton on two EPSRC funded research projects.

Dr Khursheed's PhD thesis secured second place in IEEE TTTC 'E. J. McCluskey Doctoral Thesis Award' at European Test Symposium (ETS 2010), while competing against the best PhD dissertations from all over Europe. He was also the winner of PhD-Plus award (2009-10).

Dr Khursheed is interested in all issues related to reliability, testability, and hardware oriented security of low-power, high-performance designs and 3D integrated circuits. He has published a number of papers in internationally leading journals and conferences in these areas. He was the General Co-Chair and Finance Chair of 31st edition of IEEE Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2018), Chicago (USA). In 2017, he served as Program Co-Chair of this symposium, which took place in Cambridge (UK). He served as the Guest Editor for a special section on “Robust 3-D Stacked ICs” in IEEE Design & Test magazine (May/June 2016 issue). He also served as the Program Chair (2012) and General Chair (2013-15) of Friday workshop on 3D Integration, collocated with the DATE Conference. He regularly reviews research papers for internationally leading journals and conferences. He is a member of IET, member of EPSRC peer review college and Fellow of The Higher Education Academy (UK).

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