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Analysis of High-Temperature Data Retention in 3D Floating-Gate NAND Flash Memory Arrays

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ABSTRACT In this paper, we present a detailed experimental investigation of high-temperature data retention in 3D floating-gate NAND Flash memory arrays. Data reveal that charge detrapping from the cell tunnel oxide and depassivation of traps in the string polysilicon channel are the physical mechanisms resulting in the most relevant long-term reliability issues for the memory array. On one hand, the two mechanisms give rise to threshold-voltage ($\mathbf{V_T}$) instabilities with similar activation energy and comparable magnitude on fresh devices. On the other hand, polysilicon trap depassivation displays a negligible strengthening with cycling and a more marked dependence on the cell $\mathbf{V_T}$ level during data retention with respect to charge detrapping. Results must be carefully considered in the reliability assessment of all state-of-the-art and future 3D NAND Flash technology nodes.

INDEX TERMS NAND Flash memory, 3D array, polysilicon, semiconductor device reliability, semiconductor device modeling.

I. INTRODUCTION

Today, the NAND Flash memory technology represents the dominant nonvolatile storage solution in terms of revenues and bit storage density [1], [2], [3], [4]. For the success of the technology, the memory array must have a robust reliability. That can be guaranteed only by tackling all the issues appearing along the evolutionary path of the technology. In this regard, turning the silicon channel of the strings from monocrystalline to polycrystalline as a by-product of the transition from planar to three-dimensional (3D) arrays has been a huge source of reliability issues for the NAND technology [2], [3], [5], [6], [7]. The high density of microscopic defects at the grain boundaries of the polysilicon channel of 3D NAND strings gives rise, in fact, to variability and short-term instability phenomena affecting cell threshold-voltage (V_T) [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. In addition, we recently reported experimental evidence for the growth of the number of active traps in the polysilicon channel of 3D NAND strings over long stretches of time spent at high temperature, due to the depassivation of some microscopic defects in the material. We showed that growth is responsible for the intensification of random telegraph noise (RTN) [20] and long-term V_T instabilities in 3D arrays [21]. Further evidence for the phenomenon was reported in [22], where it was also shown to worsen the cross-temperature (data storage and retrieval carried out at different temperatures) reliability of the array. In [22], besides, specific array working conditions able to restore the initial number of active traps in the polysilicon channel of the strings were also identified, pointing out the semi-permanent (or metastable) nature of the trap depassivation phenomenology. This phenomenology, moreover, was also traced back to the rupture of Si-H bonds in the polysilicon channel.

In this paper, by extending the preliminary results presented in [21], we show that trap depassivation in the polysilicon channel of the strings and charge detrapping from the cell tunnel oxide [23], [24] are the dominant sources of long-term V_T instabilities during high-temperature data retention in 3D NAND Flash arrays based on floating-gate

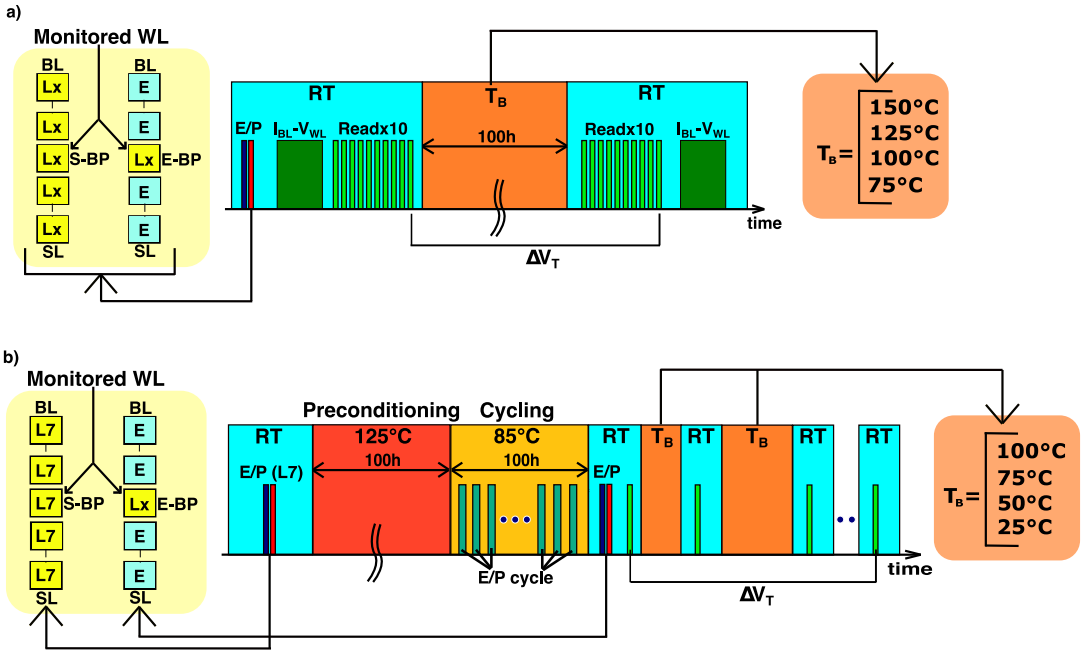

FIGURE 1. Schematics for the experimental tests considered in this work. Note that all the Read operations were carried out through the circuitry of the investigated test chips, requiring a timescale of few minutes to gather the V_T of the monitored cells.

storage. Through ad hoc experimental tests and theoretical analyses, we explore here for the first time the main dependences of the two phenomena and compare their impact on array reliability under different working conditions. The results of this investigation are of utmost importance for assessing the reliability of any 3D NAND Flash array and must be carefully considered in the development of future technology nodes.

II. HIGH-TEMPERATURE DATA RETENTION RESULTS

The samples investigated in this work are mainstream vertical-channel 3D NAND Flash arrays based on charge storage in polysilicon floating gates [25]. Floating-gate storage precludes any lateral migration of the stored charge from one cell to its first neighbors along the NAND string during data retention. That simplifies the analysis of all the other physical phenomena resulting in long-term V_T instabilities in 3D NAND Flash technologies, offering the chance to better investigate their main features and dependences as discussed in the next sections. For a detailed analysis of lateral charge migration in 3D NAND arrays exploiting a charge-trap dielectric layer as storage element, interested readers may refer to the literature in the field [26], [27], [28], [29], [30].

A. RESULTS ON FRESH (UNCYCLED) SAMPLES

As a first step in the analysis of high-temperature data retention in 3D floating-gate NAND Flash arrays, we carried out the experimental test schematically depicted in Fig. 1(a) on our samples. The test aimed to investigate the long-term V_T instabilities resulting from a 100h-long high-temperature data retention period on fresh (uncycled) arrays. V_T instabilities were monitored on the cells along the central wordline of a sub-block of the array under test. To explore the dependence of V_T instabilities on the V_T level of the monitored cells and on the string back-pattern, an Erase/Program sequence was initially employed to i) set the V_T level of the monitored cells to reproduce a randomly generated triple-level cell (TLC) pattern along their wordline and ii) create either an erased (E-BP) or a solid (S-BP) string back pattern. Then, the current I_{BL} of a few tens of bitlines was collected while reading the monitored cells with an increasing wordline voltage V_{WL}, obtaining the $I_{BL} - V_{WL}$ curve of the corresponding strings in the sub-block under test. Next, ten consecutive V_T Read operations were carried out on all the monitored cells. After that, samples were baked at a temperature T_B ranging from 75°C to 150°C, reproducing a high-temperature data retention condition for the array. At the end of the bake period, ten V_T Read operations were carried out on all the monitored cells and the $I_{BL} - V_{WL}$ curve of the same strings addressed before bake was gathered again. The V_T instabilities arising from the bake period were quantified in terms of V_T shift (ΔV_T) between the tenth Read operation carried out before and after bake on the monitored cells. In this regard, note that all the V_T Read operations and all the $I_{BL} - V_{WL}$ curve collections were run at room temperature (RT), preventing any possible impact that changes in the Read temperature may have on cell V_T [15], [16]. Besides, it is worth pointing out that, because the test in Fig. 1(a) was performed on fresh samples, the ΔV_T resulting from it are rather small. Carrying out groups of ten Read operations and evaluating ΔV_T from their last one, we minimized the possible contribution to it

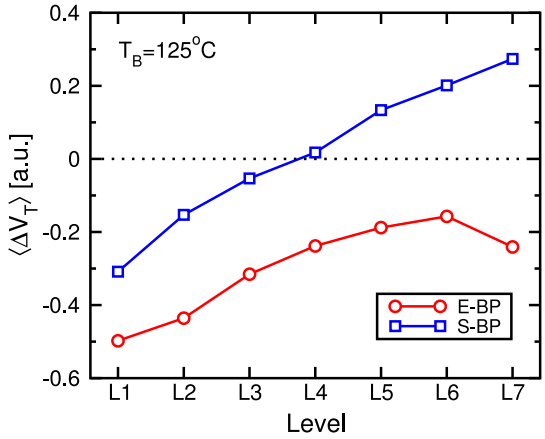

FIGURE 2. $\langle \Delta V_T \rangle$ trends with the cell V_T level obtained from the test in Fig. 1(a) in the case of $T_B = 125°C$, E-BP, and S-BP. The voltages reported in all the figures of this work have been normalized to the same arbitrary constant.

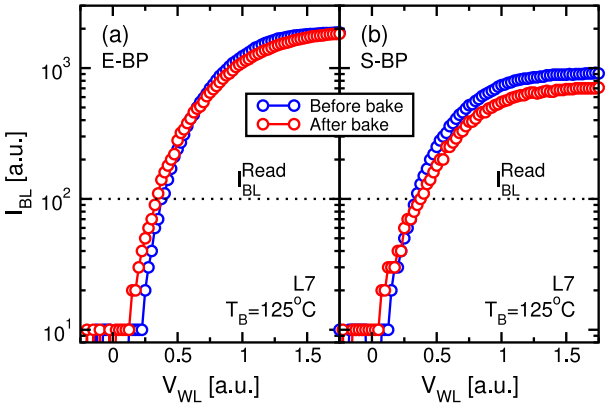

FIGURE 3. Representative example for the $I_{BL} - V_{WL}$ curves obtained from the test in Fig. 1(a) in the case of (a) E-BP and (b) S-BP, $T_B = 125°C$ and monitored cell on level L7.

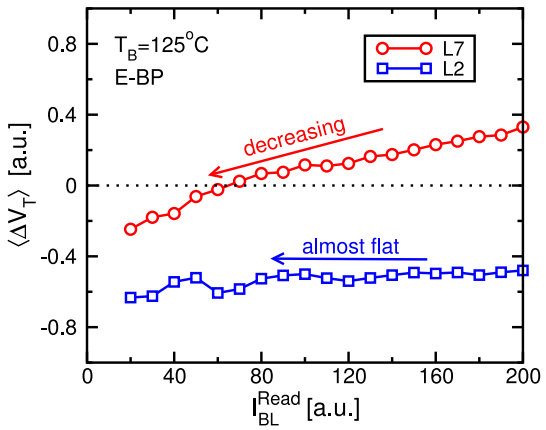

FIGURE 4. $\langle \Delta V_T \rangle$ trend with I_{BL}^{Read} resulting from the $I_{BL} - V_{WL}$ curves obtained from the test in Fig. 1(a) in the case of E-BP, $T_B = 125°C$ and monitored cells on level L2 or L7.

from transient phenomena arising when moving the array from a data retention to a Read condition [11], [13], [19].

Fig. 2 shows the average value of ΔV_T ($\langle \Delta V_T \rangle$) resulting from the test as a function of the cell V_T level, in the case of $T_B = 125°C$, E-BP, and S-BP. The $\langle \Delta V_T \rangle$ trend with the cell V_T level and its dependence on the string back pattern are far different from what typically observed on planar NAND Flash arrays. In planar NAND arrays, in fact, high-temperature data retention has always been reported to give rise to negative $\langle \Delta V_T \rangle$ increasing in magnitude with the increase in the cell V_T level due to the dominant contribution of charge detrapping to cell V_T instabilities [23], [24], [31], [32]. In this regard, the negative sign of the $\langle \Delta V_T \rangle$ values arising from charge detrapping is one of the specific features of the phenomenon observed on all planar Flash technologies, regardless of type of memory (NAND or NOR), cell dimensions, tunnel-oxide thickness and cell gate stack composition [23], [24], [31], [32], [33], [34], [35]. As demonstrated in Section II-B and in [30], charge detrapping remained a major reliability issue and its $\langle \Delta V_T \rangle$ remained negative even in the case of 3D NAND Flash technologies. The results in Fig. 2 suggest, therefore, that in the case of 3D NAND cells, charge detrapping cannot be the only physical mechanism coming into play during high-temperature data retention. An additional mechanism producing positive $\langle \Delta V_T \rangle$ must be active and give rise to relevant long-term V_T instabilities. By exploring the changes induced by the bake period in the $I_{BL} - V_{WL}$ curve of the monitored strings, in [21] we identified the additional mechanism in the growth of the number of active traps in the polysilicon channel of 3D NAND strings at high temperature. That growth was attributed to the depassivation of some microscopic defects in the material and results in the degradation of the subthreshold swing (STS) of the $I_{BL} - V_{WL}$ curves after bake both in the case of E-BP and S-BP, as shown in Fig. 3. In the case of S-BP, moreover, polysilicon trap depassivation is also responsible for a decrease in the saturation current of the string after bake. The combination of polysilicon trap depassivation and charge detrapping (and, possibly, charge loss from the cell storage layer) makes the $\langle \Delta V_T \rangle$ trend for E-BP nonmonotonic with the cell V_T level and lower than that for S-BP in Fig. 2 (see [21] for further comments and explanations and for results on the ΔV_T statistics).

Extending the previous considerations, we tried to get preliminary information on the quantitative contributions to the $\langle \Delta V_T \rangle$ values reported in Fig. 2 by inspecting the collected $I_{BL} - V_{WL}$ curves at different Read current levels I_{BL}^{Read}. Because polysilicon trap depassivation gives rise to a degradation of cell STS after bake (see Fig. 3), the contribution of the phenomenon to $\langle \Delta V_T \rangle$ should decrease when the latter is extracted at a lower I_{BL}^{Read}. This clearly appears in Fig. 4, where the $\langle \Delta V_T \rangle$ obtained in the case of monitored cells on level L7 displays a clear decreasing trend with the reduction of I_{BL}^{Read}. This trend should, eventually, reach saturation when I_{BL}^{Read} is so low to make the contribution to $\langle \Delta V_T \rangle$ from polysilicon trap depassivation negligible with respect to that from charge detrapping (remember that the latter phenomenon results mainly in a rigid leftward shift

of the $I_{BL} - V_{WL}$ curve). However, such a saturation is not reached over the I_{BL}^{Read} interval explored in Fig. 4 in the case of cells on level L7, preventing a simple extraction of the charge detrapping contribution to $\langle \Delta V_T \rangle$ for that level. That simple extraction is, instead, possible for the lowest cell V_T levels. Fig. 4 shows, in fact, that $\langle \Delta V_T \rangle$ is almost flat with the reduction of I_{BL}^{Read} in the case of cells on level L2. This means that polysilicon trap depassivation has a marked dependence on the cell V_T level and is almost negligible with respect to charge detrapping for level L2 and, in turn, L1. A similar conclusion is also supported by the RTN intensification results reported in [20] and by the experimental analyses presented in [22].

The results in Fig. 4 represent a starting point to split the polysilicon trap depassivation and charge detrapping contributions to $\langle \Delta V_T \rangle$. Such splitting, however, requires first the exploration of the V_T level dependence of charge detrapping, as done in the next section.

B. POST-CYCLING RESULTS

As a second step in the analysis of high-temperature data retention in 3D floating-gate NAND Flash arrays, we devised the test schematically depicted in Fig. 1(b) to address the impact of cycling on the long-term V_T instabilities of our samples. In the test, some fresh sub-blocks of the investigated sample were initially erased and uniformly programmed to level L7. Then, the sample underwent a so-called preconditioning phase, consisting of a 100h bake at 125°C. In this phase, we aimed to remove the contribution to the test results of charge detrapping and polysilicon trap depassivation arising from the native state of the memory cells and not from array cycling. Charge detrapping features, in fact, a high temperature activation and polysilicon trap depassivation should do the same (see [21] and Section II-C). A 100h preconditioning phase at 125°C spent with the cells under test on the highest TLC V_T level is then expected to remove the native contribution of the phenomena over subsequent stretches of time of even longer duration if spent at lower temperature. With that in mind, in the test of Fig. 1(b), the preconditioning phase was followed by a cycling phase (100h, 85°C) and by a monitoring phase consisting of RT V_T Read operations performed in-between bake periods of increasing duration and temperature $T_B \leq 100$°C. Thanks to the preconditioning phase of the test, the V_T instabilities showing up during the monitoring phase should result just of the cycling phase and not of the native state of the memory cells. During the cycling phase, the sub-blocks under test were subjected to a number of TLC Program/Erase cycles (N_{cyc}) ranging from 10 to 10k. At its end, the same sub-blocks were programmed to create a random TLC cell V_T pattern along their central wordline and an E-BP string back pattern. During the monitoring phase, V_T instabilities were quantified in terms of ΔV_T between the first and the next Read operations carried out on the cells along the central wordline of the sub-blocks (monitored cells).

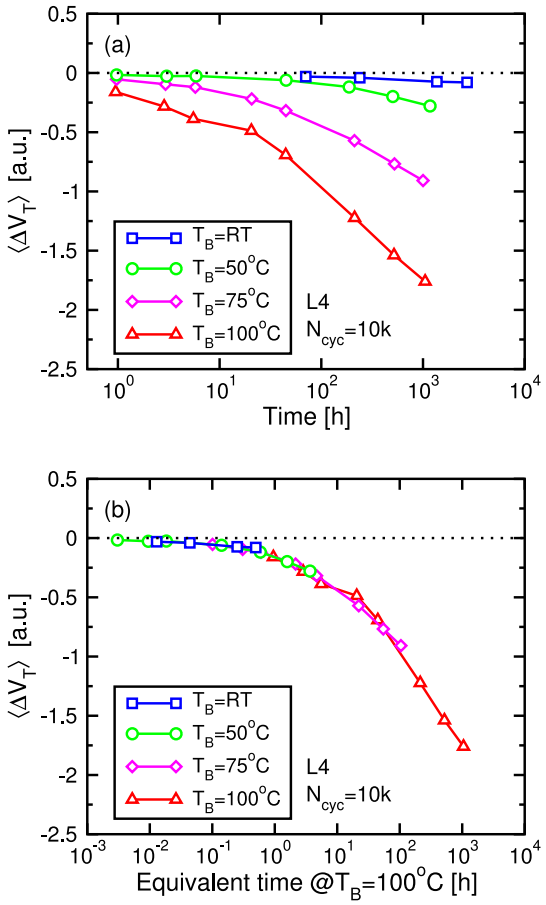

FIGURE 5. Representative example for the $\langle \Delta V_T \rangle$ transients obtained from the test in Fig. 1(b) as a function of the cumulated bake time t_B, for different T_B (the example refers to cells on level L4, $N_{cyc} = 10$k). In (a), the transients are shown as measured. In (b), they were horizontally shifted to merge over a unique trend, keeping fixed the curve at $T_B = 100$°C.

Fig. 5(a) shows a representative example for the transients obtained when reporting $\langle \Delta V_T \rangle$ as a function of the corresponding cumulated bake time t_B in the monitoring phase of the test. Only negative $\langle \Delta V_T \rangle$ values were obtained for any t_B, T_B, N_{cyc}, and V_T level of the monitored cells. Fig. 5(b) shows, besides, that the transients can be nicely merged over a unique trend through a horizontal shift along the t_B axis. The Arrhenius plot resulting from the time factors needed to reach such merging is reported in Fig. 6 and reveals that, over the explored T_B range, the temperature activation of the $\langle \Delta V_T \rangle$ transients can be described through a single activation energy E_A nearly equal to 1.1 eV. Such an E_A value represents another specific signature of charge detrapping observed over all Flash technology generations in the past [23], [24], [31], [32], [33], [34], [35]. These results suggest, therefore, that charge detrapping introduces the dominant contribution to $\langle \Delta V_T \rangle$ in the test of Fig. 1(b) and that not only polysilicon trap depassivation but also charge loss from the cell storage layer play a negligible role during the monitoring phase of that test. To further support this conclusion, Fig. 7 shows the variance of cell ΔV_T

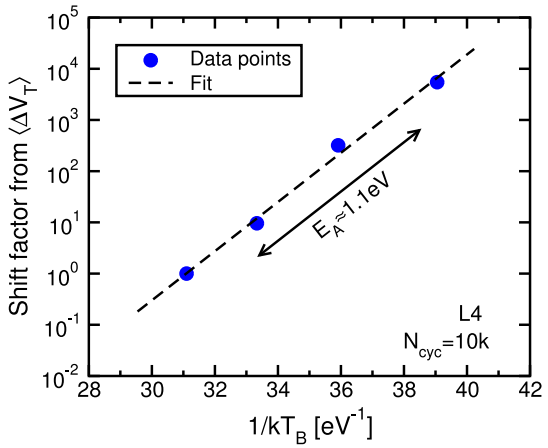

FIGURE 6. Arrhenius plot obtained from the time factors needed to merge the curves in Fig. 5 over a unique trend.

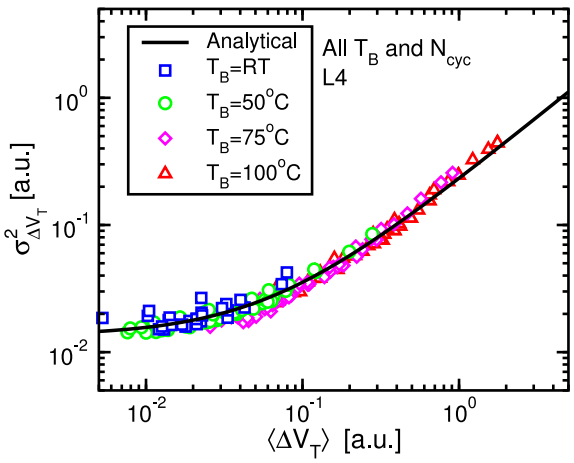

FIGURE 7. Scatter plot obtained by reporting all the $\sigma^2_{\Delta V_T}$ data as a function of their corresponding $\langle \Delta V_T \rangle$ available for different T_B and N_{cyc} from the test in Fig. 1(b), in the case of cells on level L4 during the monitoring phase.

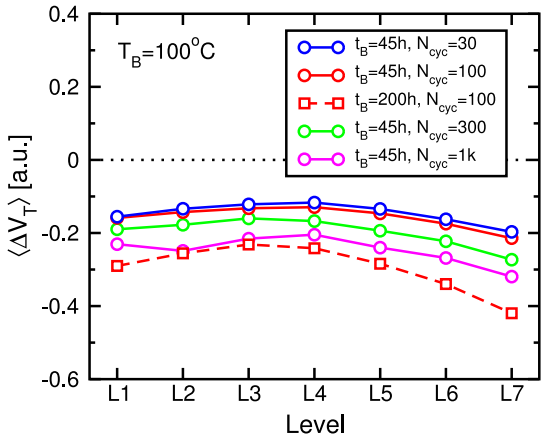

FIGURE 8. $\langle \Delta V_T \rangle$ trends with the cell V_T level during data retention obtained from the test in Fig. 1(b) in the case of $T_B = 100°C$ and different t_B and N_{cyc}.

$(\sigma^2_{\Delta V_T})$ reported as a function of its corresponding $\langle \Delta V_T \rangle$ in a scatter plot, considering all the data points obtained for a given cell V_T level during the monitoring phase at different T_B and N_{cyc}. A nice merging of the experimental data over a unique trend clearly appears. That trend can be nicely reproduced by the following relation:

$$\sigma^2_{\Delta V_T} = -\langle \Delta V_T \rangle \cdot \left(\langle \Delta V_{T,1} \rangle + \frac{\sigma^2_{\Delta V_{T,1}}}{\langle \Delta V_{T,1} \rangle} \right) + \sigma^2_{\Delta V_T^{RTN}} \quad (1)$$

where the first term on the right-hand side is what expected from charge detrapping [24], [31] and the second is a constant term arising from RTN (the latter mechanism introduces a floor in $\sigma^2_{\Delta V_T}$ due to the short-term fluctuation of cell V_T appearing whenever comparing the outcome of two subsequent Read operations).

The results in Figs. 5-7 represent solid proof that the high-temperature preconditioning phase in the test of Fig. 1(b) allowed to activate polysilicon trap depassivation to an extent that made the occurrence of the phenomenon negligible for the subsequent phases of the test. Moreover, the negligible role of polysilicon trap depassivation during the monitoring phase of the test also reveals that, differently from charge detrapping, that physical mechanism is not activated by cycling. Thanks to the preconditioning phase and the negligible activation with cycling of polysilicon trap depassivation, then, the test of Fig. 1(b) allows to easily address charge detrapping and its main dependences in the investigated 3D arrays. It is worth remarking that quite different results would have been obtained if the preconditioning phase were not included in the test.

The dominant role of charge detrapping on the results of the test in Fig. 1(b) allows for a direct exploration of the V_T level dependence of the $\langle \Delta V_T \rangle$ values arising from the phenomenon at a given t_B, T_B, and N_{cyc}. Some representative examples of such dependence are reported in Fig. 8. Results reveal a rather weak change of $\langle \Delta V_T \rangle$ with the cell V_T level. More specifically, $\langle \Delta V_T \rangle$ remains almost flat or displays a very slight increase moving from L1 to L4 and then weakly decreases moving from the latter level to L7. This behavior is somewhat different from that observed for charge detrapping on planar NAND Flash technologies in the past. On those technologies, in fact, charge detrapping has always produced a stronger and monotonic increase in the $\langle \Delta V_T \rangle$ magnitude moving from the lowest to the highest cell V_T level [23]. The reasons behind the weak $\langle \Delta V_T \rangle$ dependence on the cell V_T level appearing from Fig. 8 in the case of 3D arrays are still under investigation and are, anyway, beyond the scope of this work. What is important to point out here is that combinations of T_B, t_B, and N_{cyc} giving similar $\langle \Delta V_T \rangle$ values on level L1 also result in similar $\langle \Delta V_T \rangle$ trends with the cell V_T level as demonstrated by the set of curves reported in Fig. 8. This piece of evidence is exploited in the next section to split the contributions to $\langle \Delta V_T \rangle$ arising from charge detrapping

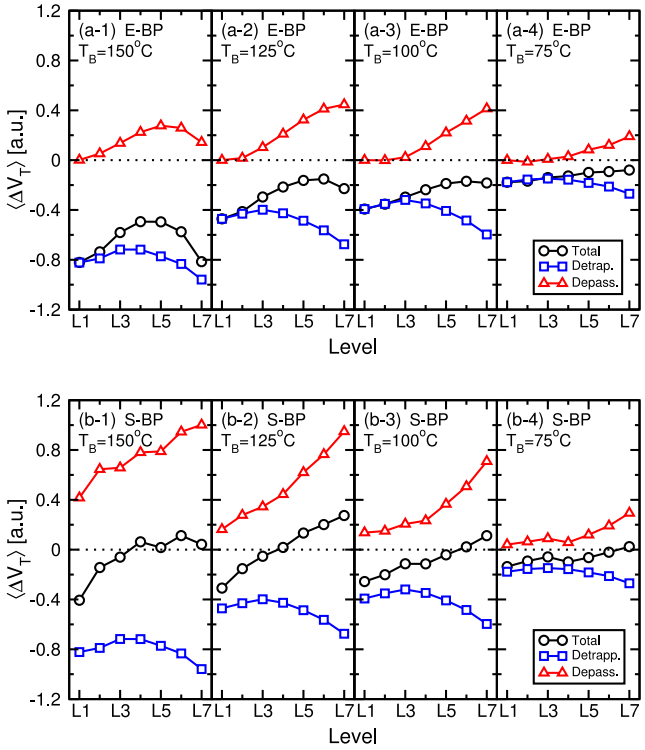

FIGURE 9. Decomposition of the $\langle \Delta V_T \rangle$ trends with the cell V_T level obtained from the test in Fig. 1(a) in their charge detrapping and polysilicon trap depassivation contributions, in the case of (a-1)-(a-4) E-BP and (b-1)-(b-4) S-BP, at different T_B. In (a-1), the downward bending of the curve for polysilicon trap depassivation at high cell V_T levels may be due to inaccuracies in the extraction procedure at very high T_B, where some changes in the charge detrapping phenomenology may occur [36].

and polysilicon trap depassivation in the case of fresh samples.

C. SPLITTING THE CONTRIBUTIONS TO $\langle \Delta V_T \rangle$ ON FRESH SAMPLES

To split the contributions to $\langle \Delta V_T \rangle$ arising from charge detrapping and polysilicon trap depassivation in the case of fresh samples (results from the test in Fig. 1(a)), we made use of two achievements reached through the analyses reported in the previous sections. The first one, obtained in Section II-A, is that the contribution to $\langle \Delta V_T \rangle$ from polysilicon trap depassivation is negligible on the lowest cell V_T levels. The second one, obtained in Section II-B, is that the contribution to $\langle \Delta V_T \rangle$ from charge detrapping changes only weakly with the cell V_T level and, more importantly, with a trend that is almost set for all the test conditions leading to the same $\langle \Delta V_T \rangle$ on level L1.

Starting from the previous two achievements, we considered that the $\langle \Delta V_T \rangle$ value obtained for level L1 and E-BP in Fig. 2 results from charge detrapping only. Besides, the contribution of charge detrapping to the results in the figure for the other cell V_T levels and E-BP was obtained by vertically shifting a $\langle \Delta V_T \rangle$ trend resulting from the test in Fig. 1(b) to make it merge with the data point in Fig. 2 on level L1. (In doing that, care was taken to considered a $\langle \Delta V_T \rangle$ trend already very close to the latter data point). The contribution from polysilicon trap depassivation to the $\langle \Delta V_T \rangle$ values reported in Fig. 2 was then calculated by subtracting the charge detrapping contribution from them. Fig. 9(a-2) shows the outcome of this procedure. Results reveal that polysilicon trap depassivation displays a stronger increase in magnitude with the increase in the cell V_T level than charge detrapping. As shown in Figs. 9(a-1)-(a-4), the same conclusion can be drawn by repeating the analysis on the data obtained at different T_B from the test in Fig. 1(a). The results in Figs. 9(a-1)-(a-4), moreover, reveal for polysilicon trap depassivation a temperature activation similar to that of charge detrapping.

To complete the analysis on fresh samples, Figs. 9(b-1)-(b-4) show the outcome of the splitting of the $\langle \Delta V_T \rangle$ values for S-BP into the contributions from charge detrapping and polysilicon trap depassivation. In the figures, the same charge detrapping curves extracted for E-BP were assumed, leading to stronger $\langle \Delta V_T \rangle$ from polysilicon trap depassivation. This agrees with the results of the analysis of the $I_{BL} - V_{WL}$ curve reported in [21] and attributing the differences in the $\langle \Delta V_T \rangle$ values for E-BP and S-BP to the degradation of the saturation current of the string due to polysilicon trap depassivation in the latter back pattern.

III. CONCLUSION

In this paper, we have quantitatively investigated the contributions to the long-term V_T instabilities of 3D floating-gate NAND Flash arrays showing up during high-temperature data retention. Charge detrapping and polysilicon trap depassivation were identified as the dominant sources of those instabilities on fresh and cycled samples, providing a first-time comparison of their dependence on temperature, cycling, and cell V_T level during data retention. The analysis represents an important step towards more complete investigations of the polysilicon trap depassivation phenomenology, which are beyond the scope of this work, and a more complete understanding of 3D NAND Flash reliability.

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