Source:
Title: A 1-A 90% Peak Efficiency 5–36 V Input Voltage Time-Based Buck Converter With Adaptive Gain Compensation and Controlled-Skip Operation
Authors: A. Bertolini, M. Leoncini, P. Melillo, A. Gasparini, S. Levantino and M. Ghioni
Published in: IEEE Transactions on Power Electronics
Date of Publication: 28 September 2023
DOI: 10.1109/TPEL.2023.3320354

A 1-A 90% Peak Efficiency 5–36-V Input Voltage Time-Based Buck Converter with Adaptive Gain Compensation and Controlled-Skip Operation

Alessandro Bertolini, Mauro Leoncini, *Member, IEEE*, Paolo Melillo, *Student Member, IEEE*, Alessandro Gasparini, Salvatore Levantino, *Senior Member, IEEE*, Massimo Ghioni, *Senior Member, IEEE*

***Abstract*—Compared to analog and digital controls, time-based control makes it possible to reduce both area occupation and power consumption, especially in converters operating at high switching frequencies. In this paper, we present a time-based buck converter with wide input voltage range for general-purpose applications. A controlled-skip operation is embedded in the PID controller to increase the light-load efficiency. To avoid large variations of the open-loop crossover frequency caused by the input voltage ranging from 5 to 36 V, an adaptive compensation of the controller gain is adopted based on a novel design methodology. These solutions are verified with a prototype buck converter implemented in a 0.18-μm BCD process, which provides an output voltage of 3.3 V and a load current capability of 1 A. The measured converter peak efficiency is 90%. The efficiency is increased from 48% to 70% at 10-mA load current and 5 V input voltage, when the converter operates in controlled-skip mode. The seamless transition between the two operation regimes is guaranteed by a finite-state machine logic, without requiring a dedicated circuit. The crossover frequency varies only by a factor of 1.8 over the input voltage range and a line regulation of 0.33 mV/V is obtained.**

***Index Terms*—DC-DC power converters, time-based control, buck converter, PID, adaptive compensation, light load efficiency.**

I. Introduction

THE trend towards DC-DC converters with smaller footprint, fast tracking and load transient response is driving the industry to ever higher switching frequencies. At the same time, it is desired to keep power consumption and area occupation of control circuits as small as possible, without compromising effectiveness and robustness. Meeting those requirements is becoming harder and harder in fixed-frequency pulse-width modulated (PWM) controllers. As a matter of fact, analog PWM controllers require an error-amplifier with large gain-bandwidth product (GBWP) and bulky passive components. The hysteretic and constant on-time (COT) control, investigated in [1]–[4], enables fast transient responses at small area and power consumption, but compromises static regulation. On the other hand, digital controllers [5]–[8] require an analog-to-digital converter (ADC) and a high-resolution and high-speed digital PWM generator, that increases the controller area occupation and power [6], [8].

An alternative approach consists in converting the voltage or current feedback signal into a time information and then performing all the control functions in the time domain. With this approach, the information is coded in the time difference between two events, allowing the controller to operate with CMOS digital-like signals without adding any quantization error. Time-based control has been recently demonstrated to achieve significant controller area and power reduction with respect to standard analog and digital implementations [9]–[13].

In this paper, we present a time-based buck converter with wide input voltage range for general purpose applications in a bipolar-CMOS-DMOS (BCD) process. A major issue arising from the wide input voltage range is the corresponding large variation of the open-loop crossover frequency, which affects both closed-loop bandwidth and phase margin, and, in turn, the system steady-state and dynamic performance. To ensure the converter properly operates at any input voltage, the worst case should be considered in the closed-loop compensation, thus compromising dynamic performances at low input voltages. We here instead present a novel design methodology, based on an adaptive proportional-integral-derivative (PID) controller, which achieves nearly constant bandwidth at any input voltage, without impairing the static line regulation.

Another well-known issue in fixed-frequency converters is the efficiency drop at light loads caused by gate-driving losses. This problem is even worse in converters having a wide input voltage range, due to the need for larger power MOSFET devices. Although the light-load efficiency of a time-based buck converter can be improved by adding a pulse frequency modulation (PFM) control [12], a dedicated circuit is needed to ensure seamless transitions between PFM and PWM operation. A more compact solution is introduced here, which provides stable and predictable controlled-skip operation at light loads over the wide input-voltage range. We demonstrate that seamless transition between controlled skip operation and the standard continuous conduction mode (CCM) operation can be handled by a simple finite-state machine (FSM) logic, without requiring a dedicated circuit.

The paper is organized as follows: in Sect. II, the time-based control in a DC/DC converter is reviewed. Section III is devoted to the description of the proposed adaptive gain compensation and controlled skip operation. Section IV

M. Leoncini, P. Melillo, S. Levantino, and M. Ghioni are with Dipartimento di Elettronica e Informazione, Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy (Phone: +39-02-2399-4035. E-mail: mauro.leoncini@polimi.it, paolo.melillo@polimi.it, salvatore.levantino@polimi.it, massimo.ghioni@polimi.it).

A. Bertolini and A. Gasparini are with STMicroelectronics Srl, Via Tolomeo 1, 20007, Cornaredo, Italy. (E-mail: alessandro.bertolini@st.com, alessandro.gasparini@st.com)

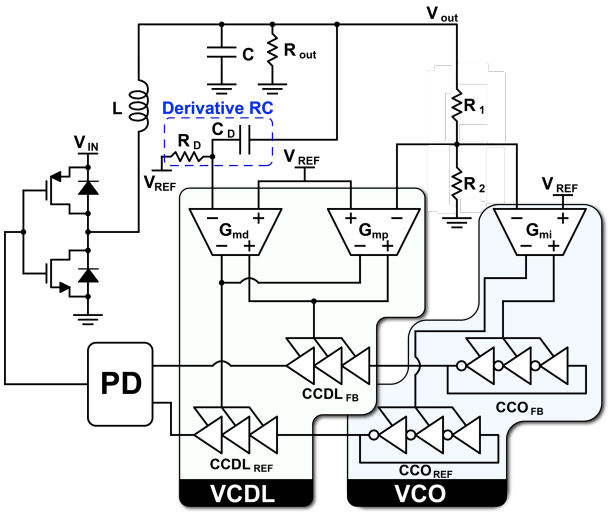

Fig. 1. Simplified block diagram of a buck converter exploiting the time-based PID compensator proposed in [9].

is focused on the circuit implementation. Section V shows the measurement results. Finally, conclusions are drawn in Sect. VI.

II. Time-based PID control

Figure 1 shows the the block diagram of a buck converter using a time-based PID compensator with a differential architecture [9]. The parameters L, C, V_{IN}, V_{out}, R_{out}, and V_{REF} are the filter inductance and capacitance, the input and output voltage, the output load resistance, and the reference voltage, respectively. R_1 and R_2 belong to the voltage divider network used to set the DC output voltage value, whereas all the other components are the core of the time-based control and they will be addressed later in this section.

The integral transfer function is obtained using a voltage-controlled oscillator (VCO) that generates a square-wave signal having a frequency that depends on the applied control voltage. The VCO is implemented by combining a differential transconductor and two current-controlled-oscillators (CCOs) leading to a transfer function from the control voltage, v_c, to the output phase, ϕ_{VCO}, given by:

$$\frac{\phi_{VCO}}{v_c}(s) = \frac{G_{mi}K_{CCO}}{s}, \tag{1}$$

where G_{mi} is the integral transconductance and K_{CCO} is the CCO gain, expressed in [rad/A·s]. The differential architecture with the two controlled oscillators, CCO_{FB}, CCO_{REF} prevents the steady-state switching frequency from changing with the output voltage [9].

The proportional transfer function is obtained with a voltage-controlled delay-line (VCDL) implemented by combining a differential transconductor and two current-controlled delay-lines (CCDLs). Each CCDL takes the CCO output signal as an input, adding to it a delay whose value is proportional to the applied control voltage. The voltage-to-phase transfer function is given by:

$$\frac{\phi_{VCDL_P}}{v_c} = G_{mp}K_{CCDL}, \tag{2}$$

where G_{mp} is the proportional transconductance and K_{CCDL} is the gain of the CCDL, expressed in [rad/A].

Since there is no straightforward technique to implement a derivative transfer function directly in the time-domain, the simplest solution is to perform a derivative action in the voltage domain using a first-order high-pass filter (C_D, R_D) cascaded to a VCDL. The resulting transfer function is

$$\begin{aligned}\frac{\phi_{VCDL_D}}{v_c}(s) &= \frac{sR_DC_D}{(1+sR_DC_D)}G_{md}K_{CCDL} \\ &\simeq sR_DC_DG_{md}K_{CCDL},\end{aligned} \tag{3}$$

where G_{md} is the derivative transconductance. The pole of the high-pass filter located above the crossover frequency of the control loop is neglected.

The outputs of the two CCDLs are then used to generate the PWM signal by means of a phase-detector (PD). Differently from the PWM generator used in the digital and voltage-mode control, this component is a simple digital gate with negligible impact on power consumption and area occupation.

The time-based PID transfer function, $G_{PID}(s)$, is obtained by summing (1), (2), and (3), taking into acccount the voltage division $N = R_2/(R_1+R_2)$ of V_{out}:

$$G_{PID}(s) = K_P + \frac{K_I}{s} + s\cdot K_D, \tag{4}$$

where

$$K_I = N\cdot G_{mi}K_{CCO} \tag{5a}$$
$$K_P = N\cdot G_{mp}K_{CCDL} \tag{5b}$$
$$K_D = C_DR_DG_{md}K_{CCDL}. \tag{5c}$$

Equation (4) can be rewritten as:

$$G_{PID}(s) = K_I\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s}, \tag{6}$$

where ω_{z1} and ω_{z2} are the angular frequencies of the two zeros generated by the PID network. Thus, the proportional and derivative gain can be also written as

$$K_P = K_I\cdot\frac{\omega_{z1}+\omega_{z2}}{\omega_{z1}\omega_{z2}}; \tag{7a}$$
$$K_D = K_I\cdot\frac{1}{\omega_{z1}\omega_{z2}}. \tag{7b}$$

III. Controller design

The prototype converter is a general-purpose buck converter having a wide input voltage range to target the 12-V and 24-V automotive applications. The minimum and the maximum input voltage are set to 5 and 36 V, respectively, to be compliant with the ISO 16750-2 international standard [14]. The system is designed to provide an output voltage of 3.3 V and a maximum current of 1 A while operating in CCM with a switching frequency f_{sw} of 1.5 MHz. A filter inductance of 4.7 μH was selected to limit the peak-to-peak current ripple to about $\pm$25% of the maximum load current in the worst operating condition. An output capacitance of 30 μF was selected to limit the output voltage variation to less than 1% of the nominal value during a load transient, when the converter operates with input voltages of 12-V or

24-V [15]. The following subsections will discuss the key features of the novel time-based PID controller, namely the *adaptive gain compensation*, which is designed to make the crossover frequency insensitive to input voltage variations, and the *controlled skip* operation, to improve the converter power efficiency in light-load conditions.

A. Adaptive gain compensation

The control-to-output transfer function, $G_{vd}(s)$ of a buck converter working in CCM is given by:

$$G_{vd}(s) = \frac{V_{IN}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}, \tag{8}$$

where Q and ω_0 are the quality factor and the angular resonance frequency of the output L-C filter, respectively. The open loop gain is obtained by combining (4) and (8):

$$\begin{aligned} T(s) &= \frac{1}{2\pi} G_{vd}(s) \cdot G_{PID}(s) = \\ &= \frac{1}{2\pi} \cdot \frac{V_{IN} K_I}{s} \cdot \frac{1 + \frac{K_P}{K_I} s + \frac{K_D}{K_I} s^2}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}, \end{aligned} \tag{9}$$

where $1/2\pi$ is the PD gain expressed in [1/rad]. Equation (9) shows that the crossover angular frequency, ω_c, of the open loop gain is proportional to V_{IN}, provided that the complex conjugate poles are properly compensated by the two real zeros. To guarantee loop stability over a wide range of input voltages, ω_c has to be designed such that its maximum value, which is usually limited to less than $\omega_{sw}/5$, occurs in the worst case of maximum input voltage, $V_{IN,max}$. As a result, at the minimum input voltage, $V_{IN,min}$, the crossover frequency is reduced by the ratio $V_{IN,min}/V_{IN,max}$, thus degrading the dynamic performance [15].

In conventional voltage-mode controllers, this issue is addressed by exploiting a feedforward compensation: the slope of the sawtooth waveform in the pulse-width modulator is varied in proportion to V_{IN} [16]. This technique is obviously inapplicable in time-based controlled converters, because of the lack of the pulse-width modulator.

Looking at (9), the crossover frequency can be made insensitive to V_{IN} also by adopting a nonlinear adaptive PID compensator, where the coefficients K_P, K_I, and K_D are made proportional to $1/V_{IN}$. On the basis of (5), those input-voltage-dependent PID coefficients can be obtained by adapting the transconductances G_{mp}, G_{mi}, and G_{md}. However, as shown in details in the Appendix, a G_{mi} variable with V_{IN} would lead to a poor static line regulation. To avoid this drawback, we can maintain a constant G_{mi} and therefore a constant K_I, and follow the procedure here described to adapt K_P and K_D. Under the assumption of $\omega_c \gg \omega_0$, which is reasonably verified in well-designed systems, (9) can be simplified as

$$T(s) \simeq \frac{V_{IN} K_D \omega_0^2}{2\pi s}. \tag{10}$$

According to (10), the dependence of ω_c on V_{IN} can be eliminated by simply making K_D inversely proportional to V_{IN}, i.e.

$$K_D = \frac{K_I}{\omega_{z1}\omega_{z2}} = \frac{K_{DV}}{V_{IN}}, \tag{11}$$

TABLE I
CONTROLLER PARAMETERS

Parameter	Value
K_{DV}	1.1 ms
K_{PV}	124
K_I	518 krad/(V· s)
ω_c	1250 krad/s
ω_{z1_o}	28 krad/s
ω_{z2_o}	84 krad/s
R_D	150 kΩ
C_D	2 pF
φ_m	68 deg

where K_{DV} is a constant expressed in [s]. By replacing (11) into (10), K_{DV} is given by

$$K_{DV} = 2\pi \cdot \frac{\omega_c}{\omega_0^2}. \tag{12}$$

Unfortunately, making K_D proportional to $1/V_{IN}$ has a drawback. As evident from (11), the frequencies of the two zeros introduced by the PID compensator are not constant, but their product is proportional to V_{IN}. These moving zeros make the control of the converter over the full range of the input voltage extremely difficult. One way to mitigate this variability is to make the coefficient K_P inversely proportional to V_{IN}, that is:

$$K_P = K_I \frac{\omega_{z1} + \omega_{z2}}{\omega_{z1}\omega_{z2}} = K_D \left(\omega_{z1} + \omega_{z2}\right) = \frac{K_{PV}}{V_{IN}}, \tag{13}$$

where K_{PV} is a dimensionless constant. By combining (11) and (13) we obtain:

$$\omega_{z1} + \omega_{z2} = \frac{K_{PV}}{K_{DV}}. \tag{14}$$

Hence, the sum of the two zeros is independent of V_{IN} whereas their product is proportional to V_{IN}. Assuming that the two zeros are real and distinct at a given input voltage, they first move towards each other as V_{IN} is increased, becoming complex conjugate when the following condition is fulfilled:

$$V_{IN} \geq \frac{K_{PV}^2}{4 K_{DV} K_I}. \tag{15}$$

The proposed design strategy starts by placing two real and distinct compensation zeros at the minimum value, $V_{IN_{min}}$, of the input voltage. Denoting the angular frequencies of the zeros at $V_{IN_{min}}$ as ω_{z1_o} and ω_{z2_o}, a conservative choice is $\omega_{z1_o} \simeq \omega_0/3$ and $\omega_{z2_o} \simeq \omega_0$. The constants K_{PV} and K_I are derived from (14) and (11):

$$K_{PV} = K_{DV} \left(\omega_{z1_o} + \omega_{z2_o}\right), \tag{16}$$

$$K_I = \frac{K_{DV}}{V_{IN_{min}}} \omega_{z1_o} \omega_{z2_o}. \tag{17}$$

Finally, the high-frequency pole, $\omega_{hf} = \frac{1}{R_D C_D}$ arising from the derivative path is located in such a way to obtain the desired phase margin:

$$\varphi_m \simeq 90^\circ - \arctan \frac{\omega_c}{\omega_{hf}}, \tag{18}$$

where $\omega_c \gg \omega_0$ is assumed.

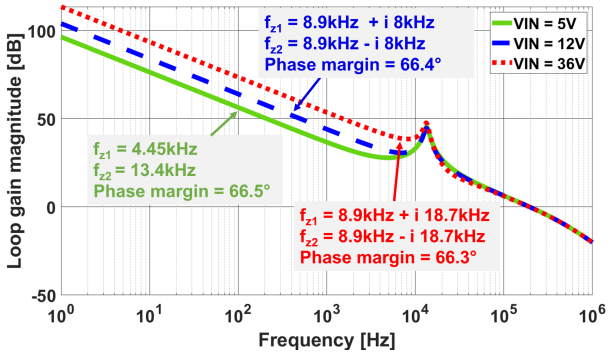

Fig. 2. Bode plot of the loop gain magnitude of a buck converter with the proposed adaptive gain compensation at different input voltage values. The phase margin and the frequency of the zeros for each operation condition are listed.

Table I summarizes the parameters obtained by going through the design procedure previously outlined. With those parameters, the compensation zeros become complex conjugate (cc) for $V_{IN} \simeq 6.4$ V. By further increasing V_{IN}, their angular resonance frequency increases, becoming eventually slightly higher than ω_0. At the same time, however, the damping factor of the cc zero pair reduces, resulting in no or negligible impact on the phase margin. The soundness of the design approach is confirmed by Fig. 2, which shows the Bode diagram of the loop gain magnitude at minimum, medium and maximum values of V_{IN}. A stable crossover frequency (i.e. 200 kHz) and phase margin (i.e. about 66 deg) are achieved by employing the adaptive PID compensator.

The practical implementation of the input voltage dependent K_P and K_D coefficients deserves further attention. Since the CCDLs are driven by transconductors (TCs), as shown in Fig. 1, the simplest approach is to modulate the transconductances G_{mp} and G_{md} by acting on the bias current of the TCs. The small-signal transconductance of a differential TC with MOSFETs operating in strong inversion, can be written as:

$$G_m = \sqrt{K_m I_T}, \tag{19}$$

where K_m is a constant that depends on the technology node and the MOSFET aspect ratio, whereas I_T is the tail bias current. To achieve the desired relationship $G_m \propto 1/V_{IN}$, a bias current given by:

$$I_T = \frac{K_T}{V_{IN}^2} \tag{20}$$

should be generated, where K_T is a constant that depends on the tail transistor.

To simplify the circuit, instead of generating the nonlinear I-V in (20), we can rely on a piecewise-linear approximation by summing two voltage-dependent currents I'_T and I''_T. The first current is linearly dependent on V_{IN}, as

$$I'_T = I_0 - \alpha V_{IN}, \tag{21}$$

where I_0 is a bias current and α is a positive coefficient. The second contribution is a piecewise linear component that can

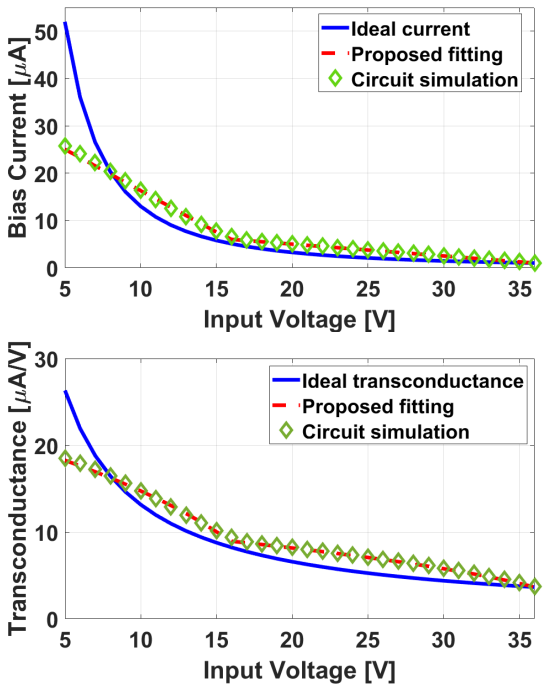

Fig. 3. Transconductor bias current I_T (upper) and proportional transconductance G_{mp} (lower) as a function of V_{IN}: ideal curve (solid line), piecewise linear fitting (dashed line), current from transistor-level simulations (diamonds).

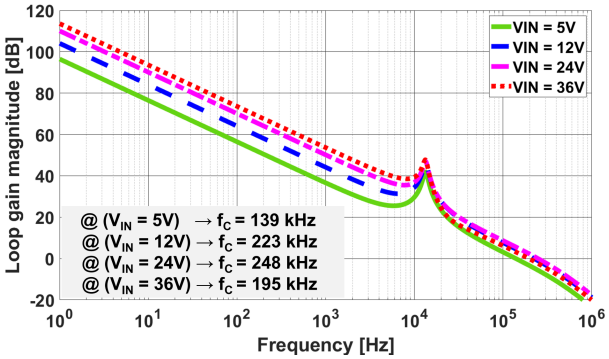

Fig. 4. Bode plot of the loop gain magnitude of a buck converter with the piecewise-linear adaptive gain compensation at different input voltage values. The crossover frequencies for each operation condition are listed.

be written as:

$$I''_T = \begin{cases} I_0 - \beta\,(V_{IN} - \gamma) & \text{if} \quad I''_T > 0 \\ 0 & \text{otherwise} \end{cases} \tag{22}$$

where β and γ are two positive coefficients.

In this design, K_T was set to 1.3 mA V^2, to keep a bias current of the proportional and derivative transconductors higher than 1 μA over the whole V_{IN} range. The values of the constants in the two currents expressions (21) and (22) were set to fit the nonlinear curve while limiting the power dissipation of the current generators, as $I_0 = 10$ μA, $\alpha = 0.25$ μA/V, $\beta = 1.5$ μA/V, and $\gamma = 9.2$ V.

Figure 3 shows the piecewise-linear approximation of the I_T current and the G_{mp} transconductance compared with the desired ones. The dots in the same plots are obtained from

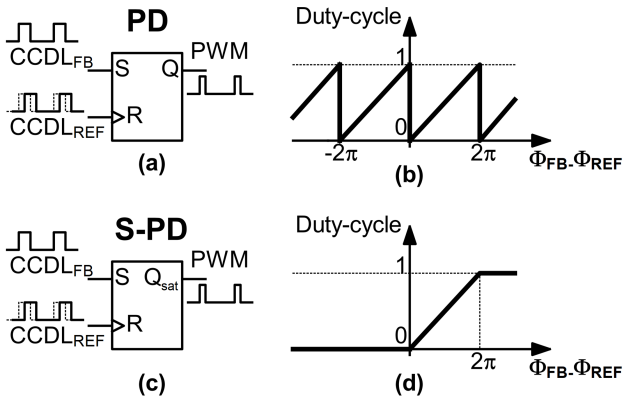

Fig. 5. (a) PD equivalent digital circuit; (b) Transfer function of the PD block. (c) S-PD equivalent digital circuit; (d) Transfer function of the S-PD block.

transistor-level simulations of the implemented circuits, that will be described in details in the following section. The magnitude of the resulting loop gain using the piecewise-linear adaptive gain compensation is shown in Fig. 4. The crossover frequency varies by a factor of 1.8 over the full input voltage range, compared to a variation by a factor of 7.2 resulting from a non-adaptive controller.

To reduce the crossover frequency variation or to apply the concept to a time-based DC/DC converter with a larger input voltage range, the piecewise-linear approximation approach can be further iterated: multiple instances of the bias current generator in (22) (with different slopes) can be added. In the present implementation, to restrain the quiescent current consumption, we decided to limit the I_T current at low V_{IN} values and accept a slight deviation from the nominal crossover frequency.

B. Controlled skip operation

Synchronous buck converters typically operate in CCM. When the average inductor current becomes smaller than half of the peak-to-peak ripple, the instantaneous current reverses for part of the switching period, leading to unwanted power loss. A common solution for increasing power efficiency is the so-called diode emulation [17], which forces the converter to operate in discontinuous conduction mode (DCM) at light loads while maintaining a constant switching frequency. This is achieved by simply turning off the low-side switch of the synchronous converter when the inductor current gets to zero. In DCM, the magnitude of the on-time decreases with the average load current. At light loads, the on-time, T_{ON}, may drop below the minimum value causing the converter to naturally skip some pulses. Although this operation can still guarantee regulation, it is unpredictable and usually responsible for large output voltage ripples. Therefore, a controlled skip operation is preferred to minimize ripple and power consumption, while still providing regulation.

In conventional analog voltage- or current-mode control, the skip operation can be implemented by monitoring the error amplifier output voltage with a skip comparator. In time-based control, the equivalent information has to be directly derived from the PD output. This is obtained by comparing the PD output with a reference on-time. The phase detector is a digital circuit commonly used in phase-locked-loops to generate a signal proportional to the phase difference between the CCDL_{FB} and the CCDL_{REF} signals as shown in Fig. 5-(a). Although the PD correctly operates when the phase difference between the two input signals is between zero and 2π, outside this range the phase wraps around 2π resulting in a non-monotonicity in the PD transfer function, as shown in Fig. 5-(b). When the phase difference between the feedback (Φ_{FB}) and the reference (Φ_{REF}) signals decreases below zero, the PD generates a signal with a duty-cycle close 1. To avoid phase wrapping, the PD is replaced with a saturated-PD (S-PD) logic function that saturates when the phase difference, Φ_{FB}-Φ_{REF}, is smaller than zero or larger than 2π (see Figures 5-(c) and 5-(d)). This logic function is embedded into an asynchronous finite-state machine (AFSM). When the duty-cycle of the S-PD is saturated to 1, the over-current-protection (OCP) prevents the inductor current from increasing indefinitely, thus avoiding circuit failures. When the duty cycle saturates to zero, the AFSM generates a glitch synchronized with the CCDL_{FB} rising edge that is used during the controlled-skip operation. When the S-PD generates a signal with a duration shorter than the target minimum on-time, the AFSM handles the violation events. Figure 6 shows the simplified state diagram of the controlled-skip operation. The relevant timing and schematic diagrams are shown in Fig. 7. When the output of the S-PD (PWM_{S-PD}) changes from zero to one, the AFSM moves to the central state, starting a new charging phase. The high-side MOS turns on (HS $= 1$), and the reset signal goes low (RESET $= 0$) enabling the circuit to generate the SKIPTON pulse of duration $T_{ON,skip}$. The control evolves based on whether the SKIPTON falling edge arrives before or after the S-PD one. In particular, the former condition occurs in the standard PWM operation, while the latter occurs in the controlled-skip operation. During the skip operation, the converter on-time is set to $T_{ON,skip}$, while the output voltage ripple is set by the hysteresis window $(V_{H+} - V_{H-})$ of the skip comparator (whose output is the signal nSKIP in Fig. 7). For this to be true, the charge at the inductor output during the skip operation (Q_{skip}) has to be limited. The worst case scenario in terms of output voltage ripple, occurs when Q_{skip} is equal to the charge flowing in the output capacitance, i.e., when the load current is zero. In this condition $(Q_{skip}/C) < (V_{H+} - V_{H-})$ has to be guaranteed. For a buck converter operating in DCM, Q_{skip} is equal to:

$$Q_{skip} = \frac{T_{ON,skip}^2 V_{IN}\left(V_{IN} - V_{out}\right)}{2LV_{out}}, \tag{23}$$

According to (23), if a constant $T_{ON,skip}$ is selected, the charge would change by more than two orders of magnitude depending on the operating input voltage level.

To overcome this issue, an adaptive $T_{ON,skip}$ value is generated, given by:

$$T_{ON,skip} = \frac{k_\tau}{V_{IN} - V_{out}}, \tag{24}$$

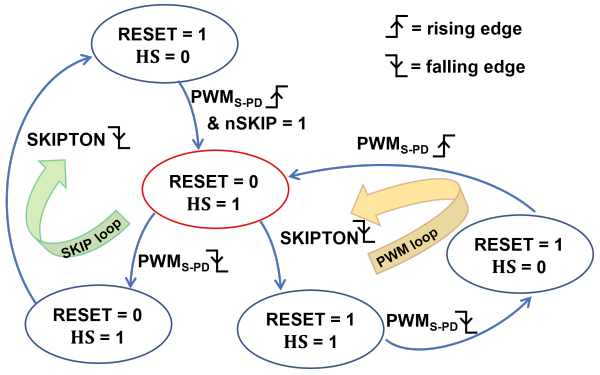

Fig. 6. Simplified state diagram for the controlled-skip operation.

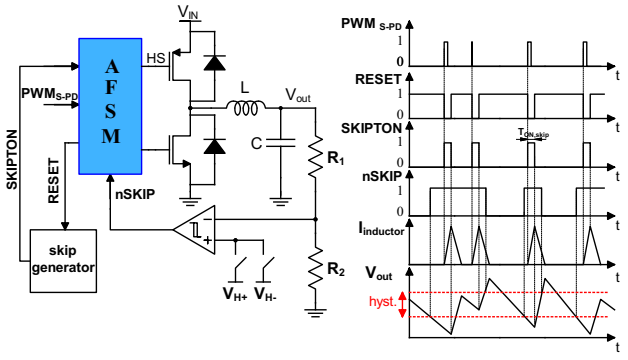

Fig. 7. Simplified circuit schematic and waveforms of the converter during the controlled-skip operation.

where k_τ is a constant expressed in $[s{\cdot}V]$. By replacing (24) into (23) we obtain:

$$Q_{skip} = \frac{k_\tau^2 V_{IN}}{2V_{out}\left(V_{IN} - V_{out}\right)}, \tag{25}$$

which shows a much lower dependence on V_{IN} with respect to (23). During the controlled skip operation, the average pulse frequency, f_{skip}, is a function of the load current i.e., $f_{skip} = I_{load}/Q_{skip}$.

The above discussed logic has a twofold advantage. First, it reduces the switching activity of the converter at light loads, thus improving efficiency. Second, being the time-based control still active during the skip operation, it automatically guarantees a seamless transition between the controlled-skip and the PWM operation, requiring no dedicated analog circuit.

IV. Circuit Design

The simplified block diagram of the implemented buck converter together with the circuit that implements the derivative transconductor with adaptive bias current is illustrated in Fig. 8, where the bias current I_0 is generated by a zero-to-absolute-temperature (ZTAT) reference. The transconductor is implemented using a differential stage whose output node is connected to the control input of the CCDLs. Since just the gain has to be adapted with the input voltage, while keeping the same CCDL bias point, the bias current of the transconductor is canceled out using an additional set of mirror stages. A similar scheme is used for the proportional transconductor, as well. The CCOs and CCDLs are realized as a cascade of standard current starved inverter cells. The circuit implementation is similar to that presented in [9] and [10] and is, thus, omitted.

The circuit schematic of the skip generator is shown in the inset of Fig. 8. As the reset signal goes to zero, the switch is opened and the capacitance C_{on} charged by a current

$$I_{on} = \frac{V_{IN} - V_{out}}{R_{on}} + \frac{V_{ov,on1} - V_{ov,on2}}{R_{on}}, \tag{26}$$

where $V_{ov,on1}$ and $V_{ov,on2}$ are the overdrive voltage of the transistors M_{on1} and M_{on2}. The first term of the sum in (26) emulates the inductor charging phase and the second one is computed neglecting the threshold variation of the transistor due to the body effect and it can be made negligible by design. Under this condition, $T_{ON,skip}$ can be computed as:

$$T_{ON,skip} \simeq \frac{V_{SET}}{V_{IN} - V_{out}} \cdot R_{on} C_{on}. \tag{27}$$

Comparing (27) with (24) we obtain:

$$k_\tau = V_{SET} R_{on} C_{on}. \tag{28}$$

Figure 9 shows the schematic of the circuit generating the tail current of the derivative transconductor, made of the sum of an I'_T current proportional to V_{IN} and an I''_T current proportional to V_{IN} over a limited range and then going to 0. The I'_T term is generated from the circuit section on the left of the schematic diagram. The M_{1a}, M_{1b}, M_{2a} transistors have the same dimensions to have the same reference current

$$I_{M1a} = \frac{V_{IN} - 2V_{GS}}{R_\alpha}, \tag{29}$$

where V_{GS} is the gate-to-source voltage of M_{1a}, M_{1b}, M_{2a}. The current in M_{2b} is the sum of I_{M1a} and the current in the resistance $R_\alpha/2$ connected to its source:

$$\begin{aligned} I_{M2b} =& \frac{V_{IN} - 2V_{GS}}{R_\alpha} + \frac{2V_{GS} - V_{GS2b}}{R_\alpha/2} = \\ =& \frac{V_{IN}}{R_\alpha} + \frac{2(V_{OV} - V_{OV2b})}{R_\alpha} \simeq \alpha V_{IN}\,, \end{aligned} \tag{30}$$

where V_{GS2b} is the gate-to-source voltage of M_{2b}, V_{OV} and V_{OV2b} are the overdrive voltages of M_{1a} and M_{2b}, respectively. The last term in (30), where we neglected the transistor threshold variation induced by the body effect, can be made negligible by design. So, what is left in (30) is a current proportional to V_{IN} with proportionality coefficient $\alpha = 1/R_\alpha$, leading to $R_\alpha = 4\ M\Omega$. Finally, $I'_T = I_0 - \alpha V_{IN}$.

To generate the piecewise-linear current component I''_T given by (22), V_{IN} is first scaled down by a factor of 8 by means of the R_{in1}-R_{in2} voltage divider. This makes the differential P-MOS stage with one input biased at 1.15 V balanced when $V_{IN} = 9.2$ V. The low pass filter network including C_F, R_{in1}, R_{in2} is instead designed to filter unwanted fast-fluctuation in the input voltage while also having a small quiescent current consumption. To this aim the resistances R_{in1}, R_{in2} are selected to keep the quiescent current below

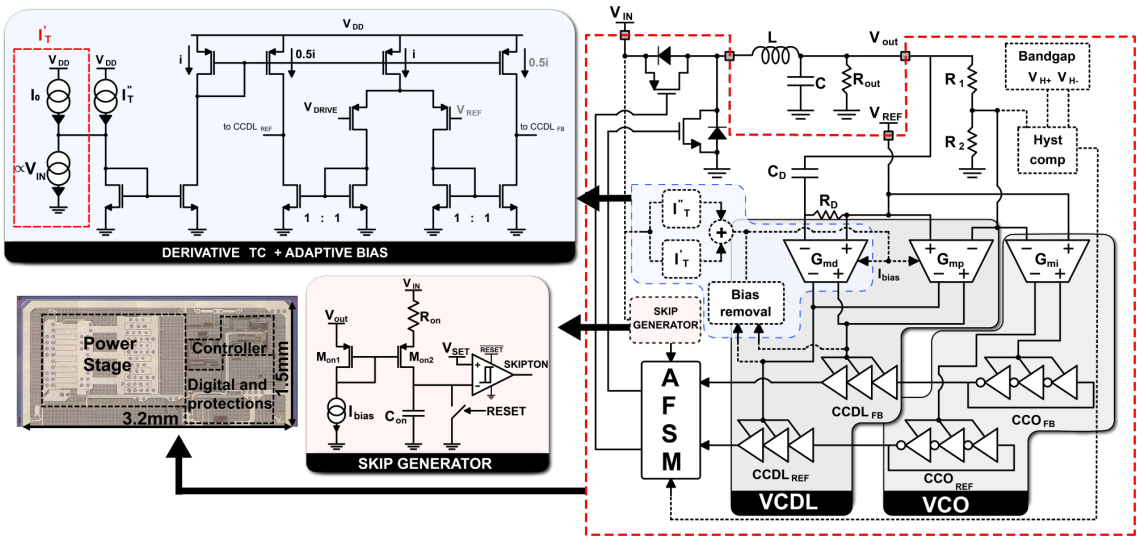

Fig. 8. Block diagram of the implemented buck converter. The three insets show the simplified schematic of the transconductor, the minimum on-time generator, and the die microphotograph.

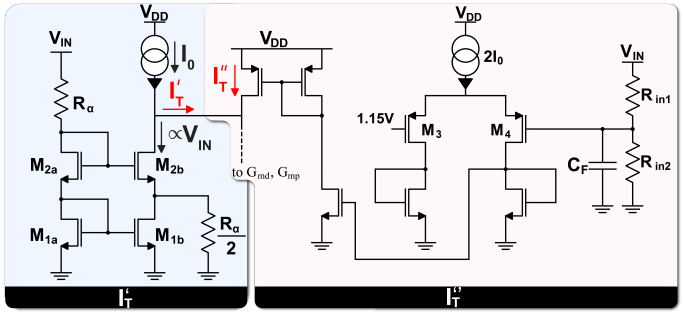

Fig. 9. Simplified circuit schematic of the input-voltage-dependent current generators.

5 μA in the worst case input voltage of 36 V while providing the target 1/8 voltage partition. These requirements are met using R_{in1}=1 MΩ and R_{in2}=7 MΩ. The filter capacitance is selected with a value C_F=1 pF, leading to a frequency of the low-pass-filter pole of f_{lp}=$1/(2\pi C_F R_{in1}//R_{in2})$=182 kHz. Taking into account that the differential stage has tail current $2I_0$ and the two current mirrors are both 1:1, the voltage-to-current DC characteristic of the circuit can be written as

$$I_T'' = I_0 - \frac{I_0}{V_{OV}} \cdot V_{ID} \cdot \sqrt{1 - \left(\frac{V_{ID}/2}{V_{OV}}\right)^2} \qquad (31)$$

where

$$V_{ID} = \left(V_{IN} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}} - 1.15V\right) \qquad (32)$$

is the input differential voltage and V_{OV} is the equilibrium overdrive voltage. If $V_{ID}/2 \ll V_{OV}$, the square root in (31) can be approximated to 1. The resulting I_T'' current is therefore linear over most of the input-voltage range and it is bound between 0 and $2I_0$. By comparing (22) and (31), the following equality must hold:

$$\beta = \frac{R_{in2}}{R_{in1} + R_{in2}} \cdot \frac{I_0}{V_{OV}}, \qquad (33)$$

which allows to derive the overdrive voltage V_{OV} for the desired β value. The total current $(I_T' + I_T'')$ versus V_{IN} obtained from circuit simulation is plotted as diamond dots in Fig. 3.

The AFSM is implemented from the state diagram using an automated design tool [18].

V. Measurement Results

The prototype buck converter incorporating the features described in the above sections was designed in a BCD technology, including CMOS transistors with 0.18-μm minimum feature. The die microphotograph is shown in the bottom inset of Fig. 8, where the main building blocks and the chip dimensions are highlighted. The overall die area is 4.8 mm^2. When the converter is operated in CCM, the total current drained by drivers and control network is 2.4 mA. Among these, the current consumption of the proposed time-based architecture is 470 μA (including the circuit required for the adaptive gain and all the bias networks), while the remaining part is distributed between drivers, digital gates (including AFSM), and auxiliary circuits (over current protection, bandgap, zero current detector, etc.).

Figure 10 shows the efficiency plot of the converter as a function of the load current in CCM operation. Measurements were performed at different input voltages, showing a peak efficiency of 90% at V_{IN} = 5 V. Figure 11 shows the converter efficiency at the minimum and maximum input voltage when the proposed controlled-skip operation is enabled. A logarithmic scale is used for the x-axis to better highlight the efficiency in the light load current range. The efficiency measured at V_{IN} = 5 V and V_{IN} = 36 V with the converter operating in CCM mode is reported for comparison. Thanks to the skip operation, the switching activity of the power stage at light loads is reduced, leading to an increment of power efficiency from 48% to 70% at 5-V input voltage and 10-mA load current. At high loads, the converter operation is automatically moved to a PWM control by the AFSM logic.

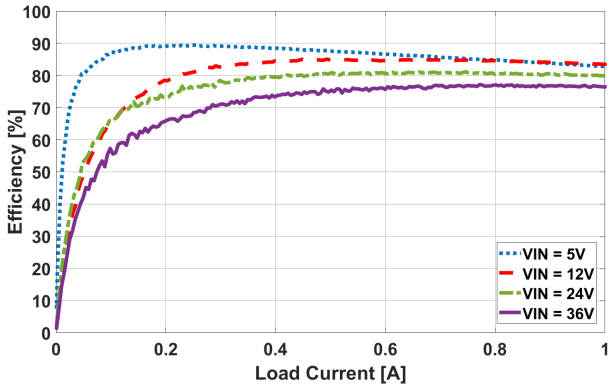

Fig. 10. Measured efficiency as a function of load current for the prototype converter operating in CCM.

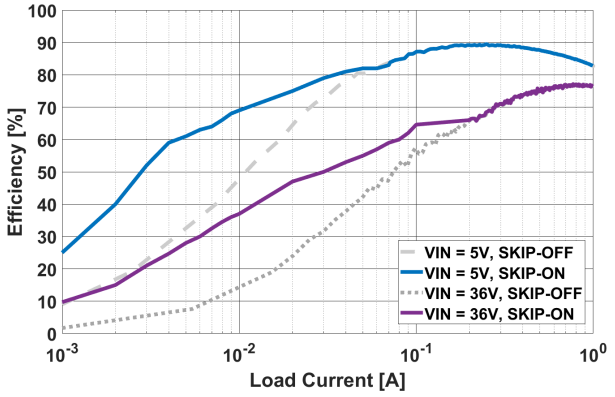

Fig. 11. Comparison of the converter efficiency with controlled-skip operation enabled (solid lines) or disabled (dashed and dotted lines).

The dynamic response of the converter to a 10 V input voltage variation is shown in Fig. 12. The input voltage changes from 10 V to 20 V with a slope of 1 V/20 μs, while the converter is operated in PWM mode with a load current of 0.2 A. The peak-to-peak output voltage variation is limited to 40 mV. The measured load transient response to a 0-1 A current step variation of the prototype converter operating in PWM with an input voltage $V_{IN} = 12$ V is reported in Fig. 13. The peak-to-peak output voltage variation is limited to about

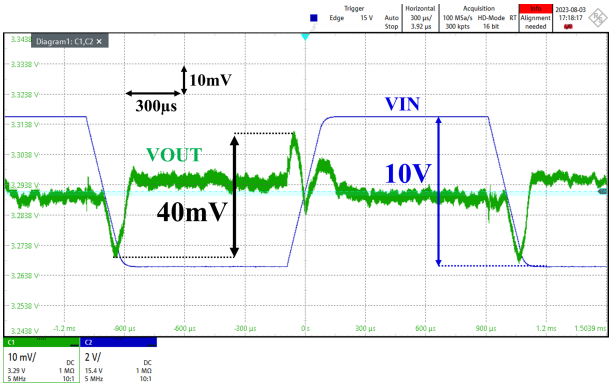

Fig. 12. Measured transient response of the converter to a 10 V to 20 V input voltage variation in 200 μs. The measurement is performed with a load current of 0.2 A

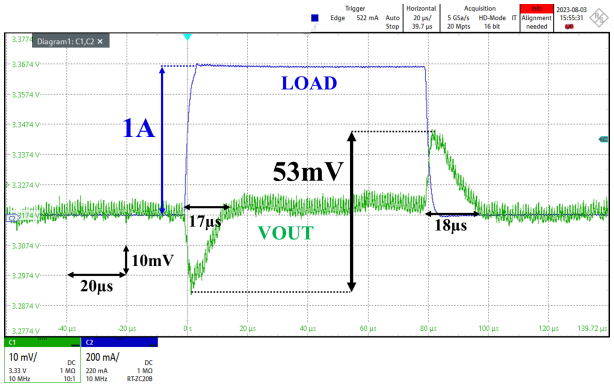

Fig. 13. Measured transient response to a 0-1 A load step variation while the converter operates in CCM. The measurement is obtained for an input voltage of 12 V.

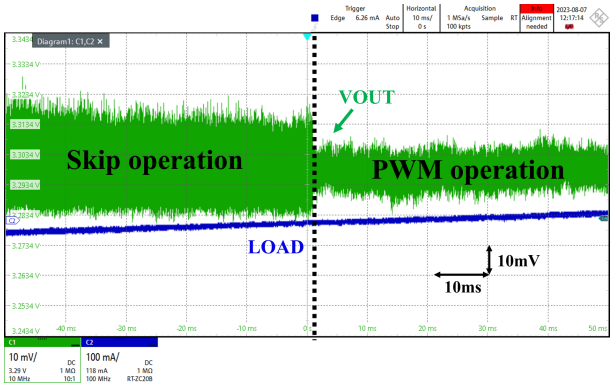

Fig. 14. Measured seamless transition between the low-current controlled-skip operation and the PWM operation. The output voltage does not show a transient response as the converter moves between the two operating modes.

53 mV.

In Fig. 14, the converter load current is varied with a slow ramp while the input voltage is kept at $V_{IN} = 12$ V and the skip operation is enabled. As far as the load current is below about 0.1 A, the converter output is regulated by the skip operation, and the output voltage ripple of 30 mV is determined by the hysteresis of the comparator in Fig. 7. When the current increases, the on-time generated by the

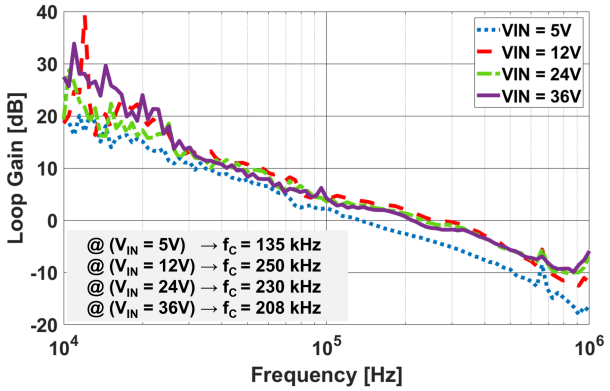

Fig. 15. Measured loop gain magnitude of the prototype buck converter when the adaptive gain compensation is enabled.

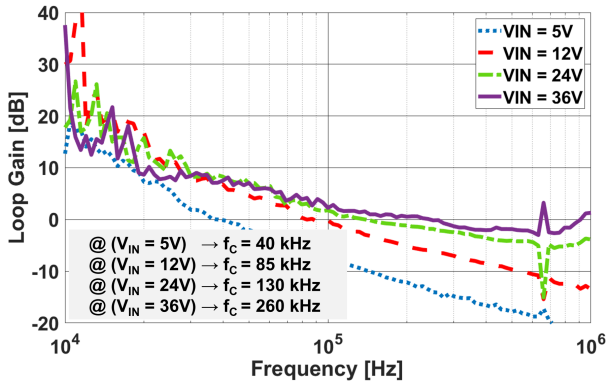

Fig. 16. Measured loop gain magnitude of the prototype buck converter when the adaptive gain compensation is disabled.

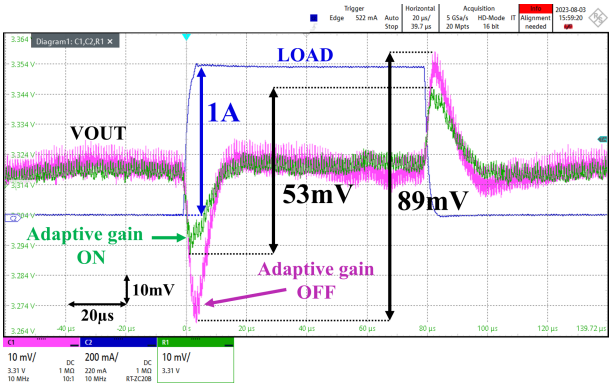

Fig. 17. Measured transient response to a 0-1 A load step variation at $V_{IN} = 12$ V, with the adaptive gain compensation enabled and disabled. The converter is operating in PWM regime.

controller becomes higher than the $T_{ON,skip}$ one. This makes the AFSM switch the control to the time-based PWM mode. The output voltage moves between the two operating points without a significant output voltage transient, demonstrating the effectiveness of the proposed seamless transition.

To assess the proposed adaptive gain compensation technique, the magnitude of the open loop gain was measured by using the methodology reported in [19]. A Picotest-J2101A injection transformer was used to apply a small sinusoidal voltage signal to 40Ω resistance placed in series with the output voltage divider. The loop response was recorded by using a Rohde&Schwarz RTA4004 oscilloscope. The measured loop gain magnitude for different input voltages with and without the proposed adaptive gain compensation is shown in Fig. 15 and Fig. 16, respectively. The comparison highlights how the adaptive gain control reduces the bandwidth variation over the whole operating range. Figure 17 shows the measured transient response to a 0-1 A load step variation at $V_{IN} = 12$ V, with the adaptive gain compensation enabled and disabled. The converter is operating in PWM regime. Thanks to the higher bandwidth provided by the adaptive gain compensation, the peak-to-peak output voltage variation is reduced from 89 mV to 53 mV. As pointed out in Sect. III and demonstrated in the Appendix, the proportional coefficient K_I was kept constant not to degrade the line regulation. Figure 18-(a) shows the DC

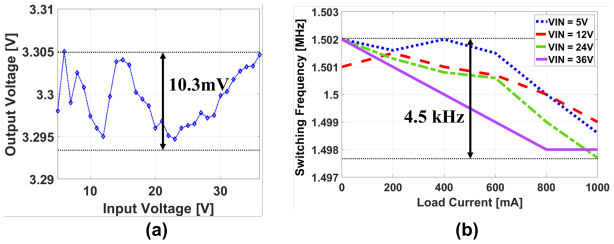

Fig. 18. (a) Measured DC output voltage as a function of the input voltage for PWM operation. The output voltage variation is limited to 10.3 mV in the whole operating range. (b) Measured converter switching frequency as a function of the load current, for different input voltages. The switching frequency variation is only 4.5 kHz in the whole operating range.

output voltage as a function of the input voltage. The excellent line regulation of 0.33 mV/V is obtained, demonstrating the effectiveness of the proposed design methodology. In Fig. 18-(b)), the converter's average switching frequency is measured at different input voltages and different load currents. Since the switching frequency is set by the CCOs bias, which is fixed, it remains stable in all the working conditions. A residual frequency variation of only 4.5kHz (i.e. 0.3% of the nominal switching frequency) was measured over the whole operating range.

Table II shows the performance comparison with state-of-the-art converters. Compared to converters using time-based control, our prototype exhibits the best line regulation of 0.33 mV/V thanks to the novel adaptive gain design methodology. Such a result is achieved despite operating over a much wider input voltage range. The controlled-skip operation provides a significant increase in converter efficiency at light loads which is, however, slightly lower than that obtained with other PFM techniques presented in the literature. This is because the time-based controller must be left active during the LCM operation in order to guarantee a seamless transition between the low-current mode (LCM) and PWM operation. Doing so, it is possible to directly implement the seamless transition algorithm into the AFSM without requiring a dedicated circuit. When compared to converters having similar input voltage and switching frequency, the prototype yields similar peak efficiency and load transient response. To better assess the latter parameter, the figure-of-merit (FOM) proposed in [23] is employed

$$FOM = \frac{\eta_{peak}[\%] \cdot \Delta I_{load}[mA]}{t_{settle}[\mu s] \cdot f_{sw}[MHz] \cdot \Delta V_{out,pkpk}[mV]} \cdot 10^{-2}, \tag{34}$$

where t_{settle} is the average settling time of the transient responses to positive and negative load steps. Among the converters reported in Table II, our prototype shows the best FOM, with the exception of [20], which incorporates an additional dedicated structure specifically designed to enhance the dynamic performance.

VI. Conclusions

When the classical time-based PID control is applied to a buck converter with a wide input range, the loop gain crossover frequency is subject to large variations. Additionally,

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART CONVERTERS

	This work	[9]	[12]	[13]	[10]	[20]	[21]	[22]
Architecture	**Time-based Buck**	Time-based Buck	Time-based Buck	Time-based Buck	Time-based Boost	Analog Buck	Digital Buck	AOT^{+} Buck
Process	**0.18-μm BCD**	0.18-μm CMOS	65-nm CMOS	65-nm CMOS	0.18-μm BCD	0.8-μm BCD	0.18-μm BCD	0.35-μm BCD
Input Voltage [V]	**5-36**	1.8	1.8	1.8	2.5-4.5	10-60	5-48	24
Output Voltage [V]	**3.3**	0.6-1.5	0.5-1.5	0.15-1.69	5	5	5	1.2
f_{SW} [MHz]	**1.5**	11-25	10	10	1.5	1	2	5
L, C [μH, μF]	**4.7, 30**	0.22, 4.7	0.22, 4.7	0.22, 4.7	2.2, 44	20, 40	–, –	0.68, 18
Load Current [A]	**1**	0.6	1	0.6	0.8	0.6	1.3	1.8
Peak Efficiency [%]	**90**	94	90	94.9	96	92.6	90.2	89.8
Adaptive Gain	**yes**	no	no	no	no	no	yes	no
Line Reg. [mV/V]	**0.33**	–	–	27	1.5	0.04	–	–
LCM*	**Pulse-skip**	no	PFM	no	PFM	no	no	no
LCM* efficiency boost @10mA (@CR**)	**24% (0.66)**	–	30% (0.83)	–	34% (1.4)	–	–	–
LCM to PWM Transition	**Automatically guaranteed**	–	Requires dedicated circuit	–	Requires dedicated circuit	–	–	–
Load step [A] $\Delta V_{DW}/\Delta V_{UP}$ [mV] Settling time DW/UP [μs]	**1** **-26/+27** **17/18**	0.5 -60/+65 3.5/3.5	0.4 -40/+40 1.8/1.8	0.48 -100/+110 3.5/3.5	0.3 -60/+58 15/20	0.4 -12.7/+9.3 12.3/7.6	1 -190/+200 24/20	1.8 -23/+37 9.6/8.7
FOM***	**0.65**	0.1	0.25	0.06	0.09	1.69	0.05	0.59

$^{+}$AOT = Adaptive on-time, *LCM = low current mode, **CR = conversion ratio, ***FOM as defined in (34), higher values are better.

the need for large blocking voltages on the power switches increases the gate charge losses, severely limiting the light load efficiency. To overcome these issues, we developed a time-based controller with an adaptive gain compensation and an AFSM-controlled skip operation for the low current mode. The loop crossover frequency is maintained nearly constant over the input-voltage-range by adopting an adaptive PID compensator based on a novel design methodology. The controlled skip operation, using a simple logic and a few analog blocks, increases the light load efficiency and ensures a seamless transition between the operating conditions. Those concepts have been demonstrated in a prototype buck converter for general purpose applications designed in BCD technology. The controlled-skip operation has been shown to boost the efficiency at light loads and the adaptive gain compensation to effectively reduce the crossover frequency variation over the whole input voltage range. The state-of-the-art line regulation for a DC/DC converter with time-based control is obtained thanks to the novel design methodology.

APPENDIX

This appendix discusses the impact of the transconductance G_{mi} of the integral path on the static line regulation of the converter. Similar to the behavior of a phase-locked loop, in the time-based controller the two CCOs reach the same frequency at steady state. From Fig. 1, the latter condition can be written as:

$$[I_{CCO} - \frac{G_{mi}}{2}(NV_{out} - V_{REF})]K_{CCO_{FB}} + \\ - [I_{CCO} + \frac{G_{mi}}{2}(NV_{out} - V_{REF})]K_{CCO_{REF}} = 0, \quad (35)$$

where I_{CCO} is the CCO bias current which is used to set the free-running frequency. In the case of perfectly matched oscillators (same I_{CCO}, same K_{CCO}), the solution of (35) is $NV_{out} = V_{REF}$.

If we instead assume a gain mismatch such that $K_{CCO_{REF}} = K_{CCO}$ and $K_{CCO_{FB}} = K_{CCO} + \Delta K_{CCO}$, (35) can be rewritten as

$$I_{CCO}\Delta K_{CCO} \simeq G_{mi}(NV_{out} - V_{REF})K_{CCO}. \quad (36)$$

Considering the relation between K_I and the integral transconductance in (5a), we can write

$$V_{out} = \frac{V_{REF}}{N} + \frac{I_{CCO}\Delta K_{CCO}}{K_I}, \quad (37)$$

where the last term represents a static regulation error. In practice, because of the differential architecture, any mismatch in the circuit implementing the integral gain is responsible for a static regulation error.

In the case of constant K_I, the static regulation error can be easily trimmed by acting on V_{REF}. Conversely, a variable K_I, such that $K_I = K_{IV}/V_{IN}$ (with constant K_{IV}), would generate an input-voltage dependent regulation error whose relative value (i.e, the static line regulation) is:

$$\frac{\Delta V_{out}}{V_{out}} = \frac{K_{CCO}I_{CCO}}{K_{IV}}\frac{\Delta K_{CCO}}{K_{CCO}}\frac{\Delta V_{IN}}{V_{out}}, \quad (38)$$

By replacing K_I, K_P, and K_D in (9) with parameters inversely proportional to V_{IN}, the zeros of the PID can be designed to perfectly cancel the complex-pole pair, leading to $K_{IV} = 2\pi\omega_c = 7.9$ Mrad/s. Assuming a $\frac{\Delta K_{CCO}}{K_{CCO}} = 1\%$, and remembering that $K_{CCO}I_{CCO} = 2\pi f_{sw}$, a static line regulation of 11.2% would be obtained. This corresponds to an output voltage variation of 270 mV over the input voltage range, which might be unacceptable in many applications.

REFERENCES

[1] R. Redl and J. Sun, "Ripple-Based Control of Switching Regulators—An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2669-2680, Dec. 2009.

[2] Q. ul Ain et al., "A High-Efficiency Fast Transient COT Control DC–DC Buck Converter With Current Reused Current Sensor," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 9521-9535, Aug. 2021.

[3] F. Bizzarri, P. Nora and A. Brambilla, "Stability Boundaries of Wide-Input-Range COT Buck Converters With Ripple Compensation," *IEEE Open Journal of Circuits and Systems*, vol. 3, pp. 15-24, 2022.

[4] J. Zhao, Q. Ye and X. Lai, "A Frequency Stable On-Time Control Buck Converter With Reference and Frequency Compensation Technique Using Low ESR Output Capacitor," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 4, pp. 3536-3545, April 2022.

[5] H. H. Ahmad and B. Bakkaloglu, "A 300mA 14mV-ripple digitally controlled buck converter using frequency domain $\Delta\Sigma$ ADC and hybrid PWM generator," in *Proc. IEEE International Solid-State Circuits Conf.*, 2010, pp. 202-203.

[6] N. Beohar et al., "A Digitally Controlled DC-DC Buck Converter with Automatic Digital PFM to PWM Transition Scheme," in *Proc. IEEE Applied Power Electronics Conf.*, 2021, pp. 517-522.

[7] C. Buccella, C. Cecati and H. Latafat, "Digital Control of Power Converters—A Survey," *IEEE Transactions on Industrial Informatics*, vol. 8, no. 3, pp. 437-447, Aug. 2012.

[8] C. -H. Tsai, C. -H. Yang, J. -H. Shiau and B. -T. Yeh, "Digitally Controlled Switching Converter With Automatic Multimode Switching," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1830-1839, April 2014.

[9] S. J. Kim et al., "High Frequency Buck Converter Design Using Time-Based Control Techniques," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, pp. 990-1001, April 2015.

[10] M. Leoncini, A. Dago, A. Bertolini, A. Gasparini, S. Levantino and M. Ghioni, "A Compact High-Efficiency Boost Converter With Time-Based Control, RHP Zero-Elimination, and Tracking Error Compensation," *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 3100-3113, March 2023.

[11] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski and P. K. Hanumolu, "A 4-Phase 30–70 MHz Switching Frequency Buck Converter Using a Time-Based Compensator," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2814-2824, Dec. 2015.

[12] S. J. Kim, W. Choi, R. Pilawa-Podgurski and P. K. Hanumolu, "A 10-MHz 2–800-mA 0.5–1.5-V 90 % Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 814-824, March 2018.

[13] J. -G. Kang, J. Park, M. -G. Jeong and C. Yoo, "A Time-Domain-Controlled Current-Mode Buck Converter With Wide Output Voltage Range," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 865-873, March 2019.

[14] Road vehicles — Environmental conditions and testing for electrical and electronic equipment — Part 2: Electrical loads. Fifth edition, 07-2023. [Online]. Available: https://www.iso.org/standard/76119.html.

[15] Kaiwei Yao, Yuancheng Ren and F. C. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1454-1461, Nov. 2004.

[16] L. Calderone, L. Pinola and V. Varoli, "Optimal feed-forward compensation for PWM DC/DC converters with 'linear' and 'quadratic' conversion ratio," *IEEE Transactions on Power Electronics*, vol. 7, no. 2, pp. 349-355, April 1992.

[17] Y. Chen, P. Asadi and P. Parto, "Comparative analysis of power stage losses for synchronous Buck converter in Diode Emulation mode vs. Continuous Conduction Mode at light load condition," in *Proc. IEEE Applied Power Electronics Conf.*, 2010, pp. 1578-1583.

[18] S. Dalle Feste et al., "A New Digital Flow for Automotive Robust Design of DC-DC Converters," in *Proc. AEIT International Conference of Electrical and Electronic Technologies for Automotive*, 2019, pp. 1-6.

[19] R. D. Middlebrook, "Measurement of loop gain in feedback systems," *Int. J. Electronics*, Vol. 38, No. 4, pp. 485-512,1975.

[20] X. Yang, H. Cao, and W. Qu, "A 9.3mv load and 5.2mv line transients fast response buck converter with active ramping voltage mode control," in *2020 IEEE Custom Integrated Circuits Conference (CICC)*, 2020, pp. 1–4.

[21] C. Yang, W. Chen, Y. Fan, and P. Gui, "A general-regression-neural-network based 5v-to-48v three-level buck/boost power converter with 40db psrr 90%-efficiency for ssd power loss protection," in *2021 IEEE Custom Integrated Circuits Conference (CICC)*, 2021, pp. 1–2.

[22] X. Ke, J. Sankman and D. Ma, "A 5MHz, 24V-to-1.2V, AO2T current mode buck converter with one-cycle transient response and sensorless current detection for medical meters," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2016, pp. 94-97.

[23] J. -J. Chen, Y. -S. Hwang, Y. Ku, Y. -H. Li and J. -A. Chen, "A Current-Mode-Hysteretic Buck Converter With Constant-Frequency-Controlled and New Active-Current-Sensing Techniques," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 3126-3134, March 2021.

Alessandro Bertolini received his B.S. degree in electronics and communication engineering from Università di Trento, Trento, Italy, in 2012 and in 2016 the M.S. (summa cum laude) in electronics engineering, from Università degli Studi di Brescia, Brescia, Italy. He conducted his master thesis reasearch project at Columbia University in the City of New York, NY, USA, within the Columbia Integrated Systems Laboratory, working on time-based techniques for the design of analog/mixed-signal ICs with ultra-reduced supply. In 2017, he joined STMicroelectronics in Milan, Italy, in a R&D team where he is currently senior analog IC design engineer, developing custom power-management ICs and complex application specific DC-DC converters. In addition, his interests are in RF/mm-Wave IC design, SERDES, PLL, microwave engineering, time-based processing circuits and precision analog circuit techniques.

Mauro Leoncini received the M.S. degree (summa cum laude) and Ph.D degree in electronics engineering from the Politecnico di Milano, Milan, Italy, in 2016 and 2021, respectively. He was winner of a research grant with the Politecnico di Milano on the design of low-power, low-noise electronics for MEMS gyroscopes. He is currently Research Assistant with the Politecnico di Milano where is focusing on the design of low-power/high-frequency time-based control for integrated DC/DC converters and high efficiency controllers in resonant switched capacitor converters.

Paolo Melillo received the B.S. and the M.S. degrees in electronic engineering from Politecnico di Milano, Milan, Italy, in 2018 and 2020, respectively, where he is currently a Ph.D. candidate in electronic engineering. His current research interests include time-based techniques and low-quiescent control for integrated DC-DC converters.

Alessandro Gasparini received the B.S. and the M.S. degrees in electrical engineering from Politecnico di Milano, Italy in 2007. He is design manager at STMicroelectronics. His main activity is related to the design of high performance DC-DC, complex PMIC like wireless charger and battery charger. He is author/co-author of more than 20 patents related to power electronics and analog mixed signal circuit design.

Salvatore Levantino (Senior Member, IEEE) received the Laurea degree (cum laude) and the Ph.D. degree in electrical engineering from the Politecnico di Milano, Milan, Italy, in 1998 and 2001, respectively. From 2000 to 2002, he was a Consultant with Bell Labs, Lucent Technologies, Murray Hill, NJ, USA. Since 2005, he has been with the Politecnico di Milano, where he is currently a Full Professor of electrical engineering. He has coauthored over 150 scientific articles and Integrated Frequency Synthesizers for Wireless Systems (Cambridge University Press, 2007). He holds 9 patents. His research interests include wireless transceivers, frequency synthesizers, data converters and power converters. He has been a member of the Steering and the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium and a TPC Member of the International Solid-State Circuits Conference (ISSCC) and the European Solid-State Circuits Conference (ESSCIRC). He was a co-recipient of the Best Paper Award of the 2018 International Symposium on Circuits and Systems (ISCAS). He was a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (2016 and 2022), and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS from 2014 to 2015 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 2012 to 2013. From 2018 to 2019, he was an IEEE SSCS Distinguished Lecturer.

Massimo Ghioni (M'90-SM'08) received the Laurea degree summa cum laude in Nuclear Engineering from the Politecnico di Milano, Italy in 1987. In 1990 he joined the Department of Electronics, Information Science, and Bioengineering - Politecnico di Milano, where he has been full professor of electronics since 2000. In 1992, he was visiting scientist at the IBM T.J. Watson Research Center, Yorktown Heights, NY. His current research interests include new topologies and control systems for high efficiency, high power density integrated DC-DC converters. He has co-authored over 240 papers in international journals and conferences and holds 8 U.S. patents. In 2004, he co-founded the Micro Photon Devices (MPD), a spin-off company of the Politecnico di Milano specialized in manufacturing photon counting and timing modules. Massimo Ghioni received the IEEE Transactions Prize Paper Award from the IEEE Power Engineering Society in 2004.