0.02 °/h, 0.004 °/√h, 6.3 mA NEMS gyroscope with integrated circuit

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***Abstract*—This work introduces a system formed by an integrated circuit and a micro-machined piezoresistive gyroscope, with navigation grade performance. After discussing the specifications in terms of maximum allowed electronic noise, so not to worsen the thermo-mechanical noise limits, three different front-end topologies are analysed, and the current-feedback instrumentation amplifier is chosen as the optimal solution in terms of noise and current consumption. After coupling to a gyroscope based on nano-gauges, the system demonstrates 200 dps full-scale, 0.02 °/h stability and 0.004 °/√h angle random walk, confirming navigation-grade performance at a current consumption well below 10 mA and an overall power consumption below 40 mW.**

***Index Terms*—Current-feedback instrumentation amplifier, inertial navigation instrumentation, NEMS gyroscopes.**

I. Introduction

GYROSCOPES based on microelectromechanical system (MEMS) technologies have revolutionized several angular rate measurement applications in the past decade [1]. So far, most of these devices were capable to reach consumer or automotive grade performance [2], [3], and only a few of them were able to demonstrate the navigation-grade [4], [5], which requires ultra-low noise (below $0.01\,°/\sqrt{\mathrm{h}}$) and long-term stability (below $0.1\,°/\mathrm{h}$ after up to $1\mathrm{h}$ navigation). Navigation-grade instrumentation based on MEMS gyroscopes would boost their use in several industrial fields, including augmented/virtual reality, autonomous driving, drones, cube satellites, and aerospace, marine and drilling applications. Compactness would also allow a redundancy [6] that other navigation-grade gyroscopes based on bulky technologies (hemispherical resonators or fiber-optic gyroscopes [7]) cannot reach.

In this context, it is fundamental to miniaturize not only the sensor, but the whole system, including the electronics, and possibly to keep the power consumption below $100\,\mathrm{mW}$ to avoid excessive heat generation, which may itself impact on long-term stability. However, works demonstrating miniaturized gyroscopes for navigation-grade performance were, to the best of the authors' knowledge, always exploiting board-level circuits formed by off-the-shelf ultra-low-noise but power-hungry analog components [5], [8], and digital processors like field programmable gate arrays [4].

In this work navigation-grade performance are shown for the first time for an instrument including a yaw MEMS gyroscope and an application-specific integrated circuit (ASIC). The two silicon chips are stacked one another, wire bonded, and fit within $(4 \times 4 \times 2)\,\mathrm{mm}^3$; overall, they draw less than $7\,\mathrm{mA}$ ($1.8\,\mathrm{mA}$ for the MEMS die and $4.5\,\mathrm{mA}$ for the ASIC die), on a $3.6\,\mathrm{V}$ supply. Such results are obtained using a MEMS process featuring piezoresistive NEMS gauges [9] and a current-feedback instrumentation amplifier (CFIA) without source degeneration resistor to minimize noise and with a dedicated offset compensation circuit to enhance stability and preserve the full-scale. Such modifications to the CFIA topology and its use with MEMS gyroscopes are, to the authors' knowledge, introduced for the first time. Two identical CFIAs are used to measure both drive and sense motion of the MEMS structure, which guarantees an optimal rejection of common-mode drifts. Additionally, this minimizes the phase difference between self-sustained drive-mode and modulated sense-mode signals, yielding an optimal phase for the demodulation reference, relevant for quadrature error rejection and improved stability.

In-operation, the system matches the noise ($0.004\,°/\sqrt{\mathrm{h}}$) and stability ($0.02\,°/\mathrm{h}$) requirements for navigation-grade, with a 3-fold reduction in supply voltage, a 20-fold reduction in current consumption, and thus, overall, a 60-fold reduction in power consumption with respect to former implementations based on board level circuits, yielding the most advanced development as of today towards navigation-grade miniaturized gyroscopes at sub 40-mW consumption.

The following sections present the gyroscope and electronic design, with particular focus on the analog front-end, as well as theoretical performances for scale-factor, noise and stability and the related measurements.

II. Gyroscope and Electronics Design

A. Gyroscope Architecture

The presented gyroscope is fabricated in the M&NEMS process [10], featuring a $20\,\mu\mathrm{m}$ MEMS structural layer thickness, and a $250\,\mathrm{nm}$ NEMS layer for piezoresistive sensing with high stress concentration. Fig.1 shows a microscope image of the device, having a total footprint of $(1.45 \times \ 0.91)\,\mathrm{mm}^2$. This sensor, already disclosed in [9], is operated via amplitude-modulated energy transfer between drive and sense modes (frequencies around $25\,\mathrm{kHz}$) through the Coriolis coupling. Thanks to the piezoresistive sensing, ultra-low noise can be achieved even in mode-split configuration, with a nominal difference between drive and sense modes of few hundred Hz. Drive forcing is based on a push-pull, comb-finger electrostatic actuation. NEMS

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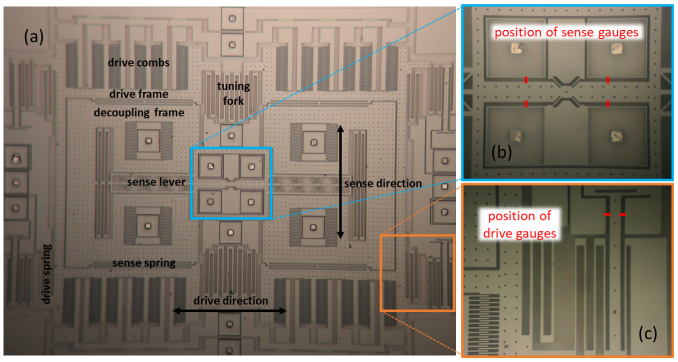

Fig. 1. Microscope image of the $(1.45 \times 0.91)\mathrm{mm}^2$ M&NEMS gyroscope.

TABLE I
NOMINAL GYROSCOPE PARAMETERS

Parameter	Symbol	Value
Mode split value	$\Delta\omega$	$2\pi 200\,\mathrm{Hz}$
Operating frequency	ω_d	$2\pi 25\,\mathrm{kHz}$
Drive quality factor	Q_d	25000-50000
Gauge factor	GF	50
Rotor voltage	V_{rot}	0 V
Actuation voltage	V_{act}	0-600 mV

piezoresistive readout is used for both drive and sense motion [10]. The doubly decoupled structure features a drive frame, a Coriolis decoupling frame, accommodating specific electrodes for electromechanical quadrature compensation, and a sense lever. In operation, the displacement for drive oscillation is set to $9\,\mu\mathrm{m}$. The decoupling mass, rigidly dragged by the drive frame, in presence of an angular rate Ω is sensitive to the Coriolis acceleration, which causes its displacement along the sense mode. Both drive and sense motions are transferred to piezoresistive NEMS gauges via properly sized lever systems.

Gyroscopes based on piezoresistive NEMS sensing have shown advantages with respect to the conventional capacitive counterpart [11], such as:

- negligible effects from capacitive parasitic couplings, and from the related unavoidable drifts [12];
- small footprint of the sensing element, allowing large mass for the same footprint, and more space for quadrature electrodes;
- low-voltage operation with grounded rotor, avoiding charge-pump noise and further reducing possible parasitic, motion-induced, capacitive charge couplings;
- identical sensing scheme and front-end sizing for drive and sense, guaranteeing, under amplitude-controlled drive motion, a self-compensation of common-mode drifts of NEMS resistance, piezoresistive factor, and bridge voltage [9]. Under this condition, the scale factor SF from input rate to resistive bridge output is expressed as:

$$SF = V_{ref}/\Delta\omega \tag{1}$$

where V_{ref} is a circuit reference voltage and $\Delta\omega$ is the split between the two modes.

Anyway, a coupling between drive motion and sense motion, not induced by the Coriolis force but rather by spurious mechanical couplings between the modes, is always present in gyroscopes [11]. Its phase is in quadrature with respect to angular-rate-induced signals. As such mechanical couplings may drift in temperature or under package stresses, an accurate demodulation reference is fundamental to prevent quadrature leakage and associated drift into the system output.

Such NEMS-based gyroscopes have shown in previous works very promising performances towards miniaturized navigation-grade rate sensors, for what concerns noise and stability [9], even in operation and under temperature sweeps [13]. However, such results were obtained with discrete electronics. This work describes the development of a dedicated ASIC and confirms the obtained performances, in the context of further advancements towards the overall system miniaturization and reduction of power consumption.

Table I shows the nominal gyroscope parameters. For more sensor details, the reader is redirected to the referenced works.

B. Analog Front-End Design Options

The ASIC is fabricated in the HCMOS9LP technology by *STMicroelectronics*. For analog circuits, thick-oxide transistors with minimum channel length of $0.35\,\mu\mathrm{m}$, and rated for a maximum voltage of $3.6\,\mathrm{V}$ are chosen, so to accommodate a large dynamic range at high sensitivity. As detailed in the next section, the IC embeds typical blocks of an AM gyroscope but readapted for NEMS gauge based devices and optimized for stability:

1) the drive loop, needed to self-sustain the oscillation along the drive axis, from NEMS piezoresistive front-end to push-pull actuation, and to provide the two demodulation references;
2) the automatic gain control loop (AGC), which regulates and stabilizes the drive oscillation amplitude x_D through a reference voltage V_{ref};
3) the sense chain, which exploits the same NEMS piezoresistive front-end as for the drive readout to minimize the demodulation phase error [14] and maximize stability;
4) a bandgap current reference, needed to provide biasing to the active stages and optimized towards optimal stability against temperature;

The consumption of the chip is $4.5\,\mathrm{mA}$ at ambient temperature. The current injected in the NEMS gauges is $1.8\,\mathrm{mA}$ ($450\,\mu\mathrm{A}$ per gauge). The total consumption is thus $6.3\,\mathrm{mA}$. The system is completed by a digital demodulator and a quadrature compensation loop (AQC), which are currently implemented off chip. As the development of a further version of the ASIC which includes these stages is ongoing, their estimated consumption is known to be less than $1.5\,\mathrm{mA}$, leaving the entire consumption of such a system well below $10\,\mathrm{mA}$.

The analysis of the IC initially focuses on the choice of the front-end stage, which is the most demanding in terms of noise specifications and thus of current consumption. The stage is the same for both drive-loop motion and sense motion detection. A comparison between three different architectures for the differential NEMS gauge readout is initially presented, highlighting advantages and drawbacks, before focusing on the final choice of a current-feedback instrumentation amplifier (CFIA) as the analog front-end of the circuit. Such a comparison is considered interesting for the readers, as the first two solutions, used so far in the literature for NEMS-based gyroscopes, do not represent the optimal solution.

The aim for the analog front-end is to achieve an input referred noise of the electronics lower than the sum of the one introduced by the resistive gauges with resistance value $R_g = 2.4\,\mathrm{k\Omega}$:

$$S_{v,NG} = 4k_BTR_g = (6.3\,\mathrm{nV}/\sqrt{\mathrm{Hz}})^2 \tag{2}$$

(k_B and T are the Boltzmann constant and absolute temperature), and of the thermo-mechanical one, referred to the analog sense chain input:

$$S_{v,TM} = 4k_BTb_s \cdot \alpha_s^2 = (8.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}})^2 \tag{3}$$

(b_s indicates the damping coefficient and α_s represents the transduction from a force acting on the sense mass to the differential voltage variation at the bridge output, $\alpha_s \propto GF/\Delta\omega$). When referring, through the scale factor SF, this combined noise in terms of input angular rate, the value corresponds to navigation-grade requirements of about 0.005 $^\circ/\sqrt{\mathrm{h}}$. Note that the noise densities above shall be obtained around the drive carrier frequency at 25 kHz: in this scenario, 1/f noise from the NEMS resistance is negligible [15]. Conversely, attention shall be paid on electronic 1/f noise, as discussed later. At the same time, other parameters such as the ouput dynamic range, common-mode rejection ratio (CMRR) and current consumption shall be optimized when sizing the front-end.

The first analysed topology is a pseudo-differential amplifier [16], that embeds the sensing gauges directly in its first stage, thus avoiding the use of a Wheatstone bridge and reducing the power consumption (Fig.2a). The working principle is based on the variation, induced by the resistive changes, of the differential signal at the input nodes V_{A+}, V_{B+}. This is copied through the feedback to nodes V_{A-}, V_{B-}, and is amplified to the differential output $V_{out,A}, V_{out,B}$ by an ideal gain within the desired frequency range of $2C_1/C_f$ (see [16] for details). The circuit has the clear advantage of using the input transistors current to bias also the sensing gauges. The main limitation of this architecture, however, can be easily highlighted with a noise analysis. The noise contribution of each transistor can be input-referred and the overall noise can be compared to the gauge noise:

$$S_{v,eq} = S_{R_g} + S_{v,M1} + \frac{\sum_{j=1}^{5} S_{i,Mj}}{\left(\frac{g_{m1}}{(1+g_{m1}R_g)}\right)^2} \tag{4}$$

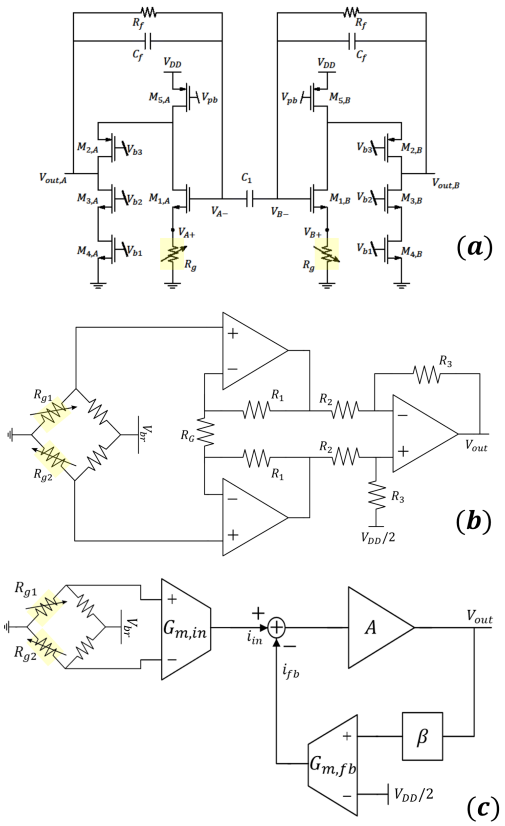

Fig. 2. Analog front-end topologies analyzed for this work: **(a)** pseudo-differential amplifier, **(b)** instrumentation amplifier and **(c)** current feedback instrumentation amplifier, the final choice for the ASIC design.

The contribution of transistors M2, M3 and M4 can be made negligible, since their bias current is at least one order of magnitude less than the one flowing into the first branch. The voltage noise introduced by M1 can also be made lower than the target one, by acting on its overdrive voltage. Yet the main limitation comes from transistor M5: as a matter of facts, its input referred noise can be expressed proportionally to the transistor parameters and the current flowing into the gauge:

$$S_{v,eq,M5} = 4k_BT\gamma \cdot \frac{2(I_g + I_{M2})}{V_{ov,M5}} \cdot \left(\frac{V_{ov,M1}}{2I_g} + R_g\right)^2 \tag{5}$$

which highlights how, once the gauge current is chosen, there is no way to reduce the noise of the stage any further (the excess noise factor $\gamma = 2/3$ accounts for the transistor saturation regime). Since the maximum current through the gauges is limited by the technology to approximately $500\,\mu\mathrm{A}$, the minimum achievable input referred noise is set at $30\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. While being very interesting for low power applications, this topology does not meet noise requirements for high-end applications. Its design was thus discarded.

The second studied topology for the front-end is the well-known instrumentation amplifier (INA) [17], shown in Fig.2b. Here the gauges are biased by a voltage V_{br} in a Wheatstone bridge configuration, whose differential output is connected to

the inputs of the INA. The input referred noise of the amplifier can be expressed as:

$$S_{v,in} = S_{R_G} + 2 \cdot S_{OTA} \tag{6}$$

Therefore, the sizing of the gain resistance R_G and of the input amplifiers must be optimized to obtain an overall noise lower than the target. Given the biasing voltage for the bridge of $2.1\,\mathrm{V}$, which approximately corresponds to the maximum gauge current, the needed gain to exploit the whole output dynamics is 21.5. This can be obtained with $R_G = 586\,\Omega$, $R_1 = R_2 = 6.125\,\mathrm{k}\Omega$ and $R_1 = R_2 = 12.25\,\mathrm{k}\Omega$. The three amplifiers were thus designed, in a 2-stage, pMOS-input, operational transconductance amplifiers (OTAs) configuration [18], with an overall power consumption of $650\,\mu\mathrm{A}$ each, $2/3$ drawn by the input pair in order to reduce the noise level, while the remaining part is used by the output stage to properly bias the feedback resistances in presence of maximum output swing. With such an optimized design, the overall noise turns out to be $\approx 8.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, slightly larger than the Johnson noise of the nano resistors. This is, in principle, in line with the target requirements. It is possible to reduce the noise contribution coming from the input OTAs, but the price to pay is a larger consumption, which would exceed the mentioned IC target.

A third option consists in reducing the number of noise sources of the front-end circuit itself: the last analysed architecture, the current-feedback instrumentation amplifier (CFIA) is investigated for this reason.

A CFIA is a front-end circuit based on a negative feedback which closes with a current summing node, as shown in the block scheme reported in Fig. 2c. It is formed by an input and a feedback transconductance amplifiers, with gain $G_{m,in}$ and $G_{m,fb}$, a high gain block A and a feedback network β, typically a resistive partition. The error signal of this high-loop-gain negative feedback is represented by the difference of the two output currents of the transconductance amplifiers. It is easy to demonstrate that, considering R_{sink} the resistors connected to the current summing node:

$$\begin{aligned} V_{out} &= A \cdot R_{sink} \cdot (i_{in} - i_{fb}) = \\ &= A \cdot R_{sink} \cdot (V_{in} G_{m,in} - V_{out} \beta G_{m,fb}) \end{aligned} \tag{7}$$

$$G_{CFIA} = \frac{G_{m,in} R_{sink} \cdot A}{(1 + R_{sink} \cdot A \beta G_{m,fb})} \approx \frac{G_{m,in}}{G_{m,fb}} \cdot \frac{1}{\beta} \tag{8}$$

With respect to the previously described INA, the first advantage of this topology lies on the fact that there is no need for an output stage for the two input and feedback transconductance amplifiers, thus reducing the power consumption or using the same current budget in the input transistor pairs only, thus lowering their noise contribution. In the literature, two types of CFIA are discussed [17]: direct feedback CFIA and indirect feedback CFIA. A preliminary analysis of the first type showed that it is not suited for this work due to the reduced input dynamics, given by the MOSFET stacking of the two transconductance amplifiers, and its intrinsic linearity error [19].

The working principle of the indirect feedback CFIA topology [20], [21], whose transistor level schematic is shown in Fig.3, is here briefly reported.

The input pair, composed by transitors M_1 and M_2, is unbalanced by the input voltage signal V_{in} coming from the Wheatstone bridge and it generates a current i_{in} that flows into the two R_{sink} resistances. Therefore, a signal is created at the input of the high-gain amplifier A, that creates a voltage difference across the gain resistance R_4. This signal is then read by the feedback transconductance pair which in turn generates a current $i_{fb} = -i_{in}$, thus forcing all the current of the input pair to re-circulate into M_3 and M_4. Overall, considering the input and feedback transconductance amplifier to be identical, the negative feedback equals the current in the two differential pairs, so copying the input voltage across the resistance R_4. The ideal gain of the stage is thus:

$$G_{CFIA} = \frac{G_{m,in}}{G_{m,fb}} \cdot \left(1 + \frac{R_3}{R_4}\right) = \left(1 + \frac{R_3}{R_4}\right) \tag{9}$$

with $G_{m,in} = G_{m,fb} = \frac{g_{m1}}{2} = \frac{g_{m3}}{2}$.

With respect to implementations already presented in the literature [17], [22], in the implementation proposed in this work, at the cost of a slight worsening in part-to-part repeatability, there are no source degeneration resistors between the sources of the input transistors and the tail generator. For low-noise applications, this avoids that the high current needed for the input and feedback transistors creates a voltage drop across the degeneration resistances, limiting the input common-mode. Additionally, this solution avoids introducing additional resistive noise, comparable to the input pair one. Therefore, it was decided to completely remove this additional noise source.

The input differential pair are chosen to be pMOS transistors thanks to their low $\frac{1}{f}$ noise. The amplification stage is a two-stage OTA, featuring pMOS transistors input and a common source with active load, to maximize output dynamics and linearity, as a second stage.

The input referred noise analysis is now presented. The noise from transistors M_1, M_2, M_3, M_4 contribute directly to the input referred noise, as well as the one from the gain resistance R_4. The other contributions can be calculated by considering the open-loop transfer function from input to output. Thus, the input referred noise results:

$$\begin{aligned} S_{v,in} &= 4S_{M1} + S_{R4} + S_{R3} + S_{R_sink} + S_{OTA} \\ &= 4\left(\frac{4k_BT\gamma}{g_{m1}} + S_{1/f}\right) + 4k_BTR_4 + \frac{4k_BTR_3}{G_{CFIA}^2} + \\ &+ \frac{4k_BT}{R_{sink}}\left(\frac{1}{g_{m1}}\right)^2 + S_{v,in,OTA}\left(\frac{1}{g_{m1}R_{sink}}\right)^2 \\ &\approx 4\left(\frac{4k_BT\gamma}{g_{m1}} + S_{1/f}\right) + 4k_BTR_4 \end{aligned} \tag{10}$$

The noise of the OTA is made negligible through a proper sizing, and the contributions from R_3 and R_{sink} can be neglected. Note that each term of Eq. 10 can be lowered by increasing the current in the input and feedback pairs, except

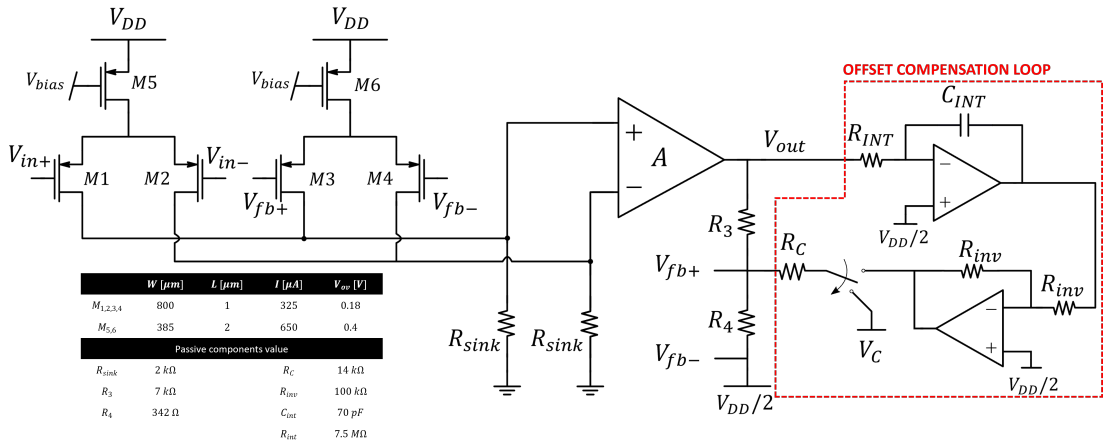

Fig. 3. Transistor level schematic of the designed CFIA. With respect to solutions from the literature there are no source degeneration resistances for transistors $M_{1,2,3,4}$ and the offset compensation circuit (both in closed-loop and open-loop approach) is shown on the right part of the image.

for R_3 and R_4. Here, it is worth to highlight one further advantage of the CFIA with respect to the INA described before: in the latter, the input OTAs noise is determined also by the four transistors used as active loads in the first stage, while in the CFIA they are replaced by the two R_{sink} resistors, thus lowering the noise sources. Also, note that the $1/f$ noise of the differential pairs is lowered by a proper sizing and made a factor 4 lower than their white noise at 25 kHz. This implies that no chopping techniques are needed at the current operating frequencies, with the used IC technology and for the proposed amplifier design.

With the proposed sizing (see the inset of Fig.3) a noise level of $5.2\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ is reached, with a total current consumption of $1.65\,\mathrm{mA}$ and a nominal gain of 21.

The designed CFIA features a selectable gain and offset compensation, implemented both in an open-loop and a closed-loop solution. The former is a useful degree of freedom to test devices of the same family, but with different electromechanical gain. The selectable gain is implemented by connecting in parallel a multiplicity of identical resistors for the gain resistance R_4, in particular the gain values were chosen to be equal to 12.67, 21.42, 36 and 44.75. The higher the device sensitivity, the lower the gain needed, so to avoid saturation of the front-end.

The offset compensation feature, which can be operated as a one-time trimming or in closed-loop mode, is mandatory to avoid any limitation of the output dynamic of the front-end [23]. Indeed, the resistance values of the gauges, arising from a micro-machining process (etching) rather than on a pure CMOS process (doping implant) present a statistical mismatch with a measured $\pm 3\sigma$ value of ΔR_{os} as large as $170\,\Omega$ ($7\,\%$ of the nominal resistance $R_{ng} = 2.4\,\mathrm{k}\Omega$), which, in turn, corresponds to an input voltage difference of:

$$\Delta V_{in} = \frac{V_{br}}{2} \cdot \frac{\Delta R_{os}}{2R_{ng}} \tag{11}$$

With typical values for the stage gain and bridge voltage, the output voltage contribution from the bridge offset is $0.9\,\mathrm{V}$, i.e. half of the output dynamics.

The proposed solution, shown in the right part of Fig.3 implements an automatic offset compensation loop: it consists in connecting a resistance R_C at the node between resistors R_3 and R_4 and to properly bias it with a voltage V_C to create an output voltage contribution that counteract to the one given by the gauge offset, which is measured by averaging the output through an integrator.

$$V_{out} = \frac{V_{DD}}{2} + (V_{in} + V_{os})\left(1 + \frac{R_3}{R_4 \parallel R_C}\right) + \\ + \left(\frac{V_{DD}}{2} - V_C\right)\frac{R_3}{R_C} \tag{12}$$

The value of R_C is nominally $14\,\mathrm{k}\Omega$, a value chosen as a compromise between the maximum possible swing between V_C and $V_{DD}/2$, i.e. $1.8\,\mathrm{V}$, and the target offset to compensate. Note that it is mandatory to have $R_C \gg R_4$ to avoid changes in the stage gain, so the added noise is negligible. While the offset compensation strategy is conceptually similar to conventional INAs, its implementation here exploits a current-based approach and is proposed for the first time, to the authors' knowledge for a CFIA.

C. System Design

This section discusses the remaining blocks of the system, schematically shown in Fig.4, where the CFIA are schematized as 4-input blocks. With respect to most of integrated drive-loop design, we note that here the front-end output is single-ended and not differential, and the loop shall be thus designed accordingly. The drive loop is completed by a phase shifting block (90D), needed to fulfill the Barkhausen condition on phase, followed by a gain stage that saturates the sinusoidal signal, providing the nonlinear block that sets the gain to unity in operation, and a H-bridge used as the actuation stage to bias the drive comb-fingers. The 90D-stage features a zero in the origin and two poles at low frequency to introduce a $90°$ shift to the signal coming from the drive CFIA, and is implemented as a bandpass filter, with the following transfer function:

$$G_{90D} = \frac{-sC_{90D,1}R_{90D,2}}{(1 + sR_{90D,1}C_{90D,1})\,(1 + sR_{90D,2}C_{90D,2})} \tag{13}$$

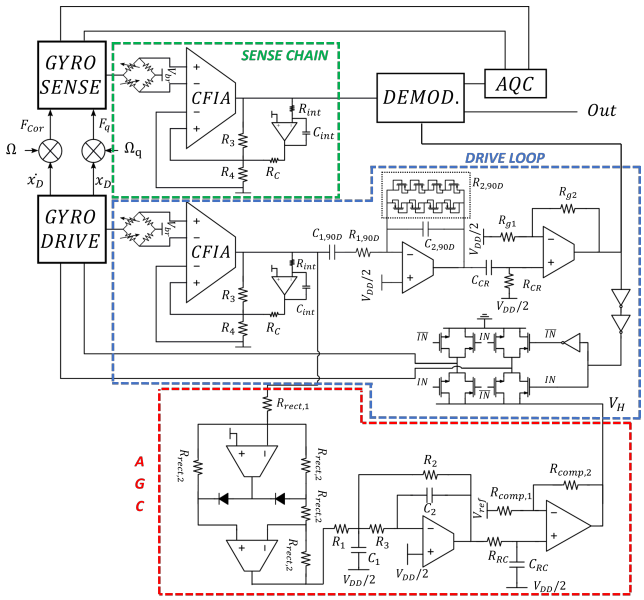

Fig. 4. Block scheme of the implemented ASIC. The drive loop (blue), AGC (red) and sense chain (green) are on chip, together with the current bandgap generator (not shown). Digital demodulation and automatic quadrature compensation loop are, in this version of the ASIC, implemented with an off-the-shelf LIA and discrete electronics, respectively.

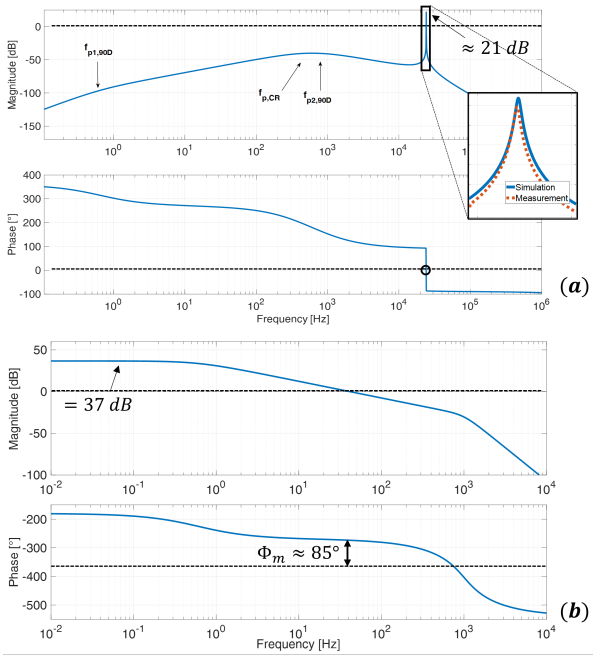

Fig. 5. Loop gain magnitude and phase of the drive loop **(a)** and of the AGC loop **(b)**. The inset shows the peak of the drive loop captured in an open-loop measurement.

In the previous sections, the importance of an accurate phase for the demodulation reference was stressed. In this context, it should be noted that the MEMS itself (block 'Gyro Sense' in Fig.4) introduces, through its transfer function excited in mode-split conditions, a phase lag between Coriolis force and sense motion. For a nominal split of 200 Hz and a sense-mode quality factor of 5000, this lag is in the order of $0.7°$. To obtain a similar lag for the demodulation reference, the gain-bandwidth product (GBWP) of the 90D amplifier and the passive components are sized in such a way that the small phase shift introduced by the MEMS sense-mode transfer function is compensated. To this purpose, the feedback resistance is implemented with a pseudo-resistor with an equivalent value in the $G\Omega$ range, and the GBWP of the designed OTA is decreased down to $1\,MHz$, acting on the Miller capacitance, to apply an additional phase lag and reach the target value. The input capacitance is set to the maximum value for this technology, $100\,pF$; the input resistance value is fixed to $2\,M\Omega$ to introduce negligible noise, but still generating a low frequency pole; finally, the feedback capacitance is chosen as $3.5\,pF$ to fix the gain of the stage nominally at 0.85. This avoids saturation in case of gain variations due to process or temperature. With this sizing, the percentage variation of the phase lag obtained from Cadence Montecarlo simulations (process spreads and temperature) is within $\pm 0.1\%$. The 90D stage output is high-pass-filtered to remove any residual offset and then amplified to saturation by a non-inverting gain equal to 30. Finally, the saturated signal passes through two inverters for edge restoring, and is used, together with a further inversion, as the input signal for the H-bridge. This last stage is formed by 4 transmission gates and has the purpose of generating a differential square-wave driving signal, between $0\,V$ and V_H for the proper bias of the actuation comb-fingers. The driving force amplitude, and thus the drive motion amplitude, are set by the value of V_H, which comes from the amplitude-gain control stage.

The AGC is a negative loop that extracts the mean value of the drive CFIA, exploiting a rectifier followed by a low-pass-filter, compares it with a reference voltage V_{ref} and amplifies it to generate the upper voltage level V_H for the push-pull actuation signal. Since the drive loop passes from differential to single-ended through the drive CFIA, topologies based on butterfly switches cannot be directly implemented[2]. As a consequence, the rectifier is here implemented with a 2-OTA full-wave rectifier, whose gain is set at $\frac{5}{8}$. This small deamplification is needed to avoid saturation of the internal nodes of the rectifier itself due to the forward voltage generated across the *on* diode. For the low-pass-filter stage, needed to cut the component at $2\omega_d$ generated by the rectification, a 3^{rd} order Butterworth low-pass filter is implemented with a 2-pole active multiple feedback cell

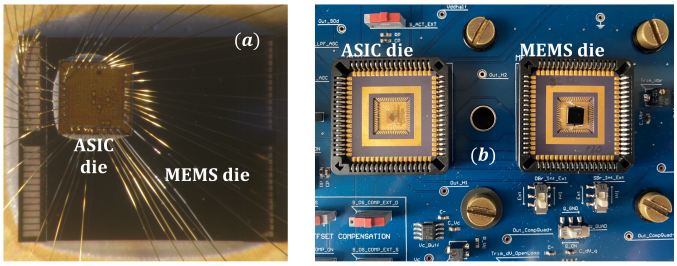

Fig. 6. Picture of the two chips in a stacked wire-bonding configuration **(a)** and in an indepedent wire-bonding configuration, with board level interconnections **(b)**.

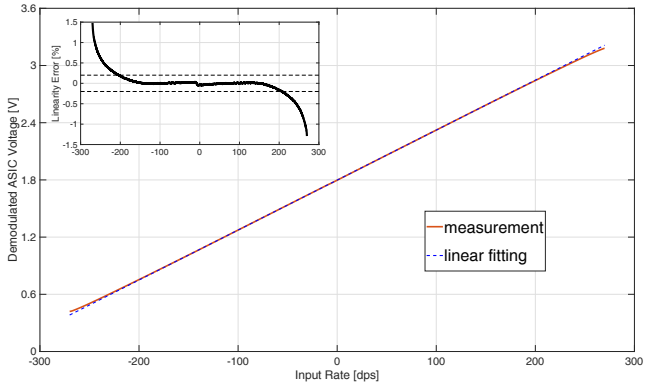

Fig. 7. Demodulated ASIC output averaged 10 times when a quasi stationary rate ramp from -270 dps to 270 dps is applied. The inset shows the linearity error lower than 0.2% up to 200 dps.

followed by a passive RC cell. The multiple feedback active filter was chosen over a Sallen-Key cell due to the lower capacitance values needed for the same pole frequency, choice again imposed by technological limits on passive components. The DC gain is set to -1, with poles frequency at $1\,\mathrm{kHz}$ allowing a reduction of more than $100\,\mathrm{dB}$ at $2\omega_d$. Finally, the comparator stage is simply a non-inverting gain set at 50. Here, the mean value of the drive CFIA is compared with a reference voltage V_{ref}, which can be expressed as a function of the drive displacement x_D:

$$V_{ref} = \frac{V_{DD}}{2} - x_D \alpha_d G_{CFIA} G_{rect} \frac{2}{\pi} \tag{14}$$

The system is biased through a bandgap current generator with a temperature coefficient for the generated current of $TC_I \approx 37\,\frac{ppm}{\mathrm{K}}$ and designed to have the minimum derivative point at ambient temperature. Fig. 5a reports the nominal loop gain of the drive loop (positive at resonance with a gain of $\approx 21\,\mathrm{dB}$), while Fig. 5b correspondingly reports the loop gain of the AGC, negative in DC and with a phase margin of $\approx 85°$.

III. Experimental measurements

The ASIC and MEMS can be either wire-bonded stacked one another (Fig. 6a) for maximum system compactness, or wire-bonded separately and then interconnected on the hosting PCB (Fig. 6b). While the latter solution is not optimal for a final product, it is very interesting as it allows testing exactly the same MEMS sensors already characterized with board-level electronics, for a direct comparison with ASIC-level electronics performance. Note that this is made possible only by the resistive sensing, which is immune to parasitic capacitance bringing noise and disturbances for capacitive-based conventional MEMS processes.

Whatever the configuration, the system is tested on a rate table for linearity measurements. A quasi stationary rate ramp from -270 dps to 270 dps is applied, and the demodulated ASIC output is captured 10 times, averaged and represented in Fig. 7. The linearity error, reported without any correcting procedure and normalized to the 200 dps full-scale, turns out to be lower than 0.2 $\%$ up to 200 dps (see the Fig. 7 inset). Saturation of the ASIC begins to be visible at the trace edges.

For noise and stability characterization, all Allan variance curves are captured under uncontrolled laboratory environment (maximum temperature variations during measurements of $\pm 2^o$ C) for a duration of more than 5 hours. After applying the Allan variance formula with a minimum of 10 averages, the results are represented in Fig. 8 for an observation interval that consequently spans 1865 s. The results obtained with the ASIC are well comparable to those obtained with board-level electronics (shown in the inset of Fig. 8), confirming the low noise introduced by the CFIA front-end and the dominant thermo-mechanical source, giving an angle random walk in the range of $0.004\ °/\sqrt{\mathrm{h}}$ to $0.006\ °/\sqrt{\mathrm{h}}$. These variations are likely due to the different damping coefficient arising due to internal pressure variation from part to part. Additionally, note that no 1/f noise contribution is visible, confirming the theoretical and design prediction.

At the same time, the stability lies in a range between $0.02\ \ °/\mathrm{h}$ and $0.03\ °/\mathrm{h}$, for observation intervals slightly longer than for board-level electronics. No device rises above $0.04\ \ °/\mathrm{h}$ after $1000\ \mathrm{s}$ of observation. Combined with noise results, this yields navigation grade performance within less than $10\,\mathrm{mA}$ of overall current consumption.

IV. Conclusion

The work introduced the operation of piezoresistive NEMS-based gyroscopes coupled to current-feedback instrumentation amplifiers as electronic front-end stages of both the self-sustained drive loop and the open-loop sense chain. This front-end type proved to be the optimal choice in terms of power and noise performance, and allowed to reach navigation-grade performance with an overall consumption well below 10 mA. Further developments are ongoing to include programmable delays on the demodulation section to guarantee minimal phase errors, which may further boost the system stability.

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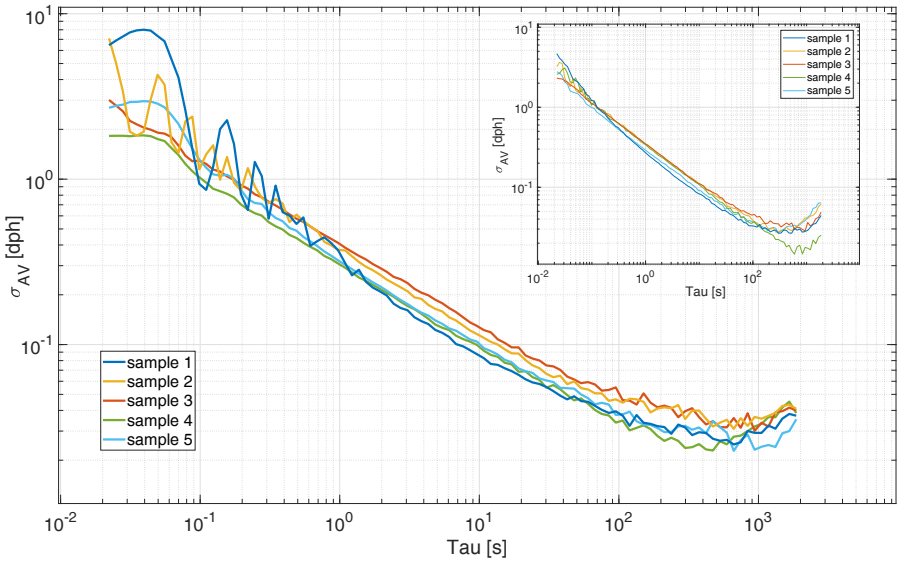

Fig. 8. 5-hr long root Allan variance vs observation interval τ for on 5 samples, demonstrating a noise between 0.004 $^\circ/\sqrt{\mathrm{h}}$ and 0.006 $^\circ/\sqrt{\mathrm{h}}$ and a stability which remains always below 0.04 $^\circ/\mathrm{h}$, best value being 0.02 $^\circ/\mathrm{h}$. The consumption in operation is 22.7 mW. The inset shows root Allan variance on the same 5 samples captured with board-level electronics, at a power consumption larger than 1.5 W.

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