Universal photonic processors in a glass-based femtosecond laser writing platform

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Abstract: Femtosecond laser writing (FLW) can open new perspectives on universal photonic processors (UPPs). We propose here two building blocks for the realization of FLW-UPPs and we show the preliminary results obtained on a 6-mode device.

1. Introduction

Recent advances in integrated photonics have led to the realization of large programmable photonic integrated circuits (PICs) [1] which find their ideal application in classical and quantum optical computing. In this scenario, a great effort is currently directed towards the development of universal photonic processors (UPPs), i.e. PICs able to implement an arbitrary unitary transformation within a given set of optical modes and thus usually referred to also as photonic FPGAs. Different UPPs have been reported in waveguide technologies as diverse as silica on silicon [2], silicon nitride [3], silicon photonics [4] and femtosecond laser writing (FLW) of silicate glass substrates [5], all of them employing meshes of thermally programmable Mach-Zehnder interferometers (MZIs). Recently, an efficient implementation of such basic building blocks (BBs) has been proposed also in an optimized FLW technology [6]. FLW can play a pivotal role in the applications by introducing features completely orthogonal to the ones provided by the standard fabrication processes and materials. Just to name a few: the chance of easily integrating three-dimensional waveguide geometries, the compatibility with polarization-encoded protocols or the possibility of propagating light with low losses ($<0.3\,\mathrm{dB\,cm^{-1}}$) down to the whole visible range, thus being compatible also with devices like integrated quantum memories [7].

2. Basic building blocks

Let us consider the UPP layout reported by Clements et al. in [8]. With this work, we propose the implementation in a FLW platform of Clements' basic BB (Fig. 1a): a reconfigurable MZI in which two thermal shifters (TS1-2, i.e. resistive microheaters) allow the manipulation of both amplitude and phase of the input signals. In order to limit power dissipation and thermal crosstalk, we take into consideration two different isolation structures (IS) for

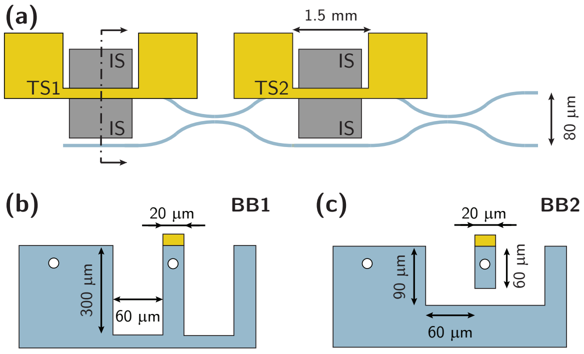

Fig. 1: (a) Basic BB for a FLW-UPP. (b) Cross section of BB1 (i.e. deep trench isolation). (c) Cross section of BB2 (i.e. bridge waveguide).

BB	Pressure (mbar)	Electrical power (mW/2π)	Max crosstalk (%)	Rise/fall time (ms)
BB1	1000	32	30	45
	2.5×10^{-3}	11	3	132
BB2	1000	25	10	25
	2.5×10^{-3}	0.9	0.5	655

Table 1: Performance summary for the BBs measured both at room pressure and in vacuum. A different position within the mesh could be at the origin of a slight variation.

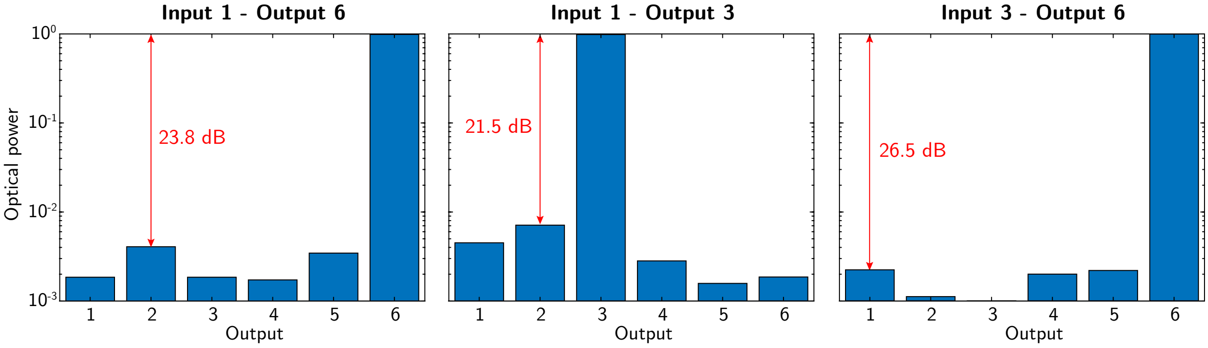

Fig. 2: Optical power measured as a function of the selected output mode when the FLW-UPP is configured as an optical switch. Extinction rate is always higher than 20 dB.

the thermal shifters [6]: BB1 features a deep isolation trench on each side of the heaters (Fig. 1b), while BB2 is characterized by placing the heaters on bridge waveguides (Fig. 1c). Preliminary test circuits have been fabricated by employing single-mode waveguides operating at 785 nm and the results of the experimental characterization are summarized in Table 1. Among these values, it is worth spotlighting the performance of BB2 in vacuum, which opens novel prospects in those applications that require operation in harsh environments like a cryostat or a satellite, where power dissipation is typically subject to strict requirements. In this condition, rise/fall times increase up to hundreds of ms, but this is not an issue for all those experiments that require even hours or days to accumulate a reliable statistics (e.g. boson sampling [9] with a large number of photons).

3. Universal 6-mode photonic processor

In order to demonstrate the potential of this implementation we have fabricated a 6-mode FLW-UPP by employing BB1 (i.e. deep trench isolation) in a Clements' layout with a total number of 30 thermal shifters. Dimensions of the final device are $80\times15\,\mathrm{mm}^2$ and insertion losses are 2.65 ± 0.05 dB (measured before the pigtailing process). The experimental characterization of the phase shifters has been carried out at room pressure for the entire set of internal phases (TS2) by employing the calibration algorithm proposed in [2], which has allowed us to retrieve the $\phi-I$ relation for all the internal heaters. Then, the universal processor has been programmed and employed as an optical switch able to route the light from a generic input to a generic output. The optical power measured as a function of the output mode is reported in Fig. 2, where we consider three different switching configurations. The extinction rate that we measure is always higher than 20 dB, thus providing a first hint both on the quality of the fabricated FLW-UPP and on the accuracy of the calibration process.

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