Research Article | Vol. 30, No. 15 / 18 Jul 2022 / Optics Express 26628
Optics EXPRESS

Temperature and wavelength drift tolerant WDM transmission and routing in on-chip silicon photonic interconnects

IOANNIS ROUMPOS,[1,*] THEMISTOKLIS CHRYSOSTOMIDIS,[1] VITTORIO GRIMALDI,[2] FRANCESCO ZANETTO,[2] FABIO TOSO,[2] PETER DE HEYN,[3] YOOJIN BAN,[3] JORIS VAN CAMPENHOUT,[3] GIORGIO FERRARI,[2] MARCO SAMPIETRO,[2] FRANCESCO MORICHETTI,[2] ANDREA MELLONI,[2] THEONITSA ALEXOUDI,[4] NIKOS PLEROS,[4] MILTIADIS MORALIS-PEGIOS,[4] AND KONSTANTINOS VYRSOKINOS[1]

[1]*Department of Physics, Center for Interdisciplinary Research & Innovation, Aristotle University of Thessaloniki, 57001 Thessaloniki, Greece*
[2]*Department of Electronics, Information and Bioengineering - Politecnico di Milano, Milano, 20133, Italy*
[3]*Interuniversity Microelectronics Center, Kapeldreef 75, Leuven B-3001, Belgium*
[4]*Department of Informatics, Center for Interdisciplinary Research & Innovation, Aristotle University of Thessaloniki, 57001 Thessaloniki, Greece*
[*]*ioroumpo@auth.gr*

Abstract: We demonstrate a temperature and wavelength shift resilient silicon transmission and routing interconnect system suitable for multi-socket interconnects, utilizing a dual-strategy CLIPP feedback circuitry that safeguards the operating point of the constituent photonic building blocks along the entire on-chip transmission-multiplexing-routing chain. The control circuit leverages a novel control power-independent and calibration-free locking strategy that exploits the 2nd derivative of ring resonator modulators (RMs) transfer function to lock them close to the point of minimum transmission penalty. The system performance was evaluated on an integrated Silicon Photonics 2-socket demonstrator, enforcing control over a chain of RM-MUX-AWGR resonant structures and stressed against thermal and wavelength shift perturbations. The thermal and wavelength stress tests ranged from 27°C to 36°C and 1309.90 nm to 1310.85 nm and revealed average eye diagrams Q-factor values of 5.8 and 5.9 respectively, validating the system robustness to unstable environments and fabrication variations.

1. Introduction

The constant growth of data center (DC) traffic [1], combined with the increasing complexity of cloud computing and AI workloads [2], is putting tremendous strain on DC and high-performance computer (HPC) operators, that have to offer increased computing power and bandwidth in a low energy, latency and footprint envelope. On the server design hierarchy, the performance bottleneck is currently located in the underlying network infrastructure, as the deployed in Multi-Socket Boards (MSB) interconnect systems, where connectivity has usually a trade-off between the achievable network radix and the induced energy consumption and latency [3–5]. In this context, Silicon Photonics (SiPho) interconnect architectures based on AWGRs have been extensively studied during the last years as a high-port count and low-power and latency technological candidate [6–9], that can offer the required performance credentials by transferring the proven benefits of point-to-point SiPho transceivers and passive wavelength routing of AWGRs in MSB deployments. Previous demonstrations have already showcased the benefits of

#455107 https://doi.org/10.1364/OE.455107
Journal © 2022 Received 28 Jan 2022; revised 20 May 2022; accepted 31 May 2022; published 8 Jul 2022

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such architectures, allowing interconnection of up to 8 sockets with 4.2 pJ/bit energy efficiency [10] and revealing a 5× reduction of execution time in multi-GPU systems [6].

Harnessing, however, these credentials necessitate a holistic system level approach that takes into account, the reality of having to co-integrate several photonic components to facilitate all the required functionalities of multiplexing, modulation and routing, as well as safeguarding the correct operating point of all the constituent devices versus the inherent temperature and wavelength perturbations typical in a DC environment. These requirements become even more strenuous, when considering Wavelength Division Multiplexing (WDM) based architectures that leverage the high bandwidth, low power, and low footprint of photonic ring resonator (RR) devices, that are highly sensitive to temperature and fabrication variations [11–16]. To this end, different feedback-based methods have been proposed to mitigate this issue and stabilize the operation of RR based structures, including RMs, that entail either tapping a small portion of the optical signal emerging at their output and measure its average power and/or optical modulation amplitude (OMA) [17–19] or exploiting photoconductive effects to estimate the light traversing the optical system [20]. In both cases however, the proposed control techniques either cause high optical losses, effectively limiting the scaling of the photonic system, or need calibrations that might be inefficient considering the required time and related power consumption. As an alternative, a ContactLess Integrated Photonic Probe (CLIPP)-equipped control system, that utilizes a non-invasive and calibration-free dithering-based feedback technique, was recently proposed and demonstrated [21,22] as a critical subsystem of an AWGR-based interconnect, validating its credentials in simultaneously locking a communication link over a passive resonant circuitry chain comprising a multiplexer (MUX), an AWGR and a demultiplexer (DEMUX). This has leveraged a dithering-based feedback mechanism that locked different photonic components in the point of maximum transmissivity. Incorporating, however, an on-chip active resonant, like an RM-based transmitter, in the resonant elements chain in order to complete an on-chip transmitter/routing interconnect system for multi-socket applications [6–8,10], necessitates a novel and more sophisticated approach, given that the optimum operating point of an RM cannot be easily defined through an optical power monitoring approach using the dithering method.

In this paper we demonstrate a temperature and wavelength resilient WDM SiPho transmitter, performing as the constituent sub-system of a 2-socket AWGR-based interconnect, that safeguards stable operation along an active-passive resonant circuitry chain through a dual control CLIPP-based feedback mechanism. The control circuitry establishes and maintains the working points of the constituent photonic building blocks, exploiting a novel algorithm to lock the RMs based on the 2nd derivative of their transfer function, that converges to an operating point close to the RM minimum transmission penalty and a proven previous approach to lock the MUXs at the point of maximum transmission. The 2-socket AWGR-based interconnect was experimentally validated in a 25 Gb/s two-socket modulation and interconnection routing scenario, with the system stressed through external temperature and wavelength perturbations. The thermal and wavelength stress tests ranged from 27°C to 36°C and 1309.90 nm to 1310.85 nm and revealed average eye-diagram extracted Q-factor values of 5.8 and 5.9 respectively, corresponding to theoretical bit-error-rate higher than 3.32×10^{-9} for both cases and validating the systems robustness.

2. System architecture and control strategy

A generic layout of the envisioned AWGR-based system, when interconnecting an N number of nodes herein defined as sockets, is illustrated in Fig. 1(a) and follows the architecture presented in [6,7]. The proposed topology consists of the following building blocks: a) N WDM optical transmitters (Tx), each containing N-1 channels at different wavelengths that are modulated with RMs, multiplexed through a double ring-based (N-1):1 WDM multiplexer (MUX) and injected to the AWGR, b) a single mid-board passive routing platform implemented by a cyclic N×N AWGR and (c) N receivers (Rx), each comprising a Photodiode (PD) followed by a Transimpedance

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(TIA) amplifier. The Tx and Rx engines connect each socket with the passive AWGR router to enable all-to-all connectivity with the remaining N-1 sockets in a low-power and low-latency fashion. It should be noted that the required number of Tx channels for each Socket is N-1, as there is no need for connectivity between the same Socket.

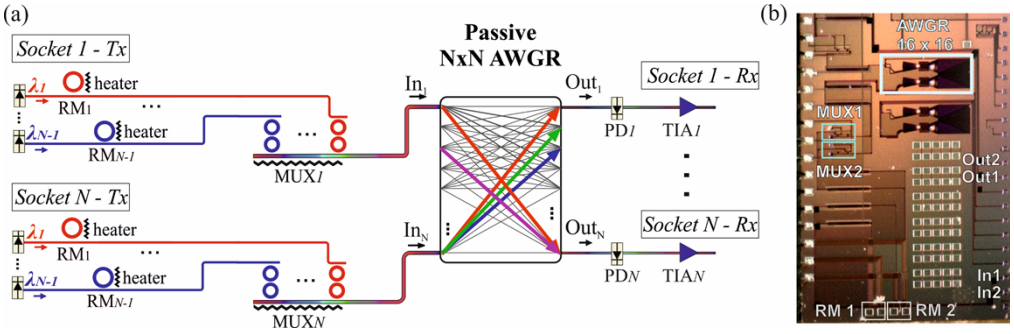

Fig. 1. (a) AWGR-based optical interconnection architecture employing ring-based WDM transceivers and (b) microscope photo of the 2-socket SiPho chip.

In this context, to assess the system level performance of the AWGR interconnect equipped with the novel dual-control CLIPP-based feedback circuitry, we utilized a previously specially designed SiPho chip [21], illustrated in Fig. 1(b), that incorporates all the necessary photonic components required to realize a 2-socket interconnection link. The optical system incorporates two Tx modules, each one equipped with an RM of 33 GHz bandwidth and Q-factor of 5000 [14], followed by an 8×1 MUX, comprising two 2nd order ring resonators, with a channel spacing of 1.2 nm. A 16×16 AWGR [23], with a channel spacing of 1.10 nm implements the passive routing core of the interconnect, receiving signals from the Tx modules and forwarding them to the respective output port based on their wavelength. Each resonance-based structure (RMs and MUXes) is equipped with an integrated heater, that enables thermal resonance tuning, while CLIPP sensors [24] are placed after each component to monitor the optical power traversing the respective optical path. Heaters and CLIPP sensors are accessible through DC pads that are wire-bonded to an interface board, which is subsequently connected to the FPGA-based control system that acquires the signals from all the sensors and drives all the heaters in parallel [25]. The board is also equipped with a temperature control system consisting of a thermoelectric cooler (TEC) and a thermistor, allowing real time monitoring and control of the average on-chip temperature.

A schematic diagram and the experimental setup including the photonic and electronic components of the integrated demonstrator is depicted in Fig. 2. Light-beams from two lasers, one tunable laser source and one DFB laser, with wavelengths of $\lambda_1 = 1310.3$ nm and $\lambda_2 = 1311.3$ nm respectively, were coupled on-chip via PDK-ready TE-polarization grating couplers (GCs), at the input optical ports of Socket 1 (In1) and 2 (In2). Each GC introduced approximately 4.5 dB of optical loss in the 1310 nm transmission window, with the injected light polarization optimized with the use of off-chip polarization controllers (PC). The two light beams were then coupled to the integrated RMs (RM1 and RM2), that superimpose the electrical data originating from each Tx to the respective optical signals. Each RM incorporates a p-n junction-based phase shifter electrically accessed with high-speed RF pads, that induces carrier depletion effect in the silicon waveguide when a reversed bias is applied [11]. It should be noted that in the following experiments only the signal traversing RM1 was modulated on-chip, due to design limitations that constrained access to the pads of RM2 with the RF tip. An Arbitrary Waveform Generator (AWG) was used to generate a 25 Gb/s NRZ pseudo-random binary sequence (PRBS-9) with a pattern length of 511 bit and a 550-mV peak to peak amplitude. The electrical signal was

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subsequently amplified in an RF amplifier combined with a DC voltage of -2.5 V via a Bias-T and finally applied to RM1 by a 40 GHz 3-dB bandwidth unterminated GS probe tip. As such, the signal applied to the RM had an RF voltage swing of 2.3 Vp-p, ranging between -1.35 V and -3.65 V. Finally, the λ1 and λ2 optical signals emerging at Output ports 1 and 2 respectively were coupled out of the chip via GCs. An optical power meter was employed to monitor the power fluctuations on the signal originating from Socket 2 at Out2, while the modulated signal originating from Socket 1 at Out1 was amplified in a PDFA, filtered in an optical bandpass filter (OBPF) with a 3-dB bandwidth of 1 nm and finally injected in a 70 GHz photodiode and monitored at a Sampling Oscilloscope (OSC). The optical path that λ2 traversed (In2-Out2), introduced ~ 19 dB of total losses, with 9 dB originating from the coupling losses of the GCs, 2.5 dB from the 8×1 MUX and 7.5 dB from the AWGR, while the optical path that was traversed by λ1 (In1-Out1) introduced an additional loss of ~ 6 dB stemming from the modulation of the signal in the microring cavity, resulting in total path losses of ~ 25 dB.

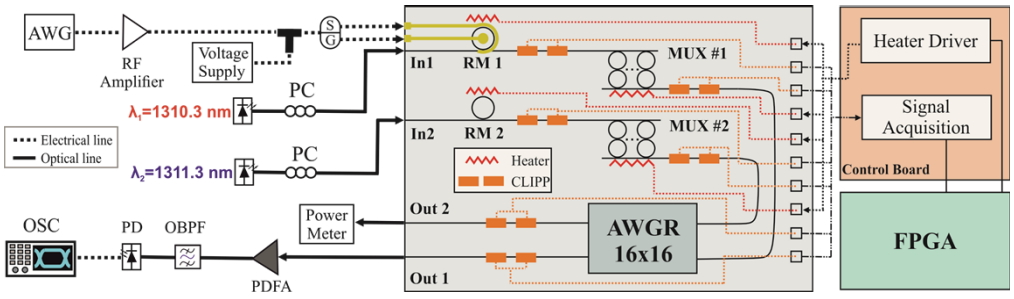

Fig. 2. Experimental setup and schematic layout of the CLIPP-equipped 2-socket AWGR-based interconnect circuit, with the electrical interface points connected to the control board and subsequently to the FPGA.

Real time resonance locking for both RM1 and two MUXes (MUX1, MUX2), was achieved through a dual control strategy, aiming to obtain maximum output power for the MUXes and near-optimum operational bias point for the RM. In both cases, the dithering technique was exploited [22]. Hence, a signal proportional to the first derivative of the transfer function was extracted and fed to a digital integral controller, that drives the heater voltage to bring the controlled device in a stationary point. By correctly setting the sign of the error signal fed to the integrator, it is possible to discriminate between the minima and the maxima in the transfer function, while it should be noted that the tuning system consumes 20 mW per controlled device [26]. Figure 3(a) illustrates the transfer function of the 8×1 MUX1 along with the output dithering signal amplitude, proportional to the MUX transfer function first derivative and obtained by sweeping the integrated heater and measuring the optical power with the CLIPP sensor at the device output. Biasing the MUX heater to drive the output dithering signal to zero results in tuning the MUX transfer function to the point of maximum transmission of the input laser wavelength. By exploiting this strategy, the incoming wavelength λ1, arbitrary tuned to an AWGR transmission peak, was used for locking MUX1 to the AWGR transfer function, as depicted in Fig. 3(b). Locking, however, RMs to their optimal operating point cannot be achieved through the same strategy, as the condition of maximum and/or minimum transmission in the RM transfer functions does not correspond to their optimal operating point. In this case, optimizing the operating point requires a more sophisticated approach and involves balancing the induced insertion loss and the achieved extinction ratio. To this end, we developed a novel control strategy that locks the RM modulator in the operating point of maximum slope, where the 2nd derivative of its transfer function is minimum. This point can be identified by extending the standard dithering technique. A small sinusoidal oscillation is superimposed to the DC voltage

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of RM integrated heater. As a result, the device transfer function vibrates around its bias point, modulating the light at its output. As the RM is a non-linear device, the output modulation contains not only the dithering frequency but also its harmonics, each having an amplitude related to the corresponding derivative of the RM transfer function. Therefore, by synchronously demodulating the CLIPP readout at twice the dithering frequency, a signal proportional to the 2nd derivative can be detected. Figure 3(c) illustrates the transfer function of RM1, acquired by sweeping the voltage of its integrated heater and measuring the power with the CLIPP sensor at its output, along with the measured 2nd derivative dithering signal. As expected, the RM points of maximum slope correspond to the zeros of the output dithering signal. Therefore, by driving the heater to this operate in this region, the RM can be tuned to a close-to-optimal bias point. This has been verified by computing the RM transmission penalty (TP). In Fig. 3(d) the achieved TP, defined as , with P_1 and P_0 corresponding to the optical power levels of the high and low-level of the transmitted bit and P_{IN} to the input optical power, is plotted against the heater induced wavelength shift [27]. The locking point achieved by employing the 2nd derivative strategy is denoted by the green scatter point, showing a transmission penalty of 9.3 dB, 1.8 dB higher than the optimum transmission point of the RM. This TP deviation can be minimized through feeding a non-zero set point to the integrator control, with its precise computation requiring however, prior calibration of the controlled device. Moreover, the figure quantifies the effect of the dithering signal amplitude on the achieved RM operation, by plotting the transmission penalty for the controlled ($V_{dith} = 2$ mV) and uncontrolled ($V_{dith} = 0$ mV) states. The close matching of the two curves validates the negligible signal degradation originating from the locking operation.

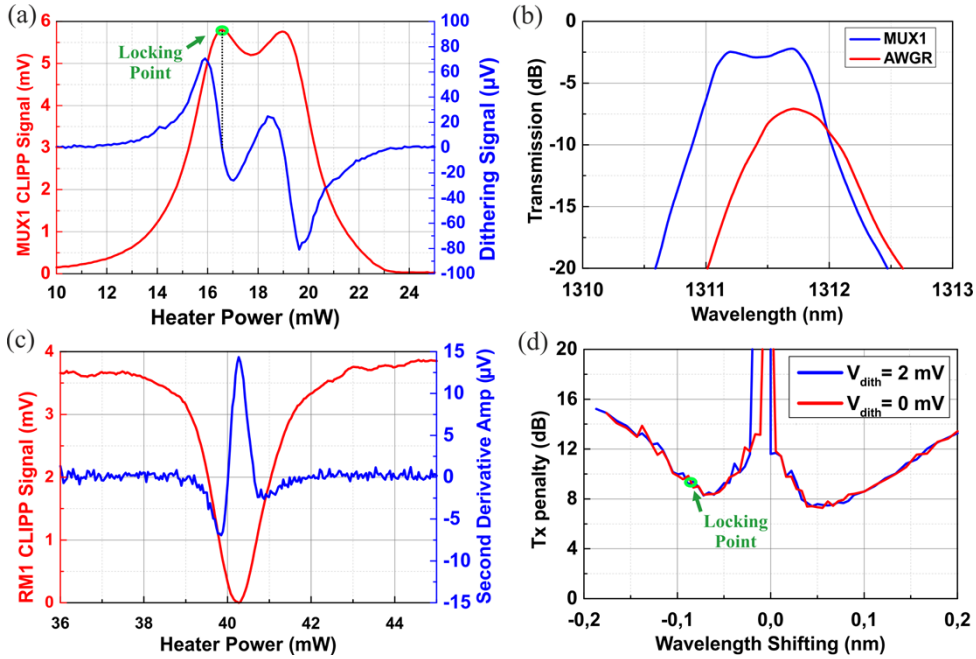

Fig. 3. (a) MUX1 CLIPP signal and output dithering, proportional to the first derivative of the device transfer function, vs heater power. (b) Transfer function of the MUX locked at the maximum transmission point of the AWGR. (c) RM1 CLIPP signal and measured second derivative dithering amplitude as function of heater power. The locking point corresponds to the zero of the second derivative. (d) Calculated transmission penalty at RM1 as function of the wavelength shift for the controlled ($V_{dith} = 2$ mV) and uncontrolled ($V_{dith} = 0$ mV) states. The locking point is highlighted with the green circle.

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The bandwidth of the control system of the RM is around few tens of Hz, enough to compensate for the slow thermal variations, usually featuring an evolution in the seconds timescale, while sophisticated higher bandwidth designs could cover RM's self-heating effects, that are yet not expected to significantly impact highly encoded data e.g. 64b/66b 100G Ethernet [28]. In the stand alone MUX control system case, the bandwidth can reach up to 400 Hz, with a locking time of about 2 ms [22]. Finally, it should be noted that this technique does not require any calibration and it is not affected by fluctuations of the input power and it is thus suitable to control complex systems with multiple devices.

3. AWGR-based interconnect, dual control system evaluation and performance benchmarking

In order to assess the performance of the two-socket, dual control strategy interconnection system, we considered two of the most critical parameters that affect WDM-based systems in real datacenter environments i.e. : (i) the operating temperature range of the deployed optical system, that is affected by both the internal components driving current and thermal behaviors and by the un-avoidable external temperature variations, imposed by the different computing and networking equipment in data center racks; (ii) precise wavelength alignment, that is affected by the mismatch of the targeted and fabricated emission wavelength of integrated lasers and becomes even more pronounced when considering dense WDM operating grids. In this context, the experimental validation of our proposed AWGR-based interconnection system comprised two stress tests, with the first dealing with the thermal on-chip variation and the second with wavelength instability/mismatch. Finally, a comparative analysis versus prior demonstrations in thermal control techniques on photonic devices and systems is presented.

3.1. Thermal stress test

In order to demonstrate the dual-strategy control system ability to compensate externally and internally induced thermal drifts, an external temperature fluctuation was applied on the chip through the on-board TEC, with two optical connections (In1-Out1, In2-Out2) realized through the AWGR interconnect. The first link comprises a CW signal that is on-chip modulated by RM1 at 25Gb/s NRZ, traverses MUX1, is routed through the AWGR and emerges at Out1, where it is evaluated with a Sampling Oscilloscope (OSC). The second link comprises another CW signal that traverses RM2 and MUX2 and emerges at AWGR Out2, where it is evaluated in terms of average optical power using an optical power meter. Figure 4(a) shows the time evolution of the on-chip temperature during the 6-minute-long thermal stress test, with the temperature varying from varying from 27°C to 36°C, with an acquisition step of 1 second. Figure 4(b) illustrates the time evolution of RM1, MUX1 and MUX2 heater voltages, that arise from the feedback control of the CLIPP-based system during operation. The curves mirror the time evolution of the on-chip temperature, revealing the correct response of the locking system to the applied temperature fluctuation. Figure 4(c) depicts the monitored optical power of the CW signal emerging at AWGR Out2 (In2-Out2) versus the on-chip temperature. A small deviation with a maximum of 2 dB is observed, originating from the transfer function of the AWGR that could not be tuned during the experiment. Figure 4(d) illustrates the time evolution of the optical power of the first link (In1-Out1) along with the Q-factor of the captured eye diagrams, acquired at various temperature points during the thermal stress test. A subset of the experimentally captured eye-diagrams is depicted in the insets of Fig. 4(d), corresponding to different temperature point during the testing phase along with an electrical eye diagram from the driver output exhibiting a Q factor of 15. The extracted Q-factor values ranged from 4.6 to 6.8, validating the ability of the dual control system to retain high-performance during the temperature stress test. The same is also confirmed by the average Q value of 5.8, corresponding to a theoretical bit error ratio (BER) of 3.32×10^{-9} [29].

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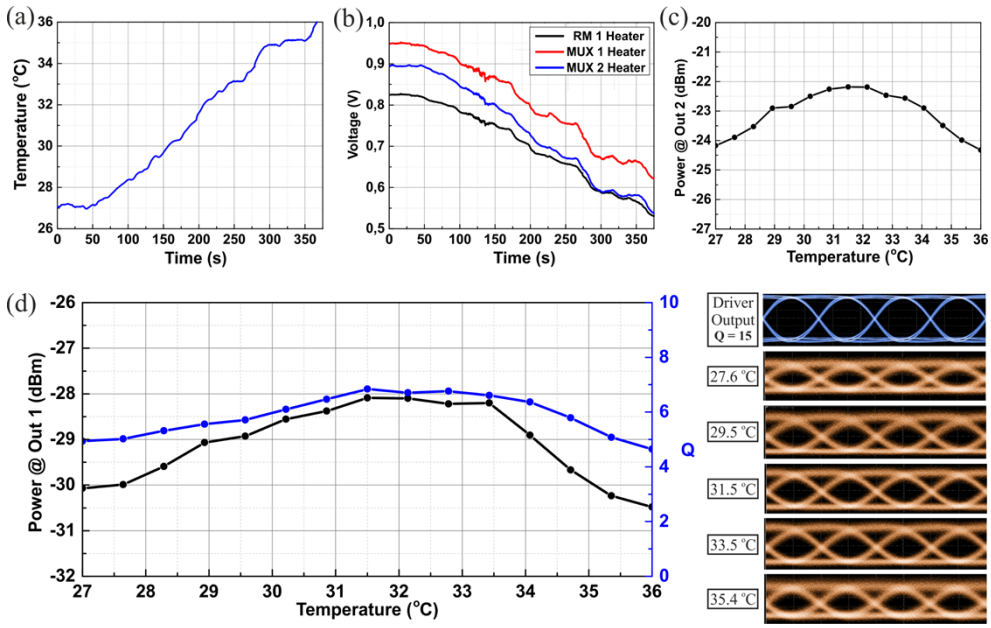

Fig. 4. (a) Temperature variations imposed on the chip through the external TEC. (b) Voltage variations of RM1 and two MUXes heaters over the testing time window. (c) Optical power of the CW signal at Out2. (d) Monitored optical power at AWGR Out1 with the corresponding Q factor values, at each temperature, revealing a mean value of 5.8. Captured eye diagrams at five specific temperatures during the thermal stress test and electrical eye diagram at driver output with Q factor of 15.

3.2. *Wavelength shift test*

After the thermal stress test, we proceeded by emulating the laser emitted wavelength instability and mismatch to the AWGR-based interconnection system grid by introducing a perturbation to Tx1 (In1-Out1) emitting wavelength. To this end, the CW light beam injected in In1 was swept in a 950 pm range from 1309.90 nm to 1310.85 nm with step of 50 pm, during a 4.5-minute-long wavelength shift stress test, as illustrated at Fig. 5(a), while the wavelength of the CW laser injected at In2 signal was kept constant at 1311.3 nm. Figure 5(b) illustrates the time evolution of RM1, MUX1 and MUX2 heater voltages, that arise from the feedback control of the CLIPP-based system during operation. The operating voltage of MUX2 remains constant throughout the experimental procedure, corresponding to the constant value of the incoming light beam wavelength at 1311.3 nm. On the other hand, the time evolution of RM1 and MUX1, reveals the effect of the compensating nature of the control system, that counteracts the increased wavelength by driving the heaters to higher voltages. The signal modulated at RM1, emerging at AWGR Out1, was evaluated in terms of average optical power and through eye diagram-extracted Q-factor values, with the respective results illustrated in Fig. 5(c). The received average optical power follows the same trend as the thermal stress test, with the AWGR channel response imprinted on the final output values shape. The optical eye-diagram extracted Q-factor values follow the same trend, with the insets of Fig. 5(c) showing the eye-diagrams at specific wavelength values. Finally, it should be noted that the recorded Q-factor values ranged

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from 4.1 to 6.8 with an average value of 5.9, that corresponds to a theoretical bit error rate value of 1.82×10^{-9}, validating the ability of the control system to compensate the wavelength drifts that are imposed to the interconnection system.

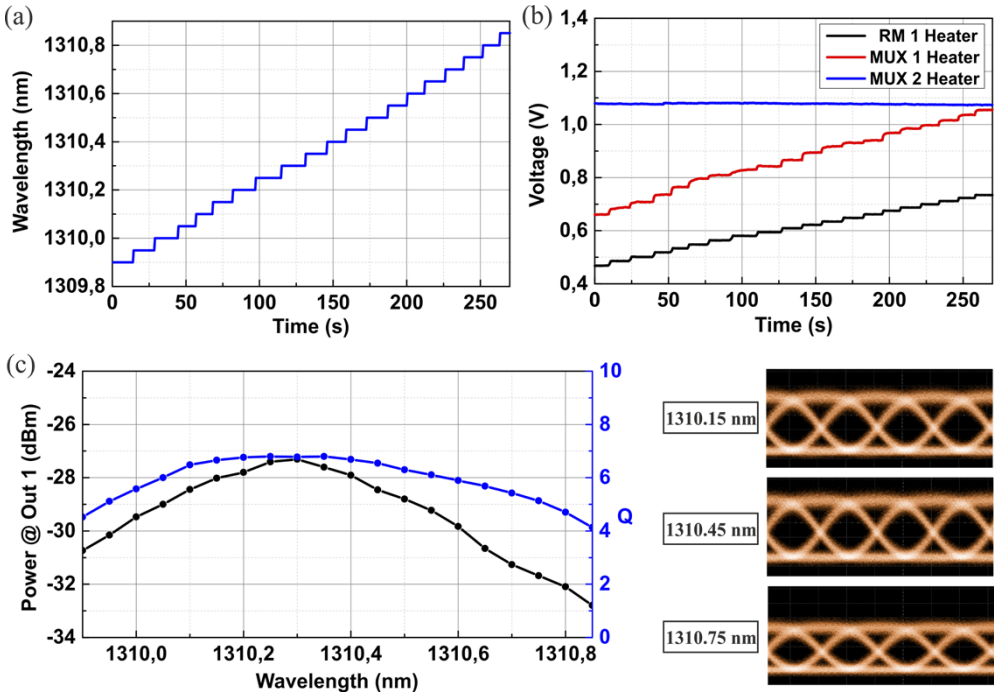

Fig. 5. (a) Wavelength variation over the testing time window, with steps of 50 pm. (b) Evolution of the RM1 and the two MUXes heater over the testing time window. (c) Monitored optical power at Out1 of the AWGR and Q factor values recorded at each wavelength, revealing an average value of 5.9. The three captured eye diagrams refer to wavelengths of 1310.15 nm, 1310.45 nm, and 1310.75 nm, respectively.

3.3. Performance comparison

To conclude, Table 1 summarizes and compares critical performance metrics of our dual control CLIPP-based system with recently demonstrated RM and Ring Resonator -based filter thermal control circuitry. As can be observed, our proposed device is positioned on the middle ground, versus prior demonstrations, on both the integration level of auxiliary circuitry, and the demonstrated data rate, that reaches 25 Gb/s and is only surpassed by [13] and [32]. However, the calibration-free and power-independent nature of our proposed scheme, combined with the first-time simultaneous control of 3 photonic devices, including both high-speed RM and filtering elements, uniquely positions our demonstration as a critical step towards fully integrated and temperature resilient photonic interconnect systems based on RMs.

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Table 1. Comparison of Silicon Photonic circuits with temperature controllers

	Wavelength	Data Rate	Driver/Controller Integration	Control Scheme	Calibration Required	Simultaneously Controlled Photonic Structures
[18]	1550 nm	25 Gb/s	Yes/No	Monitoring the average power	Yes	RM
[34]	1310 nm	10 Gb/s	Yes/Yes	Analog closed-loop w/digital reconfiguration	Not reported	RM
[13]	1310 nm	112 Gb/s	Yes/Yes	Average power stabilization	Yes	RM
[33]	1550 nm	2 Gb/s	Yes/No	OMA monitoring	No	RM
[19]	1180 nm	5 Gb/s	Yes/Yes	Bit-Statistics	Not reported	RM
[30]	1550 nm	25 Gb/s	Yes/Yes	OMA monitoring	Yes	RM
[31]	1320 nm	12 Gb/s	N/A / Yes	Power monitoring	Yes	RR Filter
[32]	1310 nm	112 Gb/s	Yes/Yes	Photocurrent sensing at the RM pn junction	Yes	RM
This work	1310 nm	25 Gb/s	No/Yes	Photocurrent sensing from CLIPP	No	RM + 2 RR Filter

4. Conclusions

In this paper, we presented and experimentally validated a temperature and wavelength perturbation tolerant AWGR-based interconnect system equipped with a dual control CLIPP-based feedback circuitry. The control system safeguards the operating point of a cascade of RM-MUX-AWGR resonant components, exploiting a novel, calibration-free and power-independent control strategy that leverages the shape of the 2nd derivative of the RMs transfer function to lock them close to the optimum operating point. The interconnect system was validated in a 25 Gb/s routing scenario by performing a thermal and a wavelength shift stress test, revealing in both cases stable operation and Q-factors higher than 5.8. These performance credentials validate the ability of the dual control CLIPP-based circuitry to compensate in real-time the thermal and wavelength perturbations imposed on the silicon photonic interconnect chip and demonstrate that the proposed system can be successfully used in multi-socket architectures, even in demanding and unstable environments like datacenters.

Funding. EU Horizon 2020 Framework Programme project NEBULA (871658).

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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