This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LSSC.2022.3173425, IEEE Solid-State Circuits Letters

A Digital PLL with Multi-tap LMS-based Bandwidth Control

Mario Mercandelli, Luca Bertulessi, Carlo Samori and Salvatore Levantino, *Senior Member, IEEE*

***Abstract*—Automatic bandwidth control based on least-mean-square adaptive filters has been demonstrated to desensitize the loop gain of a phase-locked loop from process spreads, environmental variations and channel frequency. This work extends this concept to low-jitter designs that adopts aggressive out-of-band filtering, by introducing multi-tap adaptive filtering. The method requires no injection of a training sequence, potentially degrading phase noise, and it is particularly suitable for bang-bang PLLs whose loop bandwidth depends on input noise. A 3.7-to-4.1-GHz PLL prototype embedding a 16-tap adaptive filter for loop gain estimation demonstrates 150-kHz loop bandwidth over input noise and voltage supply variations, at 183-fs RMS integrated jitter and 5.3-mW power consumption.**

***Index Terms*—CMOS, Digitally-assisted analog circuits, LMS, Frequency synthesis, Phase-Locked Loop.**

I. Introduction

Low-phase-noise and low-jitter phase-locked loops (PLLs) fully integrated in CMOS are nowadays employed as frequency synthesizers in any advanced wireless systems. To guarantee proper filtering of phase noise sources and stable phase noise profile, real products require methods to compensate the spread of several parameters. While the frequency of the reference typically obtained from a quartz crystal has good stability and the frequency division in the loop is exact, the loop filter, the phase-detector gain and the voltage-controlled-oscillator (VCO) sensitivity are subject to process, voltage and temperature [1]. Furthermore, VCO sensitivity is also a function of the synthesized frequency, as any practical VCO exhibits a voltage-to-frequency characteristic significantly nonlinear.

On this respect, digital PLLs (DPLLs) have at least two advantages: (i) they remove one source of spreads as the digital loop filter replacing the traditional analog one has a transfer function which is insensitive to variations, (ii) they enable an easier implementation of powerful background adaptive calibration algorithms to compensate system non-idealities such as loop gain variations. Those advantages combined with their scaling-friendly architecture has made DPLLs particularly attractive to cope with the surge of mobile applications recently driven by remote working and contactless businesses [2], [3]. If a binary phase detector (BPD) is adopted in place of a multi-bit high-resolution time-digital converter (TDC), DPLLs are able to reach even lower jitter and power consumption without compromises in other performance metrics. The only complication is the dependence of the BPD gain, and, in turn, of the loop gain, on the the detector input jitter [4], which adds a new source of bandwidth sensitivity.

This letter reports the design of a 3.7-to-4.1-GHz bang-bang DPLL with low oscillator phase noise and embedding a novel automatic bandwidth control (ABWC) based on a least-mean squares (LMS) adaptive algorithm, which keeps the PLL bandwidth constant across input-jitter variations, process, or supply voltage spreads [5]. While other techniques aim to automatically optimize the PLL for minimum jitter [6], [7], constant-bandwidth control is mandatory in wireless applications where spot phase noise and channel switching speed are key parameters to be guaranteed over spreads. Unlike prior art [8]–[10], the presented method is applicable to PLLs with low oscillator phase noise for multi-standard transceivers, where aggressive out-of-band filtering is used to meet the spectral phase-noise mask [3], [11].

Manuscript received January 10, 2022; revised March XX, 2022. Manuscript received April XX, 2022; revised June XX, 2022; accepted July XX, 2022. Date of publication July XX, 2022; date of current version August XX, 2022. This article was approved by Associate Editor XXXX *(Corresponding Author: Salvatore Levantino.)*

Mario Mercandelli was with the Department of Electronics, Informatics and Bioengineering (DEIB) of Politecnico di Milano, 20133 Milan (Italy). He is now with Qualcomm Inc., San Diego (CA).

Luca Bertulessi, Carlo Samori, Salvatore Levantino are with the Department of Electronics, Informatics and Bioengineering (DEIB) of Politecnico di Milano, 20133 Milan (Italy) (e-mail: salvatore.levantino@polimi.it).

Digital Object Indentifier XXX/XXX

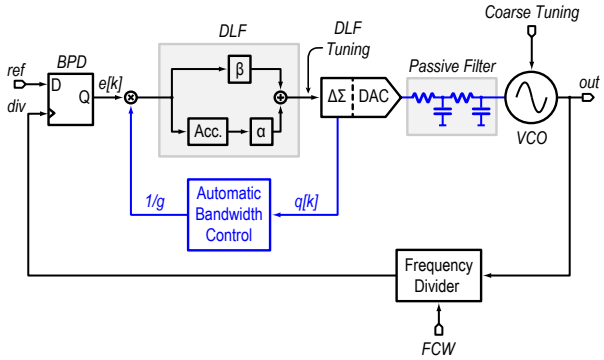

Fig. 1. Block diagram of bang-bang digital PLL with out-of-band filtering.

II. Review of Conventional Bandwidth Control

The simplified block diagram of a typical DPLL with BPD phase detector and automatic bandwidth control is shown in Fig. 1. Figure 2 shows the model in the z-domain, which provides the link between the I/O timestamps, $t_r[k]$ and $t_d[k]$, at the k-th sampling instant kT_r, where $T_r = 1/f_r$ is the reference period. The digital loop filter (DLF) $H(z)$ features a proportional–integral transfer function with coefficients β and α. The resulting loop gain is

$$G_{loop}(z) = -\frac{\frac{G}{g}}{1-z^{-1}} \cdot \underbrace{\left(\beta + \frac{\alpha}{1-z^{-1}}\right)}_{H_{DLF}(z)} \cdot H_A(z) \cdot z^{-1}, \qquad (1)$$

where $G = NK_{bpd}K_T$, N is the division factor, K_{bpd} and K_T are the gains of the BPD (bit/s) and of the DCO (s/bit), respectively, g is the ABWC normalizing gain, $H_A(z)$ is a transfer function containing high-frequency singularities, that lumps system nonidealities such as the delay introduced by the frequency divider or passive filtering between the DAC and the VCO.

To get a simple expression for the bandwidth, we can approximate the bandwidth with the unity gain frequency of the loop gain, i.e. $f_{bw} \approx (G/g)\cdot\beta f_r/(2\pi)$, as $H_A(z)$ does not play a significant role in setting that frequency. Obviously, f_{bw} is susceptible to PVT spreads, being proportional to both DCO and BPD gain via the G parameter. Moreover, the gain of a BPD, whose input-to-output characteristic is a sign function, can be defined only on average by considering the dithering action of its input random jitter, and a very good approximation of the average BPD gain is $K_{bpd} \approx \sqrt{2/\pi}\cdot(1/\sigma_{\Delta t})$,

0000–0000/00$00.00 © 2021 IEEE

2573-9603 (c) 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Politecnico di Milano. Downloaded on May 16,2022 at 15:57:28 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LSSC.2022.3173425, IEEE Solid-State Circuits Letters

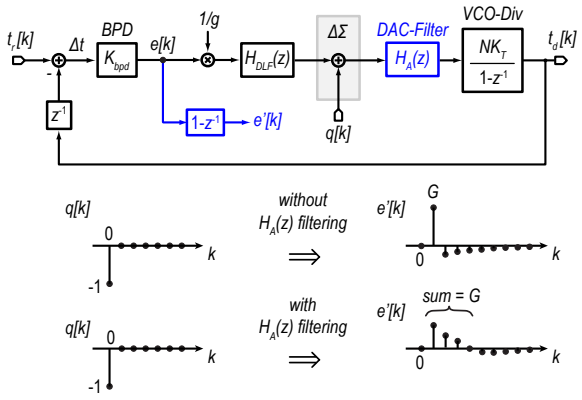

Fig. 2. PLL linear model with impulse responses.

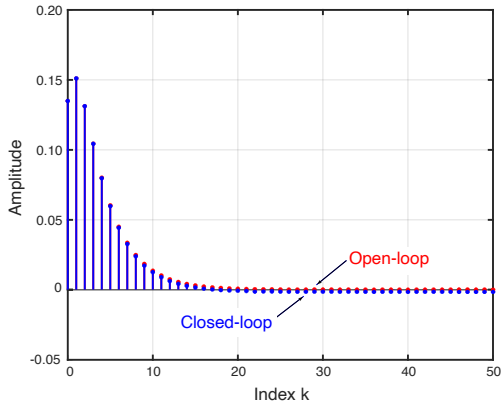

Fig. 3. Impulse response of the $z \cdot F(z)$ closed-loop transfer function (blue trace) and of the $G \cdot H_A(z)$ open-loop transfer function (red trace).

where $\sigma_{\Delta t}$ is the rms value of jitter at BPD input. This dependence gives rise to an implicit problem, since $\sigma_{\Delta t}$ depends on PLL bandwidth that in turn is a function of $\sigma_{\Delta t}$ itself through K_{bpd} [4]. To remove the sensitivity to those uncontrolled parameters, a gain g is introduced in the loop. If g tends on average to G, f_{bw} will be only set by the reference frequency and by a digital coefficient, i.e. β, and will be independent on noise and spreads.

The limited frequency resolution of the digitally-controlled oscillator (DCO) introduces a quantization noise in DPLLs, which turns into phase noise at the output. To limit this contribution, a digital $\Delta\Sigma$ modulator, shown in the block diagram in Fig. 1, is typically employed which filters the DCO quantization noise with a high-pass shape. The quantization error, $q[k]$, introduced by the $\Delta\Sigma$ in the loop (highlighted in the model in Fig. 2) can be leveraged as the training signal of an LMS loop. The G coefficient can be estimated by sensing the BPD output $e[k]$. In fact, the transfer function from $-q[k]$ to $e[k]$ is given by

$$H(z) = \frac{E(z)}{Q(z)} = G \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot \frac{1}{1 - G_{loop}(z)} \cdot H_A(z)\,. \quad (2)$$

To eliminate the integration in $H(z)$, we can rather consider the sequence $e'[k]$ obtained by computing the first difference of $e[k]$, i.e. $e'[k] = e[k] - e[k-1]$; hence, the transfer function from $-q[k]$ to $e'[k]$ is

$$F(z) = \frac{E'(z)}{Q(z)} = G \cdot z^{-1} \cdot \frac{1}{1 - G_{loop}(z)} \cdot H_A(z)\,. \quad (3)$$

The effect of the loop, represented by the $1/(1 - G_{loop})$ term in (3), provides zero DC gain, as $G_{loop}(z) \to \infty$ for $z = 1$, because of the presence of the integrators in (1), and instead tends to unity at large z, because $G_{loop}(z) \to 0$ for $|z| \to \infty$. In the absence of nonidealities or extra filtering, i.e., $H_A(z) = 1$, thanks to the theorem of the initial value and considering a left shift of one sample, the response at $k = 1$ of $e'[k]$ to a pulse $q[k]$ of amplitude -1 at $k = 0$ will be given by

$$e'[1] = \lim_{|z|\to\infty} z \cdot E'(z) = \lim_{|z|\to\infty} z \cdot F(z) \cdot Q(z) = G\,. \quad (4)$$

In other words, the impulse response will be a pulse of amplitude equal to G at $k = 1$, followed by a negative exponential decay with the dominant time constant of the closed loop, shown in the first plot in the bottom of Fig. 2, resulting from the $1/(1 - G_{loop})$ term in (3). Therefore, an adaptive filter with a single tap converging to the first sample of the impulse response is sufficient to estimate G.

The spectrum shaping of $q[k]$ induced by the $\Delta\Sigma$, while, on one hand, attenuates the quantization-induced phase noise at low frequency offsets, on the other hand, emphasizes noise at frequencies around half of the $\Delta\Sigma$ clock frequency, $f_{\rm ck}$, which would only be filtered by the first-order integrator transfer function of the DCO. This means that, depending on the value of $f_{\rm ck}$, a relatively large bump can appear in the spectrum at $f_{\rm ck}/2$. One method to more aggressively filter $q[k]$ is to implement the DCO as cascade of a digital/analog converter (DAC) and a VCO, with a voltage-mode narrow-bandwidth lowpass filter in between, as shown in the diagram in Fig. 1. By combining a second-order passive RC filter and the VCO transfer function, a third-order lowpass shaping can be easily achieved. This enables the adoption of a second-order $\Delta\Sigma$ modulator, that has been preferred, on one side, over a simple first-order one that is prone to generation of idle tones and, on the other side, over a third-order one that would have increased too much the out-of band quantization noise. Unfortunately, the extra filtering $H_A(z)$ introduced to eliminate the noise bump alters significantly $F(z)$, impairing the prior loop-gain regulation method [9].

The impulse response of $e'[k]$ in the presence of $H_A(z)$, being such that $H_A(z) = 1$ for $z = 1$, is depicted in the second plot in the bottom of Fig. 2, and shows an initial response which is longer than a single pulse. The overall impulse response, which is the result of the convolution of the response of $H_A(z)$ and that of the $1/[1 - G_{loop}(z)]$ term, is shown in the plot in Fig. 3 (blue trace), as obtained from numerical simulations. In practice, a single-tap adaptive filter would grossly underestimate G and extending the ABWC algorithm to DPLLs with out-of-band filtering calls for a novel solution.

III. Multitap Bandwidth Control

We should notice that the time constant of the loop is much slower than that of $H_A(z)$, as the extra poles added should not impair loop stability. Therefore, the initial samples of the impulse response of $z \cdot F(z)$ can be expected to be unaffected by the loop, and to be essentially given by the response of $G \cdot H_A(z)$. Referring again to Fig. 3, we note that the red trace, i.e. the impulse response of $G \cdot H_A(z)$, that is $G \cdot h_A[k]$, is a good approximation of the closed-loop impulse response $z \cdot F(z)$ for a number M of initial samples. This means that an M-tap FIR adaptive filter can be used to extract the first M samples of the impulse response from $-q[k]$ to $e'[k]$, and, if M is large enough, the sum of the M samples can be used to get the estimate of the equivalent gain G of the VCO-divider-BPD chain, $\sum_{k=0}^{M-1} G \cdot h_A[k] \approx G$, as $\sum_{k=0}^{\infty} h_A[k] = H_A(1) = 1$.

To implement this, we first replicate the oscillator code-to-phase integration via an equivalent digital integrator [see Fig. 4], obtaining the integrated training sequence, $s[k] = \sum_{h=0}^{k-1} q[h]$, from $q[k]$. The

2573-9603 (c) 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Politecnico di Milano. Downloaded on May 16,2022 at 15:57:28 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LSSC.2022.3173425, IEEE Solid-State Circuits Letters

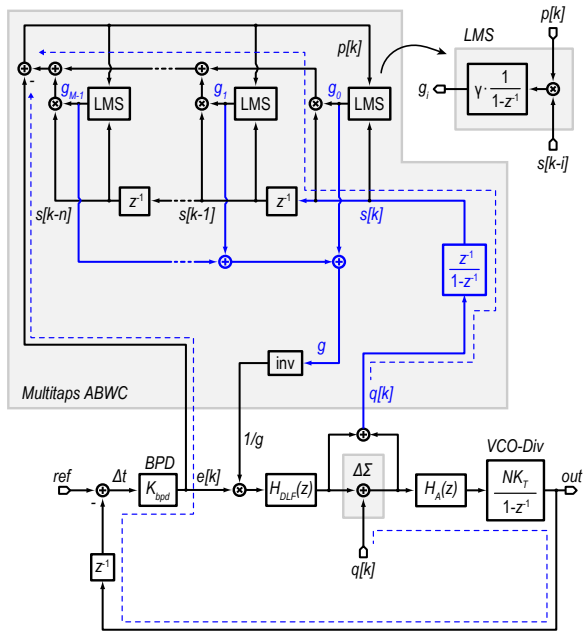

Fig. 4. Block diagram of the bang-bang DPLL with multitap ABWC.

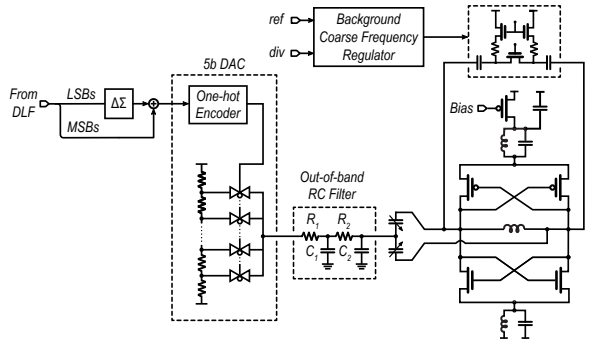

Fig. 5. Circuit diagram of the DCO with ΔΣ-DAC and out-of-band filter.

$s[k]$ sequence is then passed through a tunable FIR filter which will provide an estimation of $G \cdot H_A(z)$. The FIR filter output is then subtracted from $e[k]$ to obtain the adaptive filter error signal, $p[k] = \sum_{i=0}^{M-1} g_i[k]s[k-i] - e[k]$. At the steady-state, the LMS accumulator input will be a zero-average sequence, meaning that, the estimated coefficient g_i, will be such that it nulls on average the correlation between the sequence $s[k-i]$ and the error $p[k]$. The adaptive multitap FIR filter will converge to the best estimate of $G \cdot H_A(z)$, and, by summing all its coefficients, $g = \sum_{i=0}^{M-1} g_i$, the best estimation of G will be computed. By inverting g, the loop gain is normalized and the DPLL bandwidth is therefore accurately controlled. Clearly, the convergence of the algorithm has be to slower than PLL response, not to affect the stability of the PLL itself.

IV. Circuit Implementation and Measurement Results

The DPLL adopting the presented automatic bandwidth control system has been fabricated in a 65-nm CMOS technology. The DPLL synthesizes frequency between 3.7 and 4.1 GHz, with 52-MHz reference signal derived from an on-chip oscillator with an off-chip quartz crystal. The on-chip analog low-pass filter between the ΔΣ-DAC and the VCO, shown together with the DAC and the VCO circuit schematic in Fig. 5, has poles nominally set at 2.5 MHz and

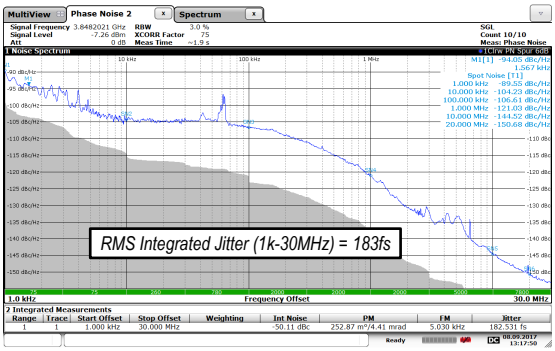

Fig. 6. Measured phase-noise of the 3.848 GHz carrier at nominal supply voltage, when the ABWC circuit is enabled.

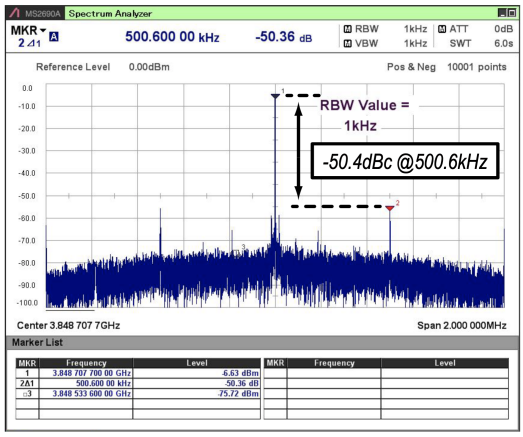

Fig. 7. Measured fractional spurs.

8 MHz frequency. The number of LMS taps to be used in the adaptive filter depends on the duration of the $H_A(z)$ filter response, shown in Fig. 3. The more narrowband is the filter, the higher the number of the taps needed. However, an accuracy tradeoff exists in the choice of the number of taps. While a larger number should allow in principle to estimate a wider portion of the filter response, the singularities associated to the closed-loop transfer function $F(z)$ alter in practice the system response at large k, yielding a less accurate result. In this work, a 16-taps FIR filter has been employed for best accuracy.

Fractional-N operation is obtained by realigning reference and divider rising edges via a digital-to-time converter (DTC) before the BPD, as in [2], [3], [9]. The DPLL overall power consumption is 5.3 mW, from a 1.2-V supply voltage. The measured phase noise when the ABWC algorithm is enabled in background is reported in Fig. 6, where the RMS phase noise integrated in the 1-kHz-to-30-MHz bandwidth is -50.1 dBc or equivalently 183 fs in terms of integrated jitter. The regulated bandwidth is 150 kHz, which is consistent with the digitally programmed setting and the spectrum profile shows that the ΔΣ quantization noise is effectively attenuated below VCO noise, as it can be appreciated from the absence of the ΔΣ modulator noise bump around $f_r/2$ (26 MHz) in the measured phase-noise spectrum. Fractional spurs for near-integer channels are below -50 dBc, as shown in the spectrum in Fig. 7.

To validate the effectiveness of the multitap algorithm, the DPLL phase noise profile has been measured in nominal conditions and varying the supply voltage and the reference phase noise, enabling and disabling the ABWC. In Fig. 8, the DPLL bandwidth has been programmed to 500 kHz, which is the worst case for the PLL phase margin and stability. The blue trace is the phase noise at nominal

2573-9603 (c) 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Politecnico di Milano. Downloaded on May 16,2022 at 15:57:28 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LSSC.2022.3173425, IEEE Solid-State Circuits Letters

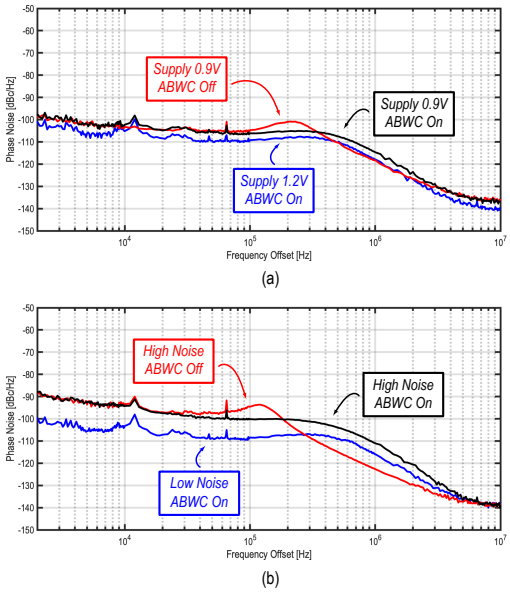

Fig. 8. Measured phase-noise spectra enabling/disabling the ABWC: (a) at nominal/increased supply voltage, (b) at nominal/increased reference noise.

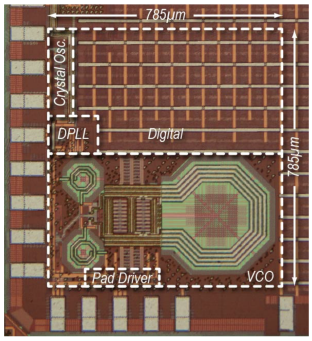

Fig. 9. Die photograph.

voltage supply of 1.2 V. Then, the ABWC is disabled, its coefficients have been frozen and the DPLL supply voltage has been lowered from 1.2 to 0.9 V, inducing a bandwidth narrowing shown by the red trace in Fig. 8(a). After enabling again the ABWC algorithm, the nominal bandwidth is restored, as demonstrated by the black trace in Fig. 8(a). A second test is performed disabling the low-noise on-chip crystal oscillator and using an external reference source with degraded phase noise performances. When the ABWC is disabled, the higher input phase-noise level induces a reduction in the BPD equivalent gain and, in turn, a narrower DPLL bandwidth, as reported by the red trace in Fig. 8(b). Once again, switching back on the multitap ABWC brings back the DPLL bandwidth to the nominal value.

The die, whose micrograph is shown in Fig. 9, occupies an area of 0.61 mm^2. A performance comparison of DPLLs with background bandwidth control is reported in Table I, demonstrating how the presented approach achieves the narrowest bandwidth and the most selective out-of-band lowpass filter. This, combined with a VCO phase noise as low as -150 dBc/Hz at 20-MHz offset, allows to reach the lowest reported jitter among bandwidth-regulated DPLLs.

V. Conclusion

This letter extends the LMS-based bandwidth control of PLLs to the case of high-order out-of-band filtering by introducing a multi-tap adaptive filter algorithm. The implemented 3.7-to-4.1-GHz fractional-N PLL demonstrates 150-kHz bandwidth, insensitive to input noise and voltage supply variations, with a 16-tap adaptive filter for loop gain estimation, at 183-fs integrated jitter and 5.3-mW power.

TABLE I
Performance Comparison Table.

	This Work	[9]	[10]
PLL Architecture	**BB-DPLL**	BB-DPLL	BB-DPLL
Type	**Fractional-N**	Fractional-N	Integer-N
Output Frequency [GHz]	**3.7-to-4.1**	2.9-to-4.0	22.5-to-27.7
Reference Frequency [MHz]	**52**	40	27
Integrated Jitter [fs]	**183**	452	279
Integration Bandwidth [Hz]	**1k-30M**	3k-30M	1k-20M
Power Dissipation [mW]	**5.3**	4.5	25
PLL Bandwidth [kHz]	**150**	300	300
LMS Taps Number	**16**	2	1
Out-of-band Filter Frequency [MHz]	**2.5**	12	N/A
Active Area [mm^2]	**0.61**	0.22	0.09
CMOS Process [nm]	**65**	65	28

Acknowledgments

The authors wish to thank Infineon Technologies Inc. for supporting this research.

References

[1] Yong-Ru Lu, Shen-Iuan Liu, Yu-Che Yang, Han-Chang Kang, Chih-Lung Chen, Ka-Un Chan, Ying-Hsi Lin, "A 2.4-3.0GHz Process-Tolerant Sub-Sampling PLL With Loop Bandwidth Calibration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 873–877, Mar. 2021.

[2] A. Santiccioli *et al.*, "A 66-fs-rms Jitter 12.8-to-15.2-GHz Fractional-N Bang–Bang PLL with Digital Frequency-Error Recovery for Fast Locking," *IEEE J. of Solid-State Circuits*, vol. 55, no. 12, pp. 3349–3361, Dec. 2020.

[3] L. Bertulessi *et al.*, "A low-phase-noise digital bang-bang PLL with fast lock over a wide lock range," in Digest of Tech. Papers of *2018 IEEE Intl. Solid-State Circuits Conf. (ISSCC)*, San Francisco (CA), Feb. 2018, pp. 252–254.

[4] L. Avallone *et al.*, "A Comprehensive Phase Noise Analysis of Bang-Bang Digital PLLs," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 68, no. 7, pp. 2775–2786, Jul. 2021.

[5] M. Mercandelli, L. Bertulessi, C. Samori, S. Levantino, "A 3.7-to-4.1GHz Narrowband Digital Bang-Bang PLL with a Multitaps LMS Algorithm to Automatically Control the Bandwidth Achieving 183fs Integrated Jitter," in *Proc. of 2021 IEEE Asian Solid-State Circuits Conf. (A-SSCC)*.

[6] Ting-Kuei Kuan and Shen-Iuan Liu, "A Bang-Bang Phase-Locked Loop Using Automatic Loop Gain Control and Loop Latency Reduction Techniques," *IEEE J. of Solid-State Circuits*, vol. 51, no. 4, pp. 821–832, Apr. 2016.

[7] Guan-Yu Su, Zhi-Heng Kang, Shen-Iuan Liu, "An Adaptive Loop Gain Tracking Digital PLL Using Spectrum-Balancing Technique," in *Proc. of 2021 Intl. Symp. on VLSI Design, Automation and Test (VLSI-DAT)*.

[8] G. Marzin, S. Levantino, C. Samori, A. L. Lacaita, "2.9 A Background calibration technique to control bandwidth in digital PLLs," in *Digest of Technical Papers of 2014 IEEE International Solid-State Circuits Conf. (ISSCC)*.

[9] M. Mercandelli *et al.*, "A Background Calibration Technique to Control the Bandwidth of Digital PLLs," *IEEE J. of Solid-State Circuits*, vol. 53, no. 11, pp. 3243–3255, Nov. 2018.

[10] C. Tsai *et al.*, "Analysis of a 28-nm CMOS Fast-Lock Bang-Bang Digital PLL with 220-fs RMS Jitter for Millimeter-Wave Communication," *IEEE J. of Solid-State Circuits*, vol. 55, no. 7, pp. 1854–1863, Jul. 2020.

[11] M. Youssef *et al.*, "A Low-Power GSM/EDGE/WCDMA Polar Transmitter in 65-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 46, no. 12, pp. 3061–3074, Dec. 2011.

2573-9603 (c) 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.
Authorized licensed use limited to: Politecnico di Milano. Downloaded on May 16,2022 at 15:57:28 UTC from IEEE Xplore. Restrictions apply.