A Squarewave-Based Multi-Frequency Impedance Analyzer Based on the Heterodyne Architecture

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***Abstract*—This paper presents a custom chip in 180 nm TSMC CMOS process for fast multi-frequency impedance measurements on biological samples. It uses square waveforms for the excitation of the sample and demodulation to drastically reduce the required power consumption of the chip. Impedance inaccuracies given by the harmonics of square waves are avoided using a mixed-signal heterodyne structure with a proper selection of the excitation and demodulation frequencies. The system allows the simultaneous measurement of the impedance at two frequencies and of the DC current. The chip dissipates only 6 mW, including the delta-sigma analog-to-digital converter, and operates up to a frequency of 12 MHz.**

***Index Terms*—Amperometry, delta-sigma modulator, electrochemical impedance spectroscopy, multi-frequency, square wave excitation**

I. Introduction

Electrochemical impedance spectroscopy (EIS) is a noninvasive, label free technique for qualitative and quantitative real-time detection of processes that take place in cells and other biological entities [1]. Recently, multi-frequency EIS-based system have been extensively used to simultaneously probe the particle properties at different frequencies [2]–[6]. In [3], the peak of the measured signal at 500 kHz indicates cell size, while at 5 MHz shows algal membrane properties, in particular, ionic permeability. Also in [4], multi-frequency EIS is used for the discrimination of live and dead cells. Instead of sweeping the whole frequency spectrum, they have proposed a set of optimal frequencies to identify the cell viability of different cell lines by characterizing membrane-relevant phenotypes, which enable complete membrane characterization with simultaneous multi-frequencies.

Although multi-frequency EIS has broad applications in the field of biology and medicine [4], to the best of our knowledge there is no multi-frequency EIS based on custom chip. The examples reported in literature use bulky and expensive benchtop instruments with sinusoidal waveforms as excitation and demodulation signals. Implementing such system with custom chip will be power hungry. To generate sinusoidal waveforms for excitation and demodulation, a digital to analog converter is needed with a high enough operating clock frequency and resolution in order to generate a sinusoidal waveform with a sufficient accuracy, which increases power consumption [7]. Using square waveforms for excitation and demodulation can alleviate these problems and it is an interesting choice for portable or wearable healthcare systems [7], [8].

In this paper, a custom chip is proposed that enables multi-frequency impedance measurement. It can also perform amperometry/cyclic voltammetry simultaneously. It uses square waveforms for excitation and demodulation to drastically reduce the required power consumption for the chip. The paper is organized as follows: Section II shows our proposed architecture. The proposed method for selecting excitation and demodulation frequencies is introduced in Section III, and measurement results are presented in Section IV. Section V summarizes the results and concludes the paper.

II. Proposed Multimodal Chip

Fig. 1 shows the schematic of the proposed multi-frequency impedance analzyer. The excitation voltage is composed of multiple square waves applied to the sample under test (SUT) through a counter electrode (CE). Here, the proposed technique is validated using two simultaneuos frequencies, f_L and f_H, but it can be extended to a multiple frequencies. A transimpedance amplifier (TIA) reads the current of SUT, I_{SUT}, through a working electrode (WE). The high-frequency response of the SUT at a frequency f_H is down-converted to a lower frequency, f_{HD}, using a square-wave mixer and digitized by a delta-sigma modulator (DSM). A direct path from TIA output to DSM input is added for simultaneous low-frequency impedance measurement at a frequency f_L and DC current measurement, enabling electrochemical impedance spectroscopy in parallel to amperometry/cyclic voltammetry measurements. The signals are summed at the input of the DSM using a current-mode adder implemented by the virtual ground of the first integrator in DSM without adding complexity to the system.

Decimator reduces the data rate from sampling rate to Nyquist rate, and also removes quantization noise that is outside the band of interest, which improves the resolution. The obtained digital data are further demodulated at f_L and f_{HD} with a digital lock-in technique to extract the information of the SUT at the excitation frequencies f_L and f_H. The double demodulation of the signal at f_H, the first in the analog domain and the second in the digital domain, implements a heterodyne architecture with multiple advantages. First, it reduces the complexity and power consumption of the analog to digital converter(ADC) thanks to the smaller required bandwidth. Second, multiple high-frequencies can be down-converted at different intermediate frequencies allowing

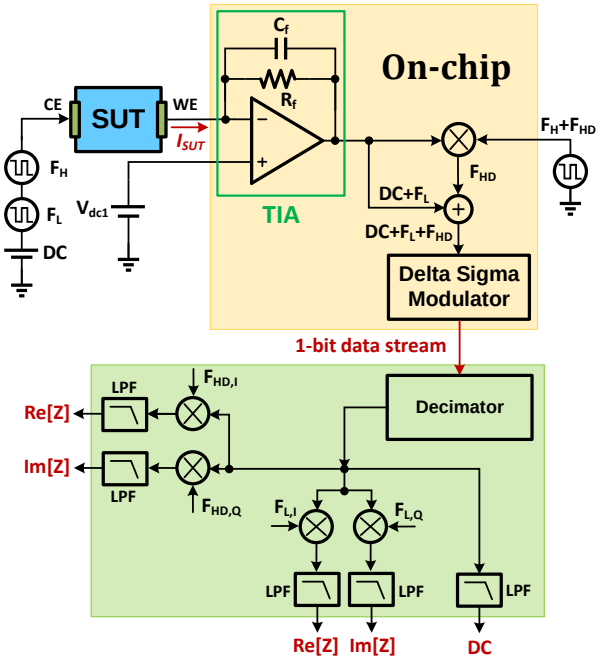

Fig. 1. Schematic of the proposed chip.

simultaneous impedance measurement using a single low-speed ADC. Finally, the double demodulation solves the main drawback of a square wave excitation, that is the low accuracy of the impedance measurement. A direct down-conversion to DC of the square wave at f_H, as in a standard lock-in amplifier, superimposes all the odd harmonics of the signals producing a result that cannot be associated with the SUT impedance at a single frequency. On the contrary, the down-conversion at an intermediate frequency can preserve the amplitude and phase of the signal at the desired frequency without superimposing harmonics. A digital low-pass filter cancels the spurious harmonics before the final demodulation used to extract the impedance of the SUT with high accuracy. In the following section, a set of rules is introduced for selecting the frequencies of excitation and demodulation signals to avoid superimposing of harmonics due to the analog down-conversion operation. By this proper selection of the excitation and demodulation square wave signals, it is possible to simultaneously measure the impedance at multiple frequencies for real-time tracking of the electrical properties of the SUT.

In the implementation of the proposed structure, we used passive double-balanced mixers for the down-conversion of the signals. They are preferred to active ones for better linearity and lower flicker noise and power consumption [9]. The TIA is based on the two-stage operational amplifier reported in [10], but without a constant gm rail-to-rail input stage. For the implementation of the DSM, a single-bit second-order continuous-time DSM (CTDSM) is used. CTDSMs benefit from intrinsic anti-aliasing property thanks to the filtering action of the integrators. In order to reduce undesired effects of harmonics, we have selected a cascade of integrators with feedback loop topology for the implementation of the modulator, as it provides better attenuation at higher frequencies than a cascade of integrators with feedforward topology, and does not have peaking in signal transfer function, which can amplify unwanted signals [11].

III. Selecting Excitation and Demodulation Frequencies

Let's suppose we excite the SUT, with three signals: DC, square wave at f_L and square wave at f_H. At the output of TIA, we will have DC, the odd harmonics of f_L at $(2n-1)f_L$ (n is an integer) and harmonics of f_H at $(2m-1)f_H$. f_H will be down-converted to f_{HD} by mixer. It is supposed that the demodulating signal is a square wave at f_H+f_{HD}. Our goal is to avoid overlapping of harmonics on the desired signals due to the demodulation. Therefore, the following conditions should be satisfied.

1) To avoid superimposing of harmonics on f_L by the product of demodulating signal (f_H+f_{HD}) and f_L

$$f_L \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq f_L$$
$$\Longrightarrow \frac{f_H + f_{HD}}{f_L} \neq \frac{2n-2}{2m-1} = \frac{even}{odd} \quad (1)$$

2) To avoid superimposing of harmonics on f_{HD} by the product of demodulating signal and f_L

$$f_L \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq f_{HD} \quad (2)$$

3) To avoid superimposing of harmonics on f_L by the product of demodulating signal and f_H

$$f_H \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq f_L \quad (3)$$

4) To avoid superimposing of harmonics on f_{HD} by the product of demodulating signal and f_H (excluding n=0, m=1)

$$f_H \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq f_{HD}$$
$$\Longrightarrow \frac{f_H}{f_{HD}} \neq -\frac{2m-2}{2n+2m-2} = -\frac{even}{even} \quad (4)$$

This later condition is practically impossible: f_H/f_{HD} not equal to even/even means f_H/f_{HD} not equal to a rational number. However, it is possible to select f_H/f_{HD} equal to a rational number with a large numerator and a large denominator. It will cause overlapping of high order harmonics that are filtered by the limited bandwidth of the circuits. Moreover, the amplitude of the harmonics of a square wave decreases with the frequency, limiting the error due to the overlap.

5) To avoid superimposing of harmonics on DC by the product of demodulating signal and f_L

$$f_L \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq 0$$
$$\Longrightarrow \frac{f_L}{f_H + f_{HD}} \neq -\frac{2m-1}{2n-1} = \frac{odd}{odd} \quad (5)$$

6) To avoid superimposing of harmonics on DC by the product of demodulating signal and f_H

$$f_H \cdot (2n-1) + (f_H + f_{HD}) \cdot (2m-1) \neq 0$$
$$\Longrightarrow \frac{f_H}{f_H + f_{HD}} \neq -\frac{2m-1}{2n-1} = \frac{odd}{odd} \quad (6)$$

The first condition can be satisfied by selecting:

$$f_H + f_{HD} = \frac{o_1}{e_1} f_L \tag{7}$$

where o_1 is an odd number and e_1 is an even number. By using this expression in the second condition:

$$\begin{aligned} & f_L \cdot (2n-1) + \frac{o_1}{e_1} \cdot (2m-1) \cdot f_L \neq f_{HD} \\ & \implies f_L[e_1(2n-1) + o_1(2m-1)] \neq e_1 \cdot f_{HD} \end{aligned} \tag{8}$$

This condition can be satisfied by selecting

$$f_{HD} = \frac{e_2}{o_2} f_L \tag{9}$$

where e_2 is an even number and o_2 is an odd number.

By using the previous equations of f_H+f_{HD} and f_{HD}, the conditions 3, 5 and 6 are always satisfied. Therefore, (7) and (9) allow a selection of the frequencies avoiding an overlap of the harmonics.

As an example, by considering f_L=11.92 kHz, f_H+f_{HD}=(20001/46)f_L=5.183 MHz, and f_{HD}=(14/9)f_L=18.543 kHz the output of the mixer is shown in Fig. 2. In this simulation, we have considered 1600 harmonics for the signals, as higher harmonics have smaller amplitude and will be filtered by TIA. The number on the vertical axis shows how many harmonics are superimposed at the same frequency. The blue crosses are the harmonics arising by the multiplication of the square wave at f_L with the reference square wave at f_H+f_{HD}, and the red circles show the harmonics resulting from multiplication of the square wave at f_H with the reference square wave at f_H+f_{HD}. Also, the red and green vertical lines show f_L, and f_{HD}, respectively. In Fig. 2, harmonics are not superimposed at the same frequency, as expected based on the previous analysis. In particular, there is just 1 harmonic at f_{HD}, and is the result of the down-conversion of the high frequency excitation signal, f_H. As an another example, for f_L=8 kHz, f_{HD}=(14/9)f_L=12.444 kHz, and f_H+f_{HD}=(112417/90)f_L=9992.622 kHz, no spurious harmonics are obtained at f_L, and just 1 at f_{HD}, confirming that we can easily select the frequencies of the impedance measurement by following (7) and (9). Without following such conditions in selecting the frequencies, after demodulation there will be many superimposed harmonics on the desired signals. Thanks to the correct down-conversion of the signals, the digital processing based on the lock-in technique can extract the correct impedance at f_L and f_H without requiring a fast analog-to-digital converter and a sinusoidal excitation.

IV. Measurement Results

In this section, measurement results obtained from different tests will be presented to validate the proposed technique and the silicon implementation on a CMOS chip. Fig. 3 shows the test board and chip photograph. Chip size is 1.6×1.25 mm^2. The total current consumption of the chip is 3.35 mA from 1.8 V supply voltage. The TIA was designed to work with working electrodes of 900 μm^2.TIA and DSM need 0.43 and 2.92 mA, respectively. For generation of clocks for DSM

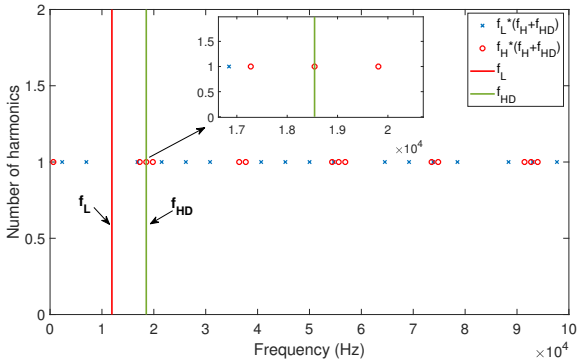

Fig. 2. Mixer output for f_L=11.92kHz, f_{HD}=18.543 kHz, and f_H+f_{HD}=5.183 MHz. The harmonics given by the square waves after the down conversion are depicted with symbols.

and mixer, Keysight 81150A function generator is used. Also, for generation of excitation signals, Tektronix AFG3152C function generator is used. Sampling frequency of the DSM is 25 MHz, and it provides SNR of 92 dB in 40 kHz bandwidth for a 1.6 V differential input signal peak. The input current range of the chip can be digitally selected to be ± 1 μA or ± 10 μA.

To test the performance of the proposed impedance measurement chip, we have used 22 kΩ resistor as SUT. The digital output of the chip was analyzed in the frequency domain using a Fast Fourier Transform on N_{fft}=2^{21} samples. In order to avoid leakage in the spectrum, and measure SNR correctly, f_L and f_{HD} must lie on a bin. Low frequency input is on bin 419 ($f_L = 419 \cdot (f_s/N_{fft})$=4.994 kHz) and high frequency input is on bin 20040 (f_H= 238.895 kHz). Also, clock frequency of the mixer is equal to f_H+f_{HD}=249.993 kHz (bin 20971). Therefore, down converted signal, f_{HD}, will appear at bin 931 (11.098 kHz). We have tested the performance of the chip with both sinusoidal and sqaure wave inputs with 10 mV amplitude. Comparison of the obtained results for square wave and sinusoidal input signals can show the advantage of

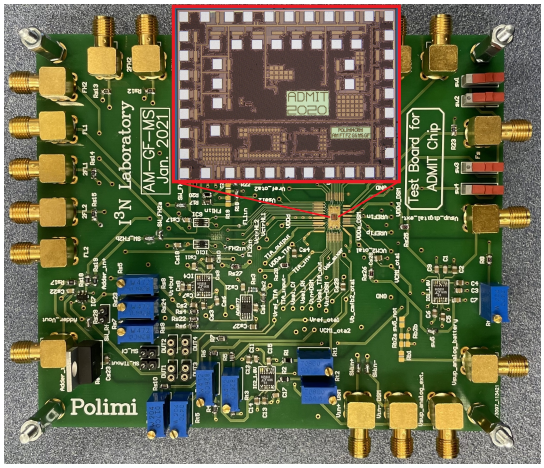

Fig. 3. Test board and chip photograph.

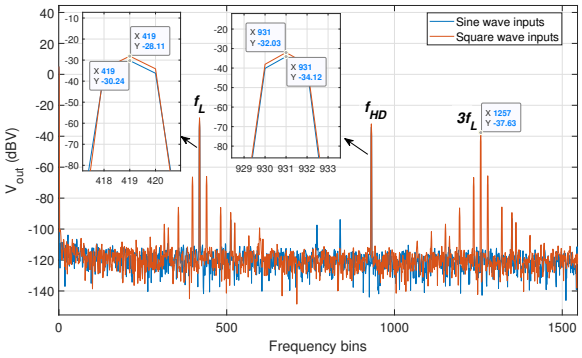

Fig. 4. Output spectrum for sinusoidal (blue) and square waves (orange) inputs.

our proposed method and how the defined rules effectively avoid superimposing of harmonics on the desired signals. Fig. 4 shows the output spectrum of the modulator for square wave and sinusoidal inputs. As it is clear from the spectrum, the proposed method is an effective way to perform multi-frequency impedance measurement.

Fig. 5 also shows the case where f_L, f_H are on bins 1000 (=11.920 kHz) and 433249 (=5164.730 kHz), respectively, and down-converted signal appears at bin 1556 (=18.548 kHz). Thanks to higher f_L, and f_H compared to Fig. 4 there are less harmonics in the spectrum, as they are filtered by TIA.

Finally, measurement results are summarized in Table I. It should be mentioned that, the maximum frequency for impedance measurement is limited by DSM's sampling frequency to avoid aliasing, and it can partially extended by increasing the sampling frequency of the DSM.

V. Conclusions

In this paper, a multi-frequency impedance analyzer based on square wave excitation and demodulation signals and a heterodyne architecture is proposed and verified using a prototype integrated circuit of 2 mm^2. A set of rules is given to measure the impedance limiting errors due to harmonics of the square wave signals. Two frequencies of the impedance

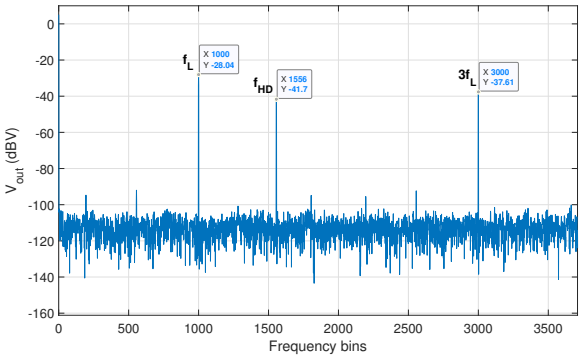

Fig. 5. Output spectrum for SUT of 22 kΩ (f_H=5.164 MHz).

TABLE I
Chip Characterization Results

Parameter	Value
Process	180 nm TSMC
Supply voltage	1.8 V
Power consumption	6 mW
Chip dimension	1.6×1.25 mm^2
Excitation signals	Square/Sine
Demodulation signal	Square
Impedance measurement bandwidth	DC-12 MHz
SNR at f_L=11.92 kHz (BW=2 kHz)	63.84 dB
SNR at f_{HD}=18.548 kHz (BW=2 kHz) (down converted from f_H=5.164 MHz)	49.25 dB

spectrum are simultaneously measured on the frequency range from DC to 12 MHz with a power consumption of the chip of 6 mW. The input current range of the chip can be ±1 μA or ±10 μA. The single ADC used for the impedance measurements also digitizes the input current enabling amperometric or voltammetric measurements in parallel to the monitoring of the impedance. It should be mentioned that the number of excitation frequencies cannot increase too much to avoid a reduction of the SNR. Moreover, to avoid overlapping of the harmonics on the desired signals, the excitation frequencies cannot be freely selected. However, using square waveforms and following our proposed set of rules to choose frequencies drastically reduce the required power consumption for the chip.

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