Closed-form Operational Boundaries for Buck Converters With Constant On-Time Control

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***Abstract*—In this paper, we provide three operational boundaries in closed analytical form for a Constant ON-Time buck converter working in continuous current mode. Two of these boundaries are related to the sudden appearance of pulse-bursting induced by either (i) the hysteresis of the comparator that drives the input of the block implementing the circuit control algorithm (*hysteresis condition*), or (ii) by a period doubling bifurcation (*bouncing condition*). The third operational boundary corresponds to the *saturation condition* of the circuit controller which does no longer guarantee an OFF-time larger than the minimum allowed one. These stability boundaries are provided both for the *adaptive* and the *fixed* ON-time working modes.**

I. Introduction

Switching DC-DC converters are typical hybrid non linear dynamical systems, which play a significant role in nowadays industrial power supply systems. Among possible control strategies of these circuits one can find the ripple-based Constant ON-Time (COT) one. This control scheme has the advantages of simplicity, low cost, fast load transient response, and high conversion efficiency under light-load conditions. COT converters are thus an attractive choice for powering demanding, high-speed digital loads such as FPGAs, ASICs, and CPUs. For the same reasons, COT converters are also largely used in low cost consumer electronics. For a successful design of a COT converter it is mandatory to guarantee that the circuit operates in a *pulse-bursting* free regime [1]–[6], viz. avoiding sub-harmonic oscillations. This is necessary to prevent the undesirable consequences of excessive ripple amplitudes in the inductor current and output voltage waveforms. Furthermore, whenever sub-harmonic oscillations occur, rich frequency spectra are observed that may translate in unpredictable electro-magnetic emissions. These are a well known design aspects, and researches are still working to propose novel analysis techniques and possible technical solutions [7]–[10]. In particular, the availability of operational boundaries, allowing to identify safe regions of operation in the circuit parameter space, is extremely important. Such boundaries are even much more significant if derived and presented in closed-form formula, since they represent effective and simple design rules that can be exploited as a first aid in the converter design, for both specific and general purpose applications.

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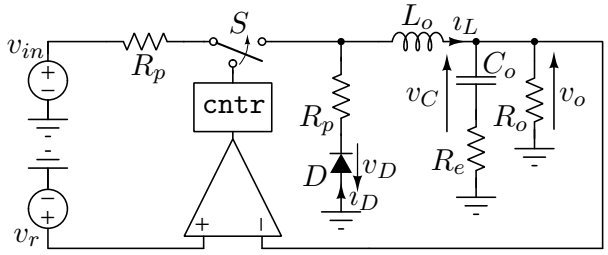

Fig. 1. The schematic of the COT converter. R_e models the equivalent series resistance (ESR) of the C_o output capacitor. The R_p resistors model both the ON-state resistance of the S high-side switch and the D low-side switch.

In [11], the authors derived a straightforward novel sufficient condition, overcoming in term of reliability the popular one presented in [1], [4], and other papers to avoid pulse-bursting. In that work the COT buck converter was studied in *fixed* ON-time working mode only. In this paper we consider both the *adaptive* and the *fixed* ON-time working modes. In particular, in the first case the COT control mimics pseudo-constant-frequency regime during steady-state operation by means of a suitable implementation of the ON-phase timer. The basic idea is to calculate the duration of this phase to emulate the duty cycle of a fixed-frequency buck controller.

We provide three operational boundaries in closed analytical form for a COT buck converter working in continuous current mode (CCM) (viz. continuous conduction mode). The converter control algorithm, which involves a minimum OFF-phase duration, interplays with the hysteresis of the comparator driving the input of the block implementing the circuit control algorithm. The expression of the *adaptive* ON-time takes into account also possible mismatches of the actual circuit w.r.t. the ideal one.

II. The COT buck converter control algorithm

The dynamics of the COT converter state variables (i_L, v_C) is divided in three phases according to a proper control algorithm. The input variable of the algorithm is the output voltage of the comparator (see Fig. 1) whose generic (in, out) transfer characteristic is reported in Fig. 2(a).

The ON-*phase* starts as soon as, being zero the comparator output, the $v_r - v_o$ signal gets positive. The controller catches the positive edge of this signal, the output of the comparator becomes positive, and the S switch is closed for the Δt_{ON} *fixed* ON-time interval. At the end of the ON-phase, S is opened and kept open for the $\Delta t_{\text{OFF}}^{\min}$ *fixed* time interval (*minimum* OFF-*phase*). This phase is mandatory in many practical designs. At the end of this phase, the controller checks the output of the comparator. If the output is zero, the S switch remains

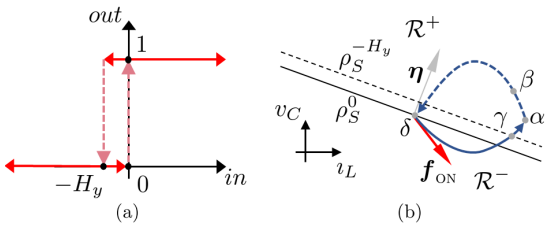

Fig. 2. (a) Asymmetric hysteretic (in, out) transfer characteristic of the comparator ($H_y > 0$). (b) A typical CCM steady-state periodic trajectory of the COT buck converter in the $(\imath_L, v_C)$ state plane. $\boldsymbol{\eta}$ is the unit vector normal to the $\rho_S^0(\imath_L, v_C)$ switching manifold and $\boldsymbol{f}_{\text{ON}}$ is the vector field governing the circuit dynamics at the beginning of the ON-phase. Since $\boldsymbol{\eta} \cdot \boldsymbol{f}_{\text{ON}} < 0$, the trajectory penetrates the $\mathcal{R}^-$ region.

open (OFF-*phase*) until the condition triggering the ON-phase becomes true again.

Since the comparator is typically characterized by hysteresis, as shown in Fig. 2(a), the OFF-phase can start only if, in the time interval $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\min}$, the $v_r - v_o$ voltage decreased below the $-H_y$ threshold, thus resetting the comparator output. If this is not the case, at the end of the minimum OFF-phase a subsequent ON-phase is immediately re-started. In case $H_y = 0$, to allow the beginning of the OFF-phase, $v_r - v_o$ must be still negative at the end of the minimum OFF-phase.

There are many reasons for adding hysteresis to the regulation comparator. For example, one may want to ensure a more "valid" triggering signal for the Δt_{ON} timer, and more generally to improve the switching noise immunity of the regulation circuit. However, as it will be appreciated in the following, a too large hysteresis can introduce undesirable side effects, and other methods for noise immunity enhancement should rather be considered.

In the $(\imath_L, v_C)$ state plane (sketched in Fig. 2(b)) the $v_r - v_o = 0$ and $v_r - v_o = -H_y$ switching conditions induced by the `cntr` block leads to the switching manifolds

$$\rho_S^{\epsilon}(\imath_L, v_C) : v_r - \frac{R_o(\imath_L R_e + v_C)}{R_e + R_o} = \epsilon \tag{1}$$

where $\epsilon \in \{0, -H_y\}$.

In adaptive COT control (i.e., pseudo constant-frequency in CCM operation and low losses), the ON-phase lasts

$$\Delta t_{\text{ON}} = \frac{v_o + \frac{s}{k}}{f_{sw}} \frac{p}{q + \frac{v_{in}}{k}} , \tag{2}$$

where v_o is the converter output voltage, v_{in} is the supply voltage, f_{sw} is the nominal switching frequency, and $k \in [1, k_{\text{MAX}}]$. k allows adjusting the desired switching frequency below f_{sw}, and it is under user control (typically implemented by adding or changing external resistors). The p, q, and s parameters are used to model possible mismatches of the *actual* circuit w.r.t. the ideal one ($p = 1$, $q = s = 0$).

Beside non-ideality factors, the ON-time governed by (2) is lower-bounded by a fixed constant value $\Delta t_{\text{ON}}^{\min}$. This means that, whenever $\Delta t_{\text{ON}} < \Delta t_{\text{ON}}^{\min}$, the COT buck converter starts working with a non-adaptive ON-time. A minimum controllable ON-time limitation is common in DC-DC converters architectures. The $v_{in}^{\dagger}$ value of the v_{in} supply voltage such that the operation mode switches from adaptive to fixed ON-time can be easily inferred from (2).

III. Fundamentals of CCM steady-state dynamics

The $\imath_L$ current is always positive thanks to the D diode in Fig. 1. Actually, in modern architectures such as synchronous buck converters, to enhance converter efficiency the diode is replaced by a low-side MOSFET which is operated as a synchronous rectifier. Consequently, "diode" D, that actually works as a controlled switch in perfect "diode emulation", is modeled as a piecewise-linear ideal component with $\imath_D = 0$ for $v_D \leq 0$ and $v_D = 0$ for $\imath_D \geq 0$. In the following we assume that the COT buck converter operates in CCM only, consequently $\imath_L$ is always positive, $\imath_D > 0$, and thus $v_D = 0$.

Figure 2(b) shows a sketch of the typical CCM steady-state evolution of the COT buck converter. This circuit is designed in such a way that the v_C voltage can be considered almost constant along the periodic steady state behaviour of the circuit, in practice its ripple can be neglected. In particular, being $\delta \equiv (\bar{\imath}_L, \bar{v}_C)$ in Fig. 2(b) the first point of the ON-phase, $\bar{v}_C$ can be derived through the $\rho_S^0(\imath_L, v_C)$ switching manifold exploiting an estimate of $\bar{\imath}_L$. An approximation of the latter can be obtained as

$$\bar{\imath}_L = \frac{v_r}{R_o} - \frac{\Delta \imath_L^{\text{ON}}}{2} , \tag{3}$$

where

$$\Delta \imath_L^{\text{ON}} = \frac{p\left(\frac{s}{k} + v_r\right)\left(v_{in} - \left(\frac{R_p}{R_o} + 1\right) v_r\right)}{f_{sw} L_o \left(\frac{v_{in}}{k} + q\right)} \tag{4}$$

is the $\imath_L$ steady-state ripple approximating as linear w.r.t. time the charging of the inductor, assuming v_o fixed at v_r during the entire periodic steady-state evolution of the COT converter, and neglecting the voltage drop across R_e. In case $\Delta t_{\text{ON}} = \Delta t_{\text{ON}}^{\min}$,

$$\Delta \imath_L^{\text{ON}} = \frac{v_{in} - \frac{v_r(R_o + R_p)}{R_o}}{L_o} \Delta t_{\text{ON}}^{\min} . \tag{5}$$

At the end of the ON-phase, corresponding to α in Fig. 2(b), $\imath_L = \bar{\imath}_L + \frac{\Delta \imath_L^{\text{ON}}}{2}$, and the minimum OFF-phase starts (the v_{in} voltage source is disconnected). At β this phase is concluded and, since the switching boundary $\rho_S^{-H_y}(\imath_L, v_C)$ is typically crossed at γ, a point in between δ and α, the comparator output is zero and the OFF-phase is continues.

The transition between CCM and discontinuous current mode (DCM) (viz. discontinuous conduction mode) can be derived by imposing $\Delta \imath_L^{\text{ON}} = {}^{2v_r}/_{R_o}$, which translates in

$$v_{in} - \frac{v_r(2L_o + \Delta t_{\text{ON}}(R_o + R_p))}{R_o \Delta t_{\text{ON}}} > 0 . \tag{6}$$

In CCM, the $T = \Delta t_{\text{ON}} + \Delta t_{\text{OFF}}$ period of the steady state solution can be achieved by solving the equation $\Delta \imath_L^{\text{ON}} + \Delta \imath_L^{\text{OFF}} = 0$, thus deriving

$$\Delta t_{\text{OFF}} = \frac{p(s + k v_r)(R_o v_{in} - (R_o + R_p) v_r)}{f_{sw} v_r (R_o + R_p)(kq + v_{in})} , \tag{7}$$

or, in case $\Delta t_{\text{ON}} = \Delta t_{\text{ON}}^{\min}$,

$$\Delta t_{\text{OFF}} = \left(\frac{R_o v_{in}}{(R_o + R_p) v_r} - 1\right) \Delta t_{\text{ON}}^{\min} . \tag{8}$$

IV. Operational boundaries

A. Bouncing condition

The sufficient condition presented in [11] to avoid the pulse-bursting phenomenon was obtained by imposing that the $\rho_S^0(\imath_L, v_C)$ switching manifold is reflective for $\imath_L \geq 0$, viz. the periodic steady-state of the circuit belongs to the $\mathcal{R}^+$ region only (see Fig. 2(b)). It translates in imposing that $\boldsymbol{\eta} \cdot \boldsymbol{f}_{\text{ON}} > 0$ for $\imath_L \geq 0$, and reduces to guarantee that

$$\begin{aligned} &\bar{\imath}_L(R_o(1+\Theta) - C_o R_e^2(Ro + Rp)) + \\ &-(L_o + C_o R_e R_o)\bar{v}_C + CoRe(R_e + R_o)v_{in} > 0 \ , \end{aligned} \tag{9}$$

where $\Theta = L_o - C_o R_e R_p$. Under the reasonable assumption $\Theta > 0$, if (9) is verified for $\bar{\imath}_L = 0$ then it is satisfied for any $\imath_L \geq 0$.

Here we propose to weaken (9) satisfying it in the neighbourhood of $\bar{\imath}_L$ given in (3). The above constraint can be solved for instance as a function of v_{in}. Since in general we must have $v_{in} > v_r$ for step-down operation, assuming $\Delta t_{\text{ON}} > \Delta t_{\text{ON}}^{\min}$, and $R_p \ll R_o$, it yields

$$v_{in} > \frac{sp\Theta + k(pv_r\Theta - 2f_{sw}C_oR_eL_oq)}{2C_of_{sw}L_oR_e} \equiv v_{in}^{\text{BN}} \ . \tag{10}$$

In the following we will show numerically that this constraint provides a good estimate of the bifurcation curve marking the loss of stability of the periodic steady-state solution through a period-doubling bifurcation.

In case $\Delta t_{\text{ON}} = \Delta t_{\text{ON}}^{\min}$, the constraint in (9), in terms of v_{in}, simply becomes

$$v_{in} > \frac{R_o + R_p}{R_o} v_r \ . \tag{11}$$

As it will be shown numerically, this condition turns out to be completely non predictive of the appearance of the instability. This means that the sufficient condition derived in [11], cannot be reliably relaxed through the approximation of $\bar{\imath}_L$, in case of a non-adaptive ON-time control strategy, at least if one is interested in identifying limit values of the v_{in} voltage.

B. Saturation condition

At steady-state the condition on saturation of the controller implies that the OFF-phase is not allowed since, exactly at the end of the minimum OFF-phase, the $v_r - v_o$ signal gets positive, viz. $T = \Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\min}$. The controller saturation is often occurring in transient response. It is an indicator that the COT architecture is fully exploited during load transient, i.e. the rate-of-rise of inductor current cannot be further increased. This operative boundary can be derived by imposing $\Delta t_{\text{OFF}} = \Delta t_{\text{OFF}}^{\min}$ exploiting (7). As a function of v_{in} it provides either

$$v_{in} > \frac{v_r(R_o + R_p)((s + kv_r)p + f_{sw}kq\Delta t_{\text{OFF}}^{\min})}{pR_o(s + kv_r) - f_{sw}\Delta t_{\text{OFF}}^{\min} v_r(R_p + R_o)} \equiv v_{in}^* \tag{12}$$

or, in case $\Delta t_{\text{ON}} = \Delta t_{\text{ON}}^{\min}$,

$$v_{in} > \frac{(R_o + R_p)(\Delta t_{\text{OFF}}^{\min} + \Delta t_{\text{ON}}^{\min})}{R_o \Delta t_{\text{ON}}^{\min}} v_r \equiv v_{in}^* \ . \tag{13}$$

C. Hysteresis condition

The effect of the comparator hysteresis manifests if in the $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\min}$ time interval its input does not trespass (decreasing) the $-H_y$ threshold. Assuming $v_C = \bar{v}_C$ during the whole COT buck converter working period, the differential comparator input decreases only during the ON-phase, since during this phase the $\imath_L$ current increases. This implies that the $-H_y$ threshold can be properly crossed merely in the Δt_{ON} time interval. To derive an approximate condition to avoid forcing a sudden ON-phase immediately after the minimal OFF-phase, it is sufficient to ensure that the variation of the differential input of the comparator is larger than the H_y hysteresis window, i.e.,

$$\frac{R_e R_o}{R_e + R_o} \Delta \imath_L^{\text{ON}} > H_y \ . \tag{14}$$

By exploiting Equations (2) and (4), the above inequality can be rewritten as either

$$v_{in} > \underbrace{\frac{pR_ev_r(R_o + R_p)(s + kv_r) + qkf_{sw}H_yL_o(R_e + R_o)}{pR_eR_o(s + kv_r) - f_{sw}H_yL_o(R_e + R_o)}}_{v_{in}^{Hy}} \tag{15}$$

or, in case $\Delta t_{\text{ON}} = \Delta t_{\text{ON}}^{\min}$,

$$v_{in} > \frac{H_yL_o(R_e + R_o) + R_e(R_o + R_p)\Delta t_{\text{ON}}^{\min} v_r}{R_eR_o\Delta t_{\text{ON}}^{\min}} \equiv v_{in}^{Hy} \ . \tag{16}$$

From (15) it is clear that, with an adaptive Δt_{ON}, a limit value exists for the R_e resistance that does not allow the COT buck converter to work for any finite value of v_{in}, i.e.,

$$R_e^{\lim} = \frac{f_{sw}H_yL_oR_o}{pR_o(s + kv_o) - f_{sw}H_yL_o} \ , \tag{17}$$

which applies only in case $pR_o(s + kv_o) - f_{sw}H_yL_o > 0$.

V. Numerical results

In the following subsections two case studies are presented in which some parameter values of the COT buck converter reported in Fig. 1 are fixed, $v_r = 1.8\,\text{V}$, $C_o = 44\,\mu\text{F}$, $R_p = 73\,\text{m}\Omega$, $R_o = 1.1\,\Omega$, and $\Delta t_{\text{OFF}}^{\min} = 25\,\text{ns}$. Concerning Δt_{ON} (see (2)), $f_{sw} = 4\,\text{MHz}$, $k = 1$, $s = 6.6\,\text{mV}$, $p = 1$, and $q = 0$, $\Delta t_{\text{ON}}^{\min} = 125\,\text{ns}$. The remaining parameters are left free and used to trace the operational boundaries introduced in Sec. IV. Of course, one may focus on other subsets of free parameters depending on the adopted overall design strategy. Simulation results were obtained by PAN circuit simulator [12], [13] and MPLAB® Mindi™ Analog Simulator.

At first, the operational boundaries presented in this paper are graphically represented in the (L_o, v_{in}) parameter plane (see Fig. 3). We have stability above the traces at different values of H_y. For low values of H_y, the *hysteresis condition* turns out to be irrelevant as a function of L_o, since the *saturation condition* (v_{in}^*) is predominant. Nonetheless, for $H_y \geq 0.5\,\text{mV}$, it is evident that the H_y and L_o pair must be properly chosen to prevent instability.

By considering the $H_y = 1.5\,\text{mV}$ case, as soon as the hysteresis boundary crosses the $v_{in}^\dagger$ limit, corresponding to the transition from adaptive to fixed ON-time, a significant change

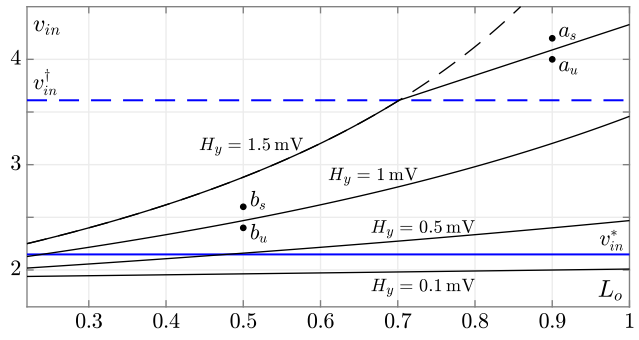

Fig. 3. $v_{in}^{\dagger}$ is the boundary between adaptive (below the dashed line) and fixed ON-time. v_{in}^{*} represents the *saturation condition*. The black solid curves, for several values of the H_y hysteresis-window amplitude, represent the *hysteresis condition*. $R_e = 5\,\mathrm{m\Omega}$. x-axis: L_o [µH]. y-axis: v_{in} [V].

is observed. In particular, adopting a fixed ON-time turns out to be convenient since a wider range of v_{in} is allowed (the solid curve lie below the dashed one which is the extension of the boundary derived if the adaptive ON-time would still operate). Fig. 3 shows the a_s and a_u points corresponding to two different pairs of (L_o, v_{in}) parameters. The former is in the stable region and the latter in the unstable region. The black trajectory in Fig. 5(a) corresponds to the a_s point in Fig. 3, whereas the grey trajectory corresponds to a_u. The inset highlights the presence of a "small turn" revealing that the grey orbit exhibits a sub-harmonic oscillation. Analogous considerations can be done for Fig. 5(b) and the b_s, and b_u points in Fig. 3. It is interesting to note that even a small amount of hysteresis added to the regulation comparator has a significant impact on the inductance values needed to maintain stable operation across the input voltage range. That is, an apparently harmless change in the internal control circuit might have a dramatic impact on the permissible selection space for external components.

In Fig. 4 the discussed operational boundaries are shown in the (R_e, v_{in}) parameter plane. The $v_{in}^{H_y}$ thin black line (*hysteresis boundary*) is the limiting factor until the COT buck converter stops working with an adaptive ON-time, viz. $v_{in}^{H_y}$ trespasses $v_{in}^{\dagger}$ from below since both v_{in}^{*} and v_{in}^{BN} (black thick line, *bouncing boundary*) lie below such a curve. This remains true for R_e values larger than that at the intersection between $v_{in}^{\dagger}$ and v_{in}^{BN}. In fact, even if for lower R_e values the v_{in}^{BN} curve abruptly falls at the constant value provided by (11), it can be noticed that such a curve move completely away from v_{in}^{PD}. The latter corresponds to the period doubling bifurcation of the CCM periodic steady-state solution. v_{in}^{PD} is computed by monitoring the eigenvalues of the monodromy matrix of such a limit cycle, having care of properly resorting to the saltation matrix operator since the circuit is a switching dynamical system exhibiting delayed events too [14], [15]. The v_{in}^{BN} boundary provides a good approximation of v_{in}^{PD} in the adaptive ON-time mode. The black trajectory in Fig. 5(c) corresponds to the c_s point in Fig. 4, whereas the grey trajectory corresponds to c_u. The shape of the grey orbit reveals that in this configuration the steady-state behaviour of the circuit is far from the "ideal" one in Fig. 2(b). Analogous considerations can be done for Fig. 5(d) and the d_s, and d_u points in Fig. 4 (the grey orbit exhibits chaotic dynamics).

Analogous considerations concerning the bouncing condition and the period doubling bifurcation of the CCM periodic steady-state solution can be done if C_o is chosen as a variable parameter. The results reported in Fig. 6 were obtained by choosing $H_y = 1\,\mathrm{mV}$ and $L_o = 0.33\,\mu\mathrm{H}$ as in Fig. 4, and $R_e = 1.5\,\mathrm{m\Omega}$. The discussed operational boundaries are shown in the (C_o, v_{in}) parameter plane. It can be noticed that, also in this case, for C_o values lower than that corresponding to the intersection between v_{in}^{BN} and $v_{in}^{\dagger}$, the former abruptly falls at the constant value given by (11). We verified the correctness of the stability boundary by performing transient simulations on the on the Mindi™ model of the MIC23303 adaptive COT

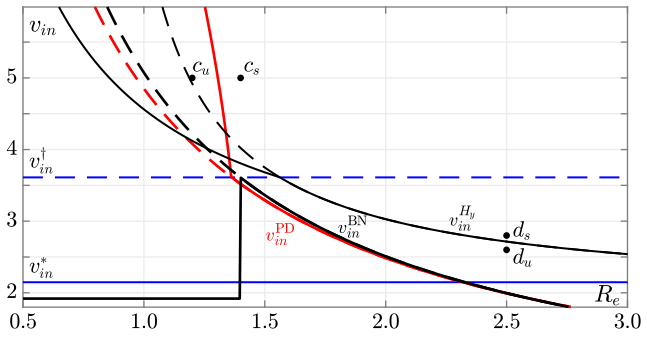

Fig. 4. $v_{in}^{H_y}$ and v_{in}^{BN} represents the *hysteresis condition* and the *bouncing condition*, respectively. v_{in}^{PD} is a period-doubling bifurcation curve. Dashed segments are the extensions of the solid ones computed with an adaptive ON-time. $H_y = 1\,\mathrm{mV}$, and $L_o = 0.33\,\mu\mathrm{H}$. x-axis: R_e [mΩ]. y-axis: v_{in} [V].

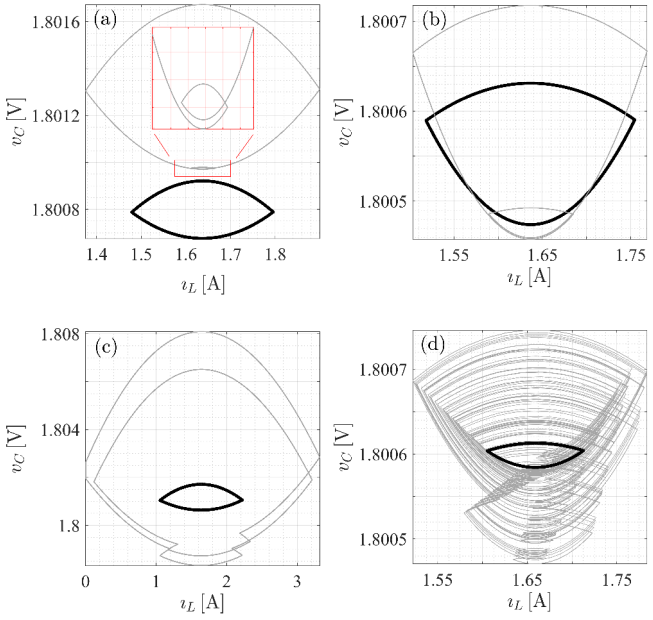

Fig. 5. Steady state behaviour of the COT buck converter for several values of the circuit parameters. (a): $L_o = 0.9\,\mu\mathrm{H}$, $H_y = 1.5\,\mathrm{mV}$, $v_{in} = 4\,\mathrm{V}$ (grey curve) and $v_{in} = 4.2\,\mathrm{V}$ (black curve). (b): $L_o = 0.5\,\mu\mathrm{H}$, $H_y = 1\,\mathrm{mV}$, $v_{in} = 2.4\,\mathrm{V}$ (grey curve) and $v_{in} = 2.6\,\mathrm{V}$ (black curve). (c): $v_{in} = 5\,\mathrm{V}$, $R_e = 1.2\,\mathrm{m\Omega}$ (grey curve) and $R_e = 1.4\,\mathrm{m\Omega}$ (black curve). (d): $R_e = 2.5\,\mathrm{m\Omega}$, $v_{in} = 2.6\,\mathrm{V}$ (grey curve) and $v_{in} = 2.8\,\mathrm{V}$ (black curve).

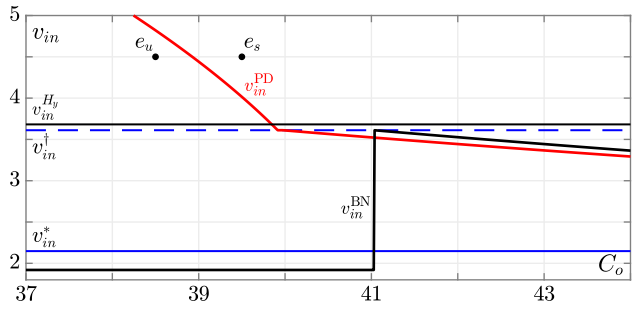

Fig. 6. At e_u and e_s, $v_{in} = 4.5\,\mathrm{V}$ whereas $C_o = 38.5\,\mu\mathrm{F}$ and $C_o = 39.5\,\mu\mathrm{F}$, respectively. $H_y = 1\,\mathrm{mV}$, $L_o = 0.33\,\mu\mathrm{H}$, and $R_e = 1.5\,\mathrm{m}\Omega$. x-axis: C_o [μF]. y-axis: v_{in} [V].

buck regulator by Microchip Technology [16]. The schematic of the circuit is reported in the upper panel of Fig. 7. The central panel and the lower panel refer to the e_s and e_u points in Fig. 6, and show $v_o(t)$ (see Fig. 1). At e_s the steady-state behaviour is periodic and it corresponds to the black limit cycle in Fig. 5. At e_u chaotic dynamics can be observed as it happens in Fig. 5(d).

VI. Conclusion

Simple algebraic expressions involving circuit parameters of a COT buck converter implementation are derived to check stability. They can be used during a preliminary dimensioning phase to adequately choose COT elements, such as inductor and output capacitor, to determine the extension of the input voltage in wide range applications and how external operating frequency adjustment impacts on stability. The effect of a possible hysteresis of the comparator (internal to the chip) is also considered, and its effects on both stability and the external inductor selection are shown. As such, addition of hysteresis to the regulation comparator should be carefully evaluated during the design of the COT controller.

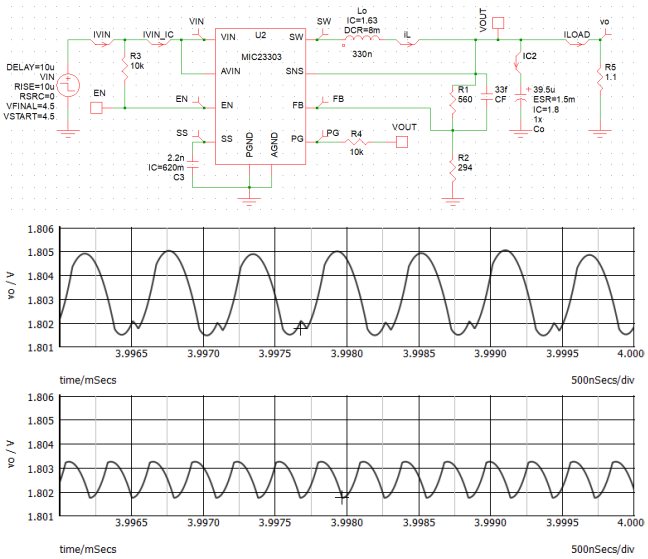

Fig. 7. Upper panel: Mindi™ simulation schematic of the MIC23303 adaptive COT buck regulator by Microchip Technology. Central panel: $v_o(t)$ at the e_u point in Fig. 6. Lower panel: $v_o(t)$ at the e_s

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