Energy Efficient RF for UDNs

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Abstract multi-standard RF front-end is a critical part for current and future mobile generations, where the size, efficiency and the integration of the elements in the RF front-end affect the expectations of the standard performance, This chapter discusses the design of power amplifier in both handset and base station of 5G and beyond. Also, this chapter deals with the filters, antennas, and the integration between these elements. A filter-antenna integration has been studied here. A synthesis-based approach has been followed for the filter-antenna co-design, moreover, design of a differentially driven reconfigurable planar filter-antenna integration with high-gain and high-common mode suppression is proposed for 5G RF front end systems. Finally, an insensitive phased array antenna with air-filled slot-loop resonators is introduced for 5G mobile communications

4.1 Introduction

This chapter addresses the design of an energy efficient and multi-standard RF front-end for next generation (beyond 5G) multi-homing small cells devices based on mmWave. Next generation UDNs need to be green, or in other words "energy aware", so as to support future emerging smart services that are likely to be bandwidth hungry, as well as support multi-mode operation (5G, LTE, LTE-A, HSDPA, 3G among others) in HetNet environments. In this context, this chapter targets the RF front-end architecture and considers power consumption as a key design metric. The functional blocks will harness RF design standardization and spectrum policy design requirements, to provide concrete solutions addressing reconfigurable antennas, tunable filters and power amplifiers, the latter that representing the key energy consumer in the RF chain. Specifically, the chapter contents include:

- MMIC Power Amplifier Technologies and Design for 5G RF Front-End.
- Load Modulation Amplifier Technique for Energy Efficient 5G Base Stations.
- Differentially-Fed Reconfigurable Filtering Antenna for Mid-Band 5G.
- Compact Filtering Antenna for Phased Arrays targeting 5G mmWave FDD backhaul.

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- Insensitive Phased Array Antenna for 5G Smartphone Applications.

4.2 MMIC Power Amplifier Technologies and Design for 5G RF Front-End

Energy-aware cellular communication can provide the reliable, high data rate and extensive connectivity for sharply increasing number of subscribers. Power Amplifier (PA) is one of the key enablers of small cell deployment, since the higher overall system efficiency is approximated by PA characterizations of efficiency and linearity. Therefore, the heterogeneous PAs in terms of energy consumption and transmission power that can prolong the battery lifetime are highly demanded. Doherty technique as one of the most popular efficiency enhancement solutions for high speed and low power applications has been extensively researched to meet the upcoming front-end and base station requirements, more details will be explained in the next section. This section reviews the latest key developments of the integrated MMIC DPAs and explores innovations of technologies and methodologies via a number of design examples that can minimize the PA die size and cost without compromising the gain and linearity performance.

4.2.1 MMIC Active Devises Technologies

In order to meet the required specifications in terms of output power, efficiency, bandwidth, and chip area the first and most important step is the technology selection that covers the substrate material and possible geometry of passive components. The compound substrates are typically characterized by thermal conductivity, cutoff frequency, breakdown voltage, integration level and cost. Several basic properties of MMIC semiconductors including Gallium Arsenide (GaAs), Silicon (Si), Silicon Carbide (SiC), Silicon-germanium (SiGe) and Gallium Nitride (GaN) that provide solutions for wide range of applications, are listed in Table. 4.1 SiGe HBT features good linearity and low-cost for cellular handset PAs, even though it is affected by heating runaway issue and low efficiency. Inherent high band gaps of both the SiC and GaN offer the possibility of operating with high voltages which, minimize the losses of matching and improve the thermal conductivity. Since, higher breakdown voltage provides more robust device, GaN HEMT on Si or SiC can maximize the power density and supply up to 180Woutput power and efficiency up to 70% at the base stations [1].

GaAs is widely accepted as a superior technology with excellent features for a small dimension and high frequency coverage handset applications. Semi insulating substrate property of GaAs provides high carrier mobility that enables fast switching in lower intensity and contributes to long-term operation as well. GaAs InGaP HBT' benefits of high current gain and single power supply polarity can downsize die and module area whiten the cell-phone front-end PAs. However, GaAs HBT device's nonlinearity influences the ideal gain characteristic and reduces its optimum operation. In general, the imbalance of thermal region due to the mismatch of entire HBT geometry at small-scale emitter size causes the heat dissipation. The heating effects can be compensated using ballast resistor as an equalizer with the penalty of gain reduction [2].

GaAs E-pHEMT technology is the Industry's workhorse for monolithic integration of low-noise and low-loss active and passive components up to mm-Wave for handset devices. In fact, it is more reliable in low voltage operation for thermal runaway, possessing the advantage

of high gain, good linearity and great transition frequency. Even though, very thin GaAs substrate thickness ($<75\ \mu m$) has a low thermal resistance, thicker substrate ($>100\ \mu m$) can be used for lower loss [3]. The cross section of a GaAs MESFET is depicted in Fig. 4.1. A thin layer of low energy bandgap InGaAs is sandwiched between both sides of higher energy band gap material layers of un-doped GaAs and doped ALGaAs. Hence, the confined electrons with a heterojunction have much higher drift velocity and move to energy levels whiten the thin layer that yield performance improvement.

Table 4.1 Overview of semiconductor materials

Material	Si	SiGe	SiC	GaAs	GaN	InP
Electron Mobility (Cm^2/V_s)	900-1100	>2000	500-1000	5500-7000	400-1600	10000-12000
Peak Drift Velocity ($10^7\ cm/s$)	0.3-0.7	0.1-1.0	0.15-0.2	1.6-2.3	1.2-2.0	2.5-3.5
Band Gap (eV)	1.1	<1.1	2.2	1.4	3.2	1.3
Freq. Range (GHz)	<40	10-40	15-20	>75	20-30	>115
Gain	Moderate	Better	Lower	Higher	Lower	Higher
Noise Figure	Moderate	Good	Poor	Good	Poor	Good
Production Maturity	12” wafer	8” wafer	4” wafer	6” wafer	4” wafer	2” wafer

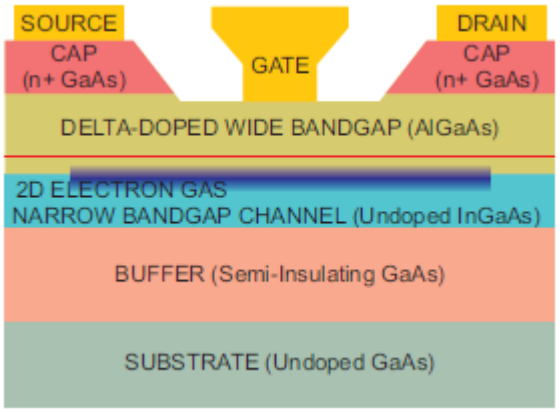


Fig.4.1 Cross-section representation of pHEMT structure including several layers of ion implanted GaAs

4.2.2 Monolithic IC Technology and Design Methodology

Advancement in microelectronics technology have enabled compact circuit configurations and formed the confinement of electromagnetic fields within the semiconductor materials. Microwave Monolithic Integrated Circuits (MMICs) drive PAs to be implemented on the surface of a semi-insulating substrate, providing much higher level of IC integration. In fact, MMICs have been pursued to outpace the discreet devices for critical target of multi-octave operation, that bring about new opportunities and challenges in RF front-end PA design and realization. MMIC offers potential advantages of thin metal thickness, multistage design for higher gain, better amplitude and phase tracking, compact size, higher operating frequency, broadband performance, circuit design flexibility and higher reliability in contrast to the Hybrid microwave integrated circuit (MIC) of packaged transistors counterparts features provided in Table 4.2. While the discrete transistors are mounted on alumina substrate, the well-characterized MMIC devices are implemented by foundry processes. MMIC foundries design a mask-set that consists of multiple geometries of active transistor features and passive

distributed components of MIM capacitors, spiral inductors and resistors that simulate the actual fabricated elements characteristics on wafer.

Table 4.2 MMIC features VS hybrid MICs

Feature	Monolithic	Hybrid
Substrate	Semi-insulator	Insulator
Interconnections	Deposited	Wire-bonded/deposited
Solid state device	Integrated	Discrete
Controlled Parasititcs	Yes	No
Equipment Cost	High	Low
Design flexibility	Very good	Good
Broadband performance	Relatively good	limited
Integration with digital ICs	Possible	N/A
Reliability	Excellent	Fair

In contrast to hybrid microwave, the post-fabrication tuning for monolithically fabricated circuits is no longer available that severs the design sophistication. Chip design flow develops by using process design kit which introduces the foundry-specific's components with more tolerant to process variation and automatic RF testing of IC on wafer for sufficient statistical characterization data.

MMIC design flow starts with a realistic circuit scheme realized by matching networks design process to justify the assumptions. The design synchronization follows to check the layout rules dictated by the foundry process via hole spacing as well as proximity between layers. Additionally, the statistical analysis on the effects of metal interconnection of physical device have to be performed using full electromagnetic EM simulator to minimize coupling effects and verify the layout standards, next, the circuit parameters should be optimized for improving yield for smaller chip size or stepping back to adapt stronger robust topology. Furthermore, Electro-thermal analysis to model the channel temperature as a function of gate width, dissipated power and number of fingers should not be trivialized. Finally, the design can pass to the manufacturing step for final check for packaging requirement and test. An accurate modeling of microstrip discontinuities and acceptable circuit performance can speed up the wafer fabrication process.

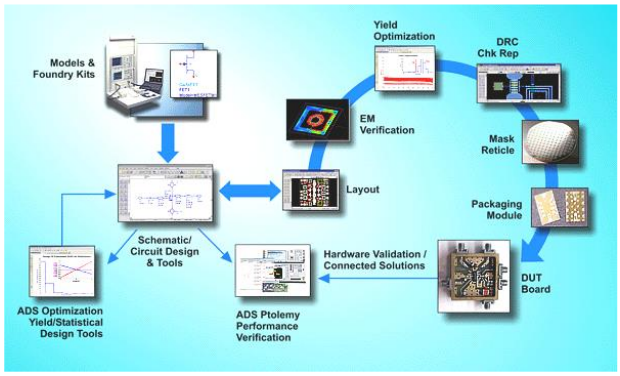


Fig. 4.2 Complete MMIC design flow

4.2.2.1 MMIC Transistor Size Selection

In the mobile handset devices and every portable battery-operated transmitter, where the actual size and weight of the overall apparatus is dictated by the choice of a lightweight and small battery pack, the available bias voltage, voltage swing and device's maximum current are all limited. In this regard, opting the most appropriate MMIC process that transfers specific output power per millimeter length is paramount important. In particular, the total dimension of device can be estimated by sufficient output power specification and available output power of a unit transistor cell. The latter factor is based on the semiconductor technology selection. While enlarging device size improves the output power, it has an inverse effect on the delivered gain, which indicates the trade-off between output power and gain over the frequency range. In fact, the output power is proportional to the device size because it is a function of drain voltage, drain current and efficiency, while the drain voltage is restricted by breakdown voltage specified by substrate material.

One possibility to achieve the maximum output power of device is to enlarge the gate periphery up to the optimum useful device size that can afford an adequate level of gain [4]. This technique depends upon the process selection and the power budget, which is carried out by enlarging the transistor gate width or increasing the number of gate fingers. It should be noted that, by expanding the gate periphery higher output power can be obtained, up to the certain size, however, after exceeding the size restriction, the power densities and device gain start to drop due to the saturation scaling and the parasititcs of output capacitance along-with phase error between the gate fingers and thermal issues are raised up [5]. Consequently, the parasititcs effects in addition with losses and instability introduced by the via inductance, become more pronounce with increasing device size and influence the PAE performance by decreasing the overall gain. Therefore, to ensure the required specifications of bandwidth, gain, output power and efficiency, consistent combination of several stages has to be adapted for better flexibility and gain flatness of the most promising MMIC PA size.

The multi-stage matching MMIC PAs comprise synthesis, analysis and optimization of input, inter-stage and output matching networks stating from output stage and proceeding back towards the former stages. Since, the interactions between stages degrade the output power overall PAE and stability across the band frequency, nonlinear models for obtaining higher PAE and wider bandwidth should be taken into consideration in all stages. It is more desirable to employ fewer stage for higher gain developed and wider bandwidth, since one of the challenges associated with cascade designing is the bandwidth shrinkage [6]. Besides, higher gain at output stage improves the peak efficiency that results in higher output power capacity, whilst, any additional gain stages only enhance the overall device gain in expense of dc power consumption and scarifying bandwidth. Therefore, the optimized PAE can be attained by minimum number of high-gain stages.

4.2.2.2 Matching Networks Design Considerations

The output matching network (OMN) is designed to maximize the output power, since the MMIC PA operates at about 1dB gain compression point of maximum output power and the gain of last stage considerably improves the PAE, it is paramount important to select an appropriate bias point for the output stage. All the matching networks contribute to combine or split the power of transistor cells with lowest loss, cover the required bandwidth and enhance the stability. Several division/combination schemes of power signal using the same substrates as matching networks have been adapted in monolithic PAs such as Wilkinson power divider/combiner [7], Lange couplers [8] and branch-line couplers [9] that further improve the overall output power and suppress any instability. One of the most compact techniques to combine a large number of transistor cells is the metal strip bus-bar combiner [10] that not only feeds the DC current to all the individual transistors in the array in-phase but also implements good matching to the load terminations. The multi-stage ladder [11] is one of the common solutions to combine devices in parallel with symmetrical arrangement of components, however parallel combining decreases the linearity and bounds the bandwidth with increasing number of transistors in low voltage technologies. Note that the number of transistors used in the output stage dictates the width of PA chip.

While the input matching network enhances the input return loss by optimizing the impedance match, the inter-stage matching networks (ISMNs) aim to compensate the gain roll-off and minimize the mismatch loss for gain flatness. Hence, the ISMNs are designed to transfer the optimal load impedance that maximizes the input power of the succeeding stage with DC separation between bias suppliers. It fact, the ISMN should be large enough to drive the output stage into saturation for archiving the best-level of power and efficiency. The optimum output power can be attained, when the input power of output stage is high enough to compress the gain by 1dB. Nonetheless, if the earlier stages cause the PA reaches the 1dB compression point before the output stage is fully compressed, a lower peak efficiency level will be achieved. As a consequence, the preceding stages should be designed for linear operation. Employing high-pass networks or large series capacitors that resonates with the matching inductors are two proposed solutions to accomplished this task [12]. A broadband ISMN requires DC isolation (blocking capacitor) between preceding and following stages, when the biasing network is generally integrated within the matching network for smaller size [13]. The gate bias contains a resistor to provide isolation between power supply and device, and the drain bias is connected to the bypass MIM capacitors, due to its influence on the maximum available gain.

4.2.3 Doherty PA Design for Mobile Handsets

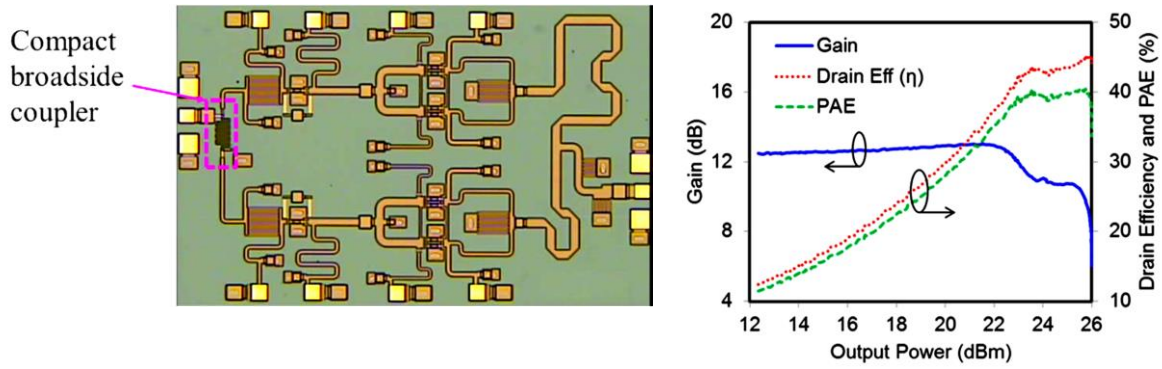
To enable a compact front-end design, significant efforts have been exerted to provide the efficient and linear handset PA when the die area has to be minimized. Dynamic load modulation, envelope tracking and dynamic control of quiescent current techniques have been adapted individually or cooperatively to improve the average efficiency of PA without compromising its linearity [14]. While the envelop tracking enhances the efficiency, it requires an external wideband, small and efficient envelope amplifier that sophisticates its implementation. On the other hand, at mm-wave band frequencies, due to the high loss of passive components, the majority of PAs exhibit very limited back-off efficiency improvement with degraded linearity. In this respect, a great interest of beyond 5G multicarrier applications has been focused on Doherty PA (DPA) technique due to its enhanced efficiency at deep power back-offs for low supply voltage applications and wideband operation potential.

The main challenges associated with the practical DPA for exploiting at mm-wave bands lie in its nonlinear distortion, sensitivity of the input delay of peaking amplifier, realizing the load modulation by narrowband quarter-wavelength at power combiner as well as adding offset lines and phase compensation network. The linear operation of handset DPAs is more critical than the base station DPAs due to the absent of the extensive digital predistortion technique. At lower power levels, the carrier PA should operate highly linear, even though it matches to a high impedance, whilst, at the Doherty region, where, the level of output power with the phase shift between two active devices can significantly vary, the optimum gate bias voltages of both PAs assistances with an offset-line at peaking path can develop the linear operation of DPA. The linearity of a fully integrated HBT DPA has been improved at research level in [15] by employing a consistent direct power splitter based on BPF networks and a phase compensation network in the peaking path that can adjust the power dividing ratio according to the input impedance of carrier and peaking Pas, while, the peaking PA receives more power with lower impedance for better power handling.

On the other hand, the gain compression of carrier PA and gain expansion of peaking PA introduce an opposite third order IMD phase relation between the carrier and peaking PAs that has a detrimental effect on the linearity of DPA. Symmetric IMD3 of carrier PA can be suppressed by proper bias condition of peaking PA, that can compromise between the flat response of the nonlinear characteristics of amplitude modulation/phase modulation (AM/PM) variations and the efficiency enhancement. Furthermore, the precise harmonic load terminations can help to alleviate the IMD generation since, the IMD2 can be cancelled by short-circuited of second harmonic [16]. Typically bias buffer is required for handset PAs to set the bias point, however, the available bias headroom of HBT devices at very low supply voltage is limited due to the summation of two series PN junctions, that deteriorates the efficiency performance at bias point less than 3V.

Despite the fact that employing Class-AB for carrier PA with a resistive load at the fundamental and short-circuited of all harmonics can optimize the DPA linearity, Cripps [17] indicates that both the efficiency and output power have been degraded. For better harmonic suppression, Class-F operation mode uses both arms shunt stubs and series tuning line to minimize the simultaneous presents of current and voltage except at fundamental frequency across the targeted bandwidth. In fact, the Class-F/F^{-1} improves the efficiency and output power by inserting the second and third-harmonic traps realized by the extra control circuits (HCC) [18]. A fully matched microwave saturated DPA based on Class-F PA including HCCs and offset-lines to control the finite harmonic content according to the power levels is proposed in [19] that can deliver excellent efficiency of 53% PAE and 10W output power at 2.14GHz. However, it should be noted that, the harmonic manipulating for waveform-shaping at higher frequency is more challenging due to the low impedance of drain capacitor. On the other hand, the constant peak voltage waveform of continuous Class-F can be supplied by technologies with very large breakdown voltage, whilst the low voltage technologies used in handset PA diminish the output power densities. Furthermore, incorporating HCC enlarges the die size of the device and narrows the band frequency respond which is not desirable for RF front end module. The reported fully integrated 2μm GaAs HBT DPA in work [20], designed for handset application can regulates the second harmonic for higher efficiency across the band frequency. Such a lumped DPA can provide over 27% PAE and 23.6dBm output power across 2.2-2.8 GHz for WiMAX application.

For further improving the DPA efficiency, the work [21] employs HCC to resonate out the output capacitance of active devices by the inductances of bias lines. While, the short-circuited second harmonic has minor effects on linearity of DPA, it generates an in-phase second harmonic current at peaking PA that maximizes the half-sin current and results in a higher PAE. The proposed DPA employs an off-chip output matching network on the package model and a high pass π-type lumped matching technique as a direct input power divider, as well as it eliminates the offset lines and quarter-wave transmission line. The implemented DPA based on n InGaP/GaAs HBT at 1.9GHz has a chip area of $1.1\times 1.2\ mm^2$ and provides 25.1 dB gain, a PAE of 45% and output power of 27.5dBm . However, in practical DPAs base on HBT the maximum gain is not maintained and the nonlinear components will change as an exponential function. A Ka-Band DPA based on E-mode GaAs process using an input broadside coupler is reported in [22] that can provide 29% PAE at 6dB OBO and 26 dBm output power at 28 GHz. Fig. 4.3 shows the chip photo of DPA with the size of 2.2 × 1.3mm and the measurement results. The proposed integrated ultra-compact broadside coupler using stack-up as an input power divider can eliminate the offset-line at peaking path, since the coupler has an inherit phase shift.



a **b**

Fig. 4.3 a Layout of GaAs DPA MMIC, **b** Experimental results

Cripps [23], presented the conceptual analysis of even-order harmonics on improving the linearity using the transistors with nonlinear transconductance, that validates the superior linear performance of Class-J mode in DPA using only the second harmonic voltage enhancement technique in comparison with Class-F PA utilizing odd-order harmonics. Small-size HCC for second harmonic load can be realized by MIM capacitors and bond-wires at the drain of carrier and peaking PAs. To further reduced the MMIC DPA size, it is recommended that all the $\lambda/4$ lines at the impedance transformer give place to an equivalent low-pass π-type distributed network of series transmission line connected to shunt capacitors at each end [24]. Class-J PA offers a linear operation of fundamental frequency and a potential wideband and high efficient performance. The principle of Class-J mode of operation is to shift the phasing of the current and voltage waveforms. The overlap between drain voltage and current waveforms introduces a pure reactive component that can be utilized to terminate the second harmonic and bandwidth extension as well [25]. Harmonic tuning of Class-J PA with the purpose of engineering the voltage waveform is accomplished whiten the low-loss matching network, without requiring HCC. However, the overlap between waveforms degrades the efficiency improvement and can be reduced by an accurate second harmonic voltage component generation, while higher harmonics are short out. Employing a nonlinear gate-source capacitor at the gate node [26] or

nonlinear drain-source capacitor for shaping the voltage waveform, can balance the phase shift. The nonlinear capacitor changes the frequency components of drain voltage by generating odd-harmonics that increases the fundamental components and load impedance, subsequently, the output power and efficiency will be improved. Although, this approach shapes proper current and voltage waveforms, higher-order filters increase the PA implementation complexity. Also, the phase shift of the second harmonic voltage with respect to the fundamental voltage components affects the efficiency. The work [27] exploits the second harmonic tuning technique incorporating dual band active load modulation. This technique uses a reduced conduction angle of Class-C current injection to the drain node of main Class-J PA at the second harmonic frequency. The injected current poses an additional phase shifter and introduces the so-called Class-J2 PA that characterized by a band pass filter tuned for second harmonic and a phase offset between the main transistor' current and the injected current. However, the power injection at second harmonic provides the maximum 5% higher drain efficiency than that of Class-B PA because of DC power consumption of peaking PA. Furthermore, since the Class-C PA conducts current only at second harmonic, the output power at the fundamental frequency will be degraded. This topology has been modified by reducing the phase shift relative to the drain current of main PA and including the fundamental frequency injection as well, thus, the current flow to the load at fundamental will be contributed to deliver higher output power. State-of-the-art MMIC DPAs implemented on different technologies are summarized in Table 4.3.

Table 4.3 Performance comparison of mobile handset DPAs

Ref.	year	Technology	Freq. (GHz)	PAE % OBO	Gain (dB)	Pout (dBm)	Area (mm^2)
[15]	2010	2-µm InGaP/GaAsHBT	2.5-2.7	25	19	24.6	1.44
[22]	2017	E-mode 0.15-µm GaAs	28	29	12	26	2.85
[28]	2014	D-mode GaAs	23-25	20	12.5	30	4.29
[29]	2018	E-mode 0.15-µm GaAs	31.1	28	14	26.3	3.75
[30]	2019	0.15-µm GaAs	27-30	31	11.8	26.5	2.86
[31]	2017	0.15-µm GaAs	28.5	27	15	28	4.93
[32]	2014	0.15-µm GaAs	22.8-25.2	38	12.5	30	4.29
[33]	2017	0.13-µm SiGe	28	13.9	18.2	16.3	1.76
[34]	2018	90-nm CMOS	34	13.1	19.8	20.7	0.45
[35]	2020	130 nm SiGe BiCMOS	24-30	20	20	28	4.19
[36]	2019	130 nm SiGe BiCMOS	28	19.5	18.2	16.8	1.76

4.3 Load Modulation Amplifier Technique for Energy Efficient 5G Base Stations

The development of mobile generations has been significantly affected by the users requirements and expectations, where one of the main attracted feature is the data rate which has been significantly increased over the past 30 years, in addition to the voice services that was the main reason for implementing the wireless communications; video streaming,

browsing, gaming, etc, require high data rate that needs to be sent within a limited bandwidth. In this case, complex modulation schemes are used to utilise the available bandwidth effectively. However, the generated modulated signal will have an envelope which has a peak-to-average power ratio that force the amplifier to be back-off from the most efficient point (usually near to the saturation region) into a region that keeps the required linearity depend on each generation specifications, the following subsections will deal with the efficiency enhancement techniques and more details will be given to Doherty amplifier technique (load modulation technique)[37-39].

4.3.1 Efficiency Enhancements Techniques

Several techniques are used for improving the efficiency of power amplifier such as Out-Phasing technique (also it so called, linear amplification using non-linear devices, LINC), where there are two amplifier are working in their nonlinear region, however, the input amplitude for these two amplifier are constant and only their phases are changing. This method is mainly depending on the following trigonometric identity, so that, the signal linearity will be kept[40].

$$\cos(A) + \cos(B) = 2\cos\left(\frac{A+B}{2}\right).2\cos\left(\frac{A-B}{2}\right) \quad (4.1)$$

Another efficiency technique is the Envelope Tracking (ET), where the power amplifier supply voltage will be changed according the envelope of the input signal, in this case, the envelope of the baseband signal should be known, however, this technique suffers form the complexity and the bandwidth limitations.

The third technique is the Envelope Elimination and Restoration (EER), which was invented by Leonard Kahn, in this technique, there are two amplifiers, the first one is a highly linear amplifier used to amply the signal envelope, whereas the second amplifier is a non-linear amplifier used for amplifying a constant level of input signal. The main difference between the ET and EER is, for ET, the suppled voltage is adjusted to reduce the dissipated power (unused power), whereas in EER, the supply voltage is used for shaping the output waveform. The final technique is Doherty Technique which will be discussed in detail in the following subsection, where its main advantage is it does not require complex circuit and its simplicity.

4.3.2 Load Modulation Amplifier Principles

The Doherty amplifier operation is explained in detail in many materials; however, a short summary will be provided. W. Doherty, in 1936, came up with a new concept for combining two amplifiers outputs, Doherty used a quarter-wavelength transmission line and two tube amplifiers. The first amplifier is called carrier amplifier, whereas the second one called the peaking amplifier, where the first one operates all the time on the other hand, the second amplifier operates only during the load modulation region, at the same time, the bias condition of the carrier amplifier was as class AB, whereas the bias condition of the other amplifier was as class C amplifier. For the impedance inverter, a quarter wavelength transmission line was used as an to invert the impedance amount seen by the carrier amplifier as illustrated in Fig. 4.4.

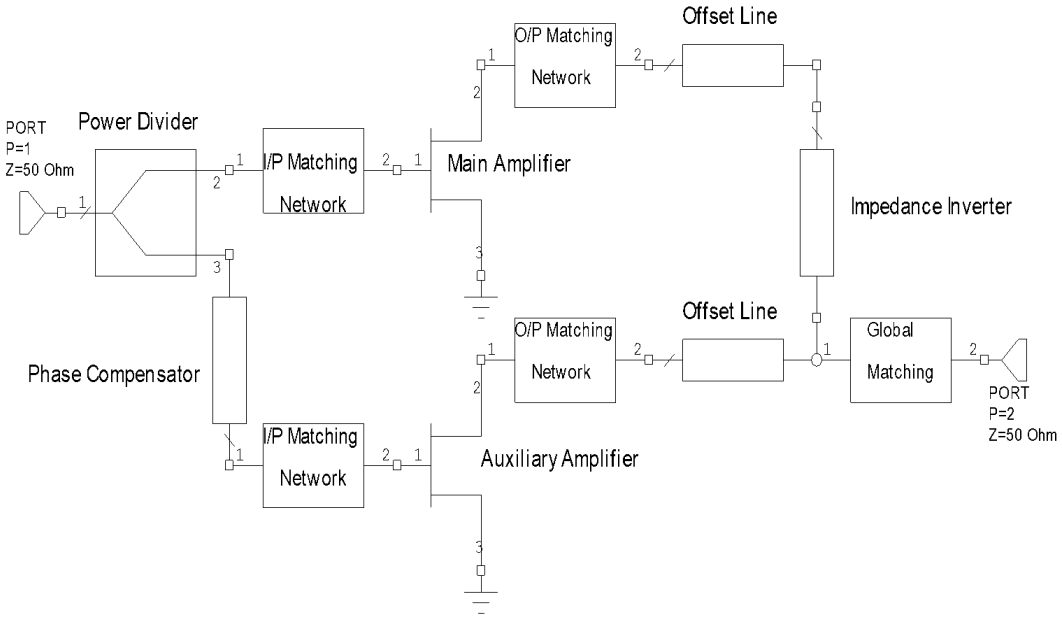


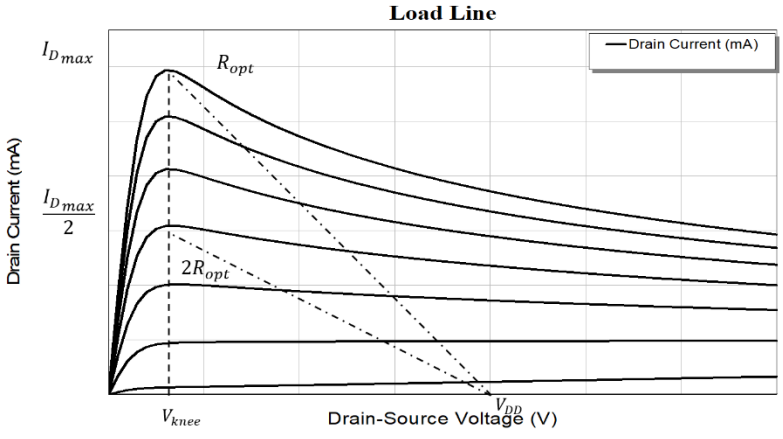
Fig.4.4 Load modulation structure

The characteristic of a transistor can be explored by applying different gate voltages and checking the behaviour of the drain current, as illustrated in Fig. 4.5. The power amplifier load impedance can be determined using (4.2) assuming that the drain parasitic of the transistor is disregarded:

$$R_{opt} = 2\frac{V_{dd}-V_{knee}}{I_{max}} \tag{4.2}$$

The Doherty amplifier relies on load modulation technique, where its operations can be summarized by two regions of operation assuming both amplifiers are connected to a load of 25Ω and matched to 50Ω.

Fig. 4.5 Load line of a transistor including self-heating effect.



At low input power region, the carrier amplifier is working, nevertheless, due to the quarter wavelength transmission line impedance inversion property, the impedance seen by the carrier amplifier is 100Ω, which is double the optimum load seen by the carrier amplifier, so the first peak efficiency will be seen due to the carrier amplifier saturation.

At the load modulation region, the Doherty operation will be clear, where a current will be injected, to the summing node, by the peaking amplifier, so two current will be contributed to the same load. There will be a reduction from a 100Ω to 50Ω of the impedance seen by the carrier amplifier depending peaking amplifier current. However, the saturation of the carrier amplifier continues until its maximum power.

4.3.3 Efficient Load Modulation Amplifier Design: 5G Case Study

One of the main challenges in designing the current and future power amplifiers is the size in addition to the other key requirements that are essential for each standard. In this design, a compact load modulation amplifier that can be used for 5G base station will be presented. As mentioned in the previous section, the normal Doherty amplifier can be designed using two amplifiers with the quarter-wave length transmission line that acts as impedance inverter. Fig. 4.6 shows the designed 5G power amplifier, where this design represents a compact power amplifier و where there is not quarter wave-length transmission line between the two amplifiers, the main idea of the design is to create a virtual transmission line that has been embedded in the design. This amplifier works for sub 6-GHz bands specifically, at a centre frequency of 3.6 GHz with a bandwidth of 400 MHz. the amplifier consists of two transistors, which are CG2H40025 and CG2H40045 transistors for the main and the peaking amplifier respectively. The main amplifier can deliver a maximum power of 25W, whereas the peaking amplifier can deliver a power of 45W. so both amplifiers can provide a peak power of 70W.

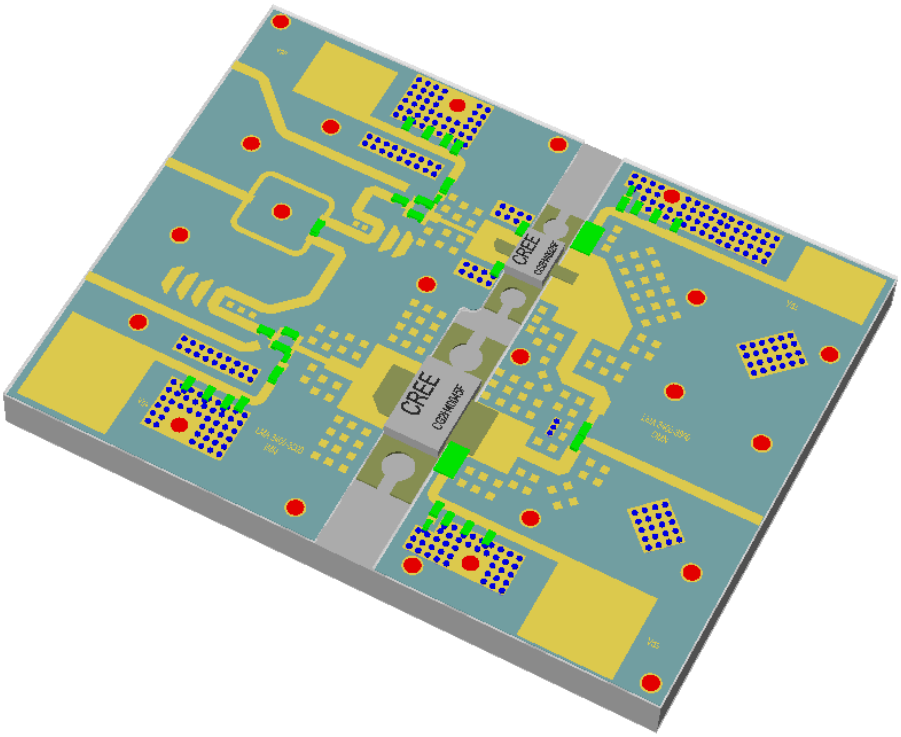


Fig. 4.6 Compact load modulation design.

In simple words, each amplifier characteristics will be investigated in detail including small and large signal measurements, the procedure for designing such amplifier can be summarised as following: For the main amplifier, since it works all the time so the overall

efficiency will be determined by the main amplifier performance, at the back-off, the main amplifier needs to see an impedance that provide the highest achievable efficiency at the back-off, after that, as the peaking amplifier starts injecting current into the summing point the amplifier modulated impedance needs to be an impedance that can provide the highest achievable power [38].

On the other hand, the peaking amplifier needs to see an impedance that can provide the maximum power that can deliver, at the same time, it should not load or change the impedance of the main amplifier at the back-off region.

Fig. 4.7 shows the performance of the designed amplifier, it can be seen that the amplifier delivered an average gain of 10.5 dB with a peak power of 48 dBm, at the same time, it can be noticed that the amplifier achieved an average peak efficiency of 70% with a back-off efficiency of 50% at 40 dBm output power. One of the main challenges in this design was the circuit design complexity, where too many parameters are required in designing each amplifier matching networks [41].

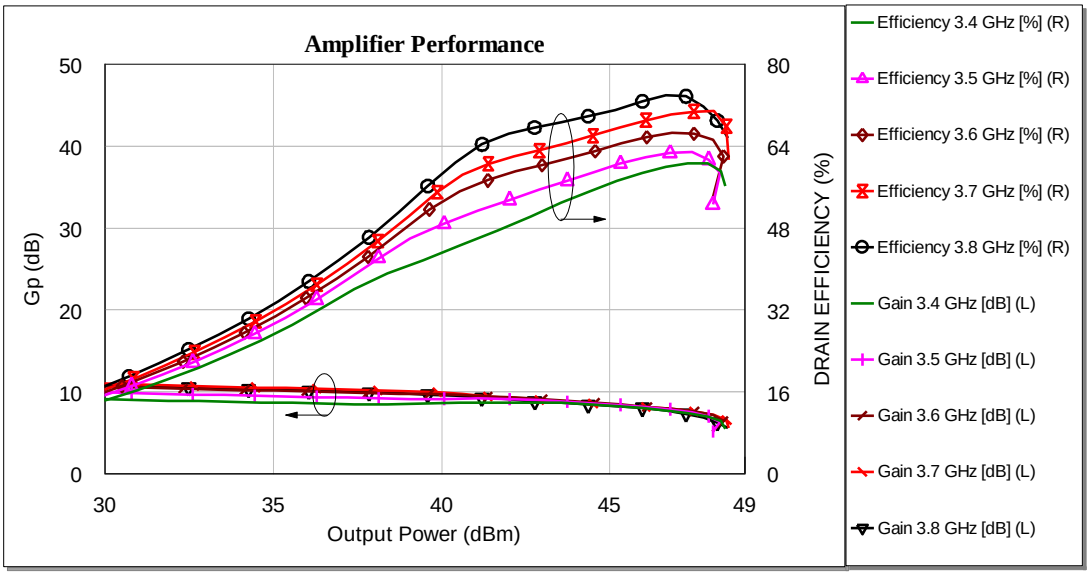


Fig. 4.7 Designed load Modulation Amplifier

4.1.1 Differentially-fed Filtering Antenna Structures for Recent Wireless Systems

With the fast development of current wireless communication systems, fourth-generation (4G) (2.6-2.7 GHz) and sub-6 GHz fifth-generation (5G) bands have been proposed for several RF planar circuits including power amplifiers, filters and antennas [42], [43]. RF components using differentially-fed ports are in high demand for 4G and 5G applications. Also, differential-fed RF structures offer promised characteristics for 5G applications and can provide some important and attractive properties [44], [45]. The main essential advantages for differentially fed RF circuits are:

- Multi-functional property.
- High filtering level to the interference signals
- High common-mode suppression

- High roll-off skirt selectivity.
- Wide-band harmonic rejection
- Low radiated power loss.
- Low cross-polarization.

Nowadays, differentially fed components with dual-polarization performance have been commonly used to improve the radiation characteristics of the entire RF front end applications [46]. Several differentially driven antenna configurations have been proposed, such as uni-planar microstrip antennas [47], [48], magneto-electric multi-dipole structures [49], cavity-backed antennas [50]. In [46], a differentially-fed microstrip antenna fed by orthogonally-phased ports with 0^0 and 180^0 signals was reported. The antenna has a high realized gain of about 11 dBi and low cross-polarization of -18 dB in the E-plane. It also provides a 10 dB fractional bandwidth of 16% at 13.2 GHz for Ku-band systems. Apart from the ordinary differential-fed planar structures, the configurations presented in [47] and [48] apply a folded plate pair to construct the differentially-driven signals. The reported antennas have a stable maximum gain of about 9 dB at the center frequency and over the entire bandwidth which leads to the high linearity in the radiations and symmetrical characteristics at the dual mode of operation. A differentially excited microstrip antenna with a maximum realized gain of 9 dBi and a 140 MHz impedance bandwidth was reported. In [49], the introduced antenna can work with several systems including other RF differentially-fed/balanced elements, energy harvesting, radiofrequency identification (RFID) applications.

On the other hand, planar filter-antenna integrations (filtering antennas) can also be used to improve the entire performance of the RF front end systems [51], [52], [53]. The integrated design of a filter antenna combination utilizing a multi-layered-substrate was reported for recent and future RF front end systems including 5G applications. The configuration is a third-order ring open-loop resonator connected to a T-shaped strip radiator. The multi-layered technology is applied to achieve a compact size structure. The filtering antenna design uses a Rogers RT5880 dielectric material in the middle layer with a permittivity of 2.3 and thickness (h) of 0.581 mm. The designed filtering antenna (filtenna) works on 2.5 GHz and has a fractional bandwidth of about 3.0% and a realized gain of about 2.1 dB at the center frequency. Although the design has a compact size, it has a complex configuration due to the use of a multi-layer technology. While in [52], the proposed filtenna was tracked similar design procedure and obtained good scattering parameter and radiation results with a circular polarization performance. Nevertheless, the reported design utilized different design techniques using the substrate integrated waveguide structure.

Reconfigurable and Tunable Filtering Antenna Structures

By integrating the filtering antenna with the reconfigurability/tenability function, more attractivie combination with efiicient performance can be obtained [54], [55]. Conversely, this will also lead to some more challenges in simulation, fabrication and measurement settings. Two PIN-diodes and four varactor diodes are used in the reconfigurable/tunable design in [54]. Although this requires a more complicated configuration, it also leads to a very small size structure with good filtering performance and flexible tuning capability. In [55], a tunable/reconfigurable bandpass characteristics were obtained by implementing a filtering antenna structure. The design offers a high degree of freedom to control the scattering

parameters and the radiation patterns using a small size layout. Therefore, this multi-function design has been proposed for several 5G front end systems. In addition, the main types of switching techniques that can be used in the biasing circuits of the tunable/reconfigurable RF are explained in table 4.4 below [56]:

Table 4.4 RF reconfiguration techniques [56].

Properties	PIN Diode	Varactor	RF MEMS	Photoconductive
Speed (μsec)	$1–100 \times 10^{-6}$	0.1	1–200	3–9
Quality factor	50–85	25–55	86–165	-
Voltage (V)	3–5	0.1–15	20–100	1.8–1.9
Current (mA)	3–20	1–25	0	0–87
Power (mW)	5–100	10–200	0.05-0.1	0–50
Temperature sensitivity	Medium	High	Low	Low
Cost	Low	Low	Medium	High
Loss at 1 GHz (dB)	0.3–1.2	0.5–3	0.05–0.2	0.5–1.5
Fabrication complexity	Commercially available	Commercially available	Low fabrication complexity	Complex

Differentially-fed Reconfigurable Filtering Antenna Design:Configuration

Fig. 4.8 illustrates the configuration of the designed differential-fed reconfigurable planar filter-antenna. The designed microstrip filtering antenna consists of circular dick radiating patch with a diameter (D = 30mm) and pair of differential feeding probes. It should be noted that loading the open ring slots with different configurations to the radiating element can reshape the distribution of the surface current or generate another frequency mode of operation. Thus, the structure size can be reduced and the entire performance will be modified and developed.

In this design, four open-ring resonators are etched on the radiating layer to obtain broadside patterns with nulls at both sides of the passband transmission, resulting in a filtering performance with a wide-stopband suppression. The total circumference of each ring is about half the wavelength of the center frequency ($\lambda/2$). To achieve the reconfigurability property, two PIN diodes are placed on the ground layer to control the current distribution and, therefore, providing two resonance frequencies for 4G and 5G spectrums. Just to prove the design topology, practical PIN-diode switches, SMP1320-079 from Skyworks Solutions Inc, were utilized each with a size of 1.5x0.7 mm^2. In computer simulation technology, CST microwave studio, these diodes are modeled with a lumped element circuit which presents 1.0 Ω as the resistance value of the PIN-diode in the ON configuration (forward basing) and 0.5 pF as the capacitance value in the OFF configuration (reverse biasing).

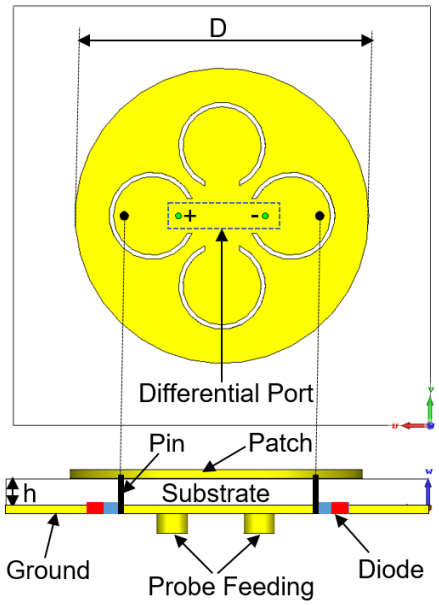


Fig. 4.8. Top and side views of the designed reconfigurable filtering antenna

Moreover, in the OFF configuration, the PIN-diode can be designed as a series capacitance with a parasitic inductance as shown in Fig. 4.9. While, in the ON configuration, the PIN-diode can be modeled as a series resistance with a parasitic inductance. The parasitic inductance generated due to the package behavior of the PIN-diodes. The model equivalent circuit parameters can be obtained from the manufacturer's data where L_S = 0.7 nH, C_T = 0.3 pF and RS = 1 Ω. As the value of Rp is higher than the reactance of C_T, it can be neglected in the equivalent circuit.

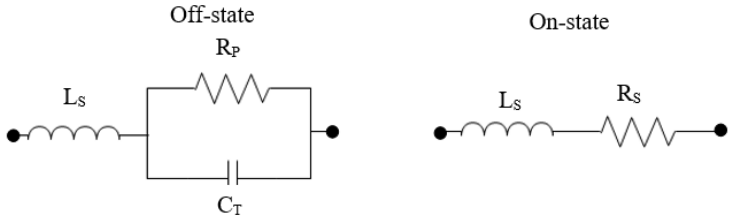


Fig. 4.9. RF equivalent circuit model for the PIN-diode

- **Filtering antenna analysis and performance**

Reconfigurable filter-antenna integration (filtenna) characteristics in regards to the reflection coefficients and peak realized gain for both diodes configurations (ON and OFF) are presented in Figs. 4.10 and 4.11, respectively. The gained performance proves that the filtering antenna resonances at 2.6 GHz and 3.5 GHz with peak realized gain 5dB and 7.5dB at OFF and ON configurations, respectively, with impedance bandwidth 100 MHz.

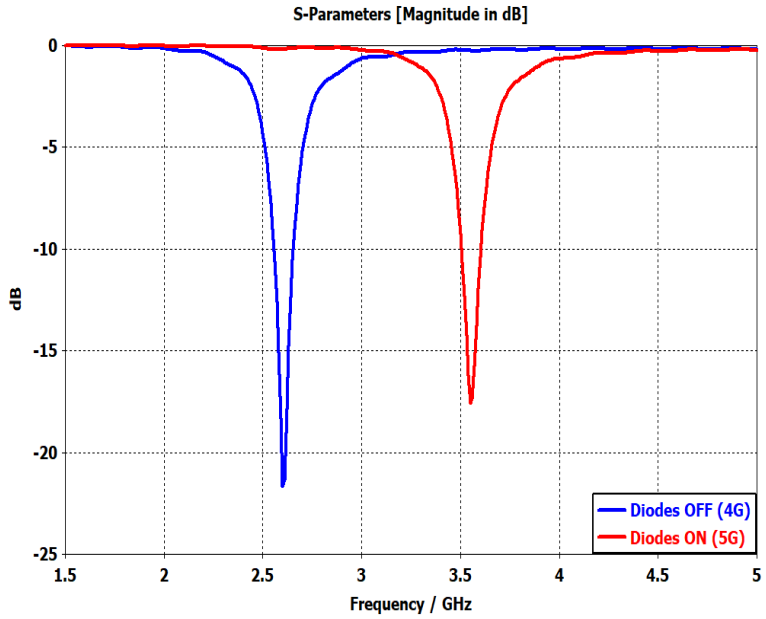


Fig. 4.10. S-parameter results of the proposed reconfigurable filtering antenna

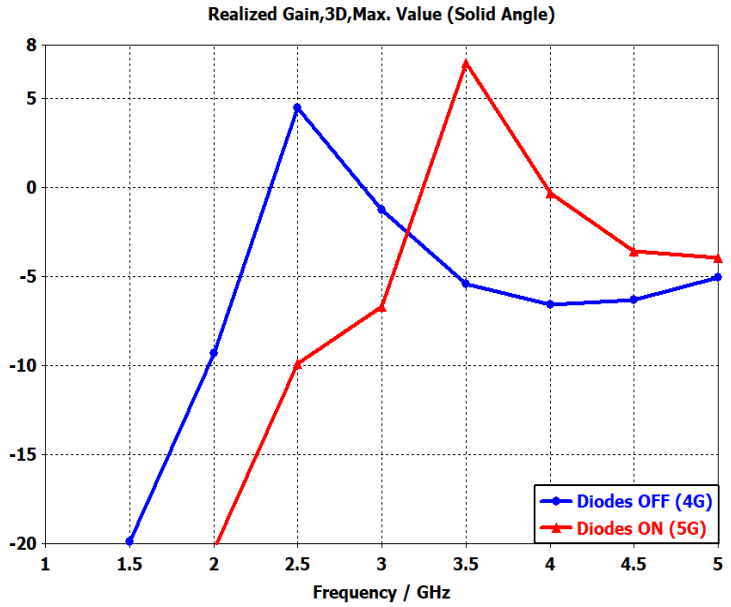


Fig. 4.11 Realized gain results of the proposed reconfigurable filtering antenna

Also, Figs. 4.12 and 4.13 show the radiation-pattern characteristics for the proposed reconfigurable filtering antenna at diodes-OFF and diodes-ON configurations, respectively. At diodes-OFF configuration (Fig. 4.12), the operating frequency 3.6 GHz and main lob magnitude 8.13 dBi. The angular width (3 dB) 73.50 and side lobe level -23.8 dB. On the other hand, at diodes-ON configuration (Fig. 4.13), the operating frequency 2.65 GHz and main lob magnitude 7 dBi. The angular width (3 dB) 86 and side lobe level -17 dB. Fig. 4.13 shows the 3D-simulation results for radiation-pattern directivity that correspond to the two configurations of diode switch in both forward and revers bias.

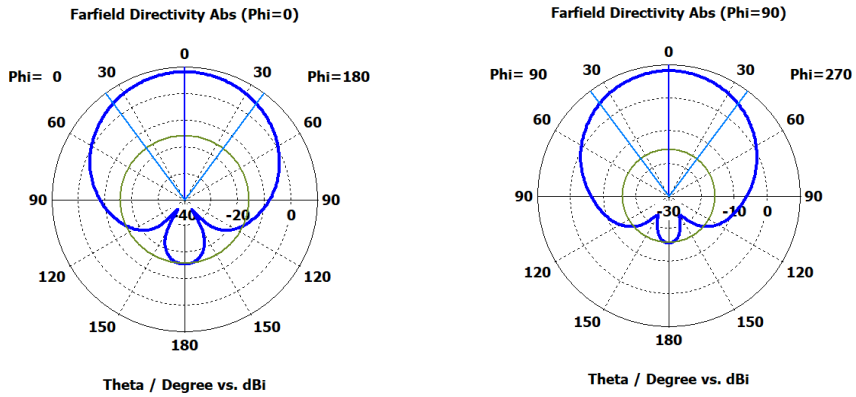


Fig. 4.11 2-D Radiation pattern characteristics at diodes-OFF configuration

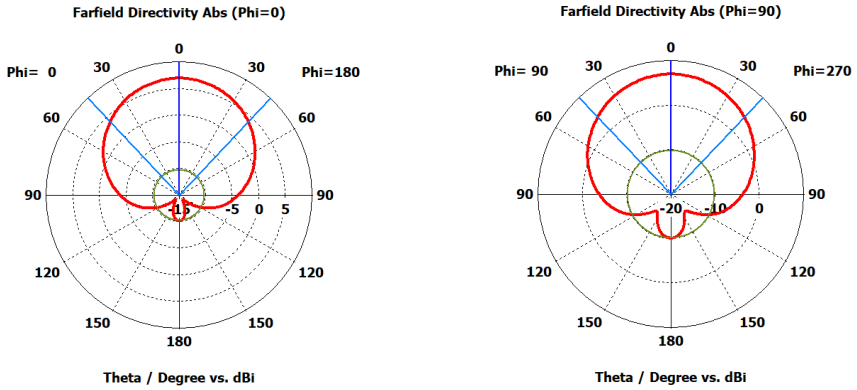
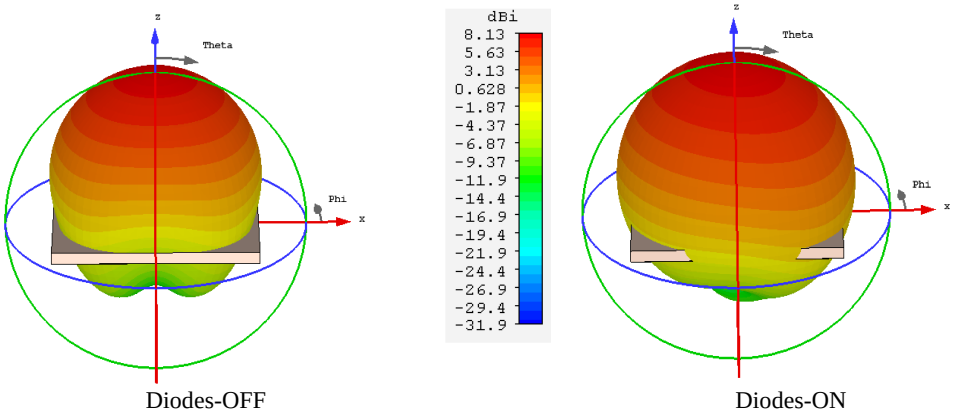


Fig. 4.12 2-D Radiation pattern characteristics at diodes-ON configuration



Diodes-OFF Diodes-ON

Fig. 4.13 3-D Radiation pattern characteristics of the proposed filtering antenna

4.5. Compact Filtering Antenna for Phased Arrays targeting 5G mmWave FDD backhaul

The 5G access network targets millimeter wave (mmWave) frequencies for the support of the high data rates required by the Enhanced Mobile Broadband services. This in turn leads to a huge densification of the cellular base stations to overcome the high propagation losses of mmWaves. This densification gives the name to hyper dense scenarios.

On the other hand, the 5G fronthaul/backhaul network is expected to be fiber-optic based. However, a fully optical network is not feasible in these hyper dense scenarios, first due to the

high cost that such deployment would represent, as well as to fiber installation restrictions. These restrictions may be natural but also due to local environmental policies. Finally, the deployment time represents also a big disadvantage compared to its counterpart: radio links. Therefore, this leaves enough space for current and future point-to-point wireless links. As an improvement over current architectures, the new wireless fronthaul/backhaul network is expected to be reconfigurable to satisfy the dynamic nature of the mobile traffic. Phased Array Antenna (PAA) in the backhaul equipment is a promising solution to respond not only to this need, but also to provide the equipment with the ability to automatically recover the link when misalignments occur, increasing its availability. However, there are some challenges to overcome before using it in a commercial equipment [57] , [58], especially those that use frequency division duplexing (FDD) for transporting bidirectional data streams.

The present study focuses on designing a compact filtering antenna to serve as the base radiation element for a PAA expected to be placed in a SIAE MICROELETTRONICA backhaul equipment, which uses FDD as a duplexing technique and works at 25 GHz.

4.5.1 Phased Array Antenna Architecture for FDD Applications

SIAE's equipment as well as most wireless backhauling equipment uses FDD for transporting bidirectional data streams. It means that two different frequencies are used for transmission (Tx) and reception (Rx). In the current architecture of the equipment, the Tx and Rx chains are connected to the antenna through a diplexer, ensuring 65 dB of isolation between chains, as shown in Fig. 4.14a. In the 25 GHz band the lower frequency band spans from 24.549 GHz up to 24.997 GHz, while the upper frequency band ranges between 25.557 and 26.005 GHz.

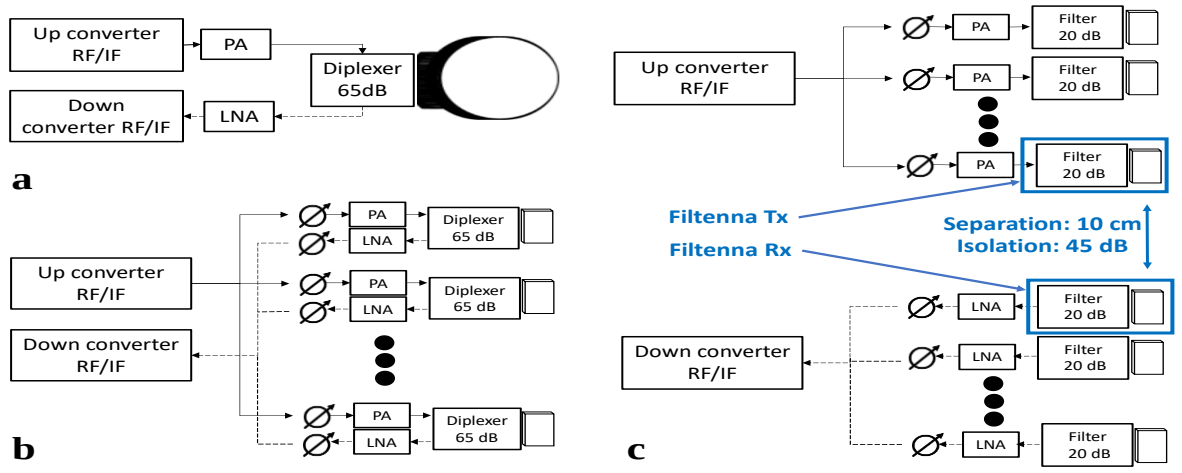


Fig. 4.14 Front-end architectures for backhaul equipment using FDD duplexing: **a** Current architecture, **b** Architecture with a PAA using a single antenna array, **c** Architecture with a PAA using two antenna arrays, one for Tx and the other for Rx. PA is Power Amplifier in the Tx chain. LNA is Low Noise Amplifier in the Rx chain

In a first attempt, one could think of extrapolating this architecture to that of a PAA, as shown in the Fig. 4.14b. Note that in this architecture it is still necessary to guarantee 65dB of isolation between the Tx and Rx chains. Also note that according to the antenna array theory [59], the separation between adjacent antennas should be around half of wavelength (~ 6 mm at 25 GHz) to minimize unwanted grating lobes which appear especially when electronic beam steering is

applied. Then, designing this highly selective diplexer, that is easily integrable with the rest of the PAA components, and in such a small space, represents quite a big challenge. Consider that the current diplexer is the union of two 8-pole waveguide bandpass filters with physical dimensions in the order of centimeters. For these reasons, the architecture that seems most viable is the one shown in Fig. 4.14c. With two different arrays, one for Tx and other for Rx, a natural isolation appears. This isolation is dependent on the separation distance between the arrays and on any absorbing material or structures placed between them. By initially neglecting the latter possibility, full wave simulations of two arrays of patch antennas at different distances, show that a reasonable separation distance of 10 cm guarantees a natural isolation of around 45 dB between the Tx and Rx chain. However, 20 dB are still missing to comply with equipment specification. Consequently, a filter with lower order is still required between the antenna and the active component (i.e. LNA or PA) in both Tx and Rx with the aim to provide the remaining 20 dB of isolation. For better integration, two Filtennas (filter + antenna) have been designed to provide this isolation, one for Tx the other for Rx chain. Although it may appear that the filter is only needed on the Tx chain to remove the undesired wideband noise from the Tx signal that would cancel the low-level received signal in the Rx band, the sensitive Rx front stages must also be protected from the high-power Tx signal, though out of Rx band, in order to avoid saturation of the LNA and consequent distortion of the received signal. Thus, a Filtenna in each chain is needed. Note that the Filtennas are now the base radiation element of the PAA and since the design procedure is the same for both, the following section will focus only on the Tx frequencies.

4.5.2 Filtenna Design Leveraging Filter Synthesis

There are different methods to design a Filtenna [60]. First, we have the traditional one, in which the antenna and filter are designed separately and then a matching network is designed to connect them, like the work in [61]. Second, a co-design approach can be followed, in which a filter response is obtained by embedding filtering structures into different parts of the antenna (e.g. slots, splint ring resonators), trying not to alter the radiation performance, like the work in [62], [63]. The main disadvantage of the first approach is that the matching network could introduce additional losses to the circuit and increase the footprint of the Filtenna. In the second approach, the main issue is that the design procedure is mainly based on full-wave optimization, which is time consuming. Finally, a filter synthesis-based approach can be also followed, in which the antenna can behave like the last stage of the filter (i.e. resonator and load conductance or only the load conductance), like the works detailed in [64] and [65]. This last approach has the advantage that the antenna is part of the filter, therefore there is no need of a matching network. Also, mostly all the design procedure is systematic, also supported with full-wave optimization at the end. Additionally, it allows to know in advance the expected S_{11} with a fair precision. For these reasons, this work is dedicated to this approach.

Within the last approach, two techniques can be followed: a lossless synthesis or a lossy one. The first one assumes that all the resonators of the filter are lossless, which fits quite well in air-filled waveguide filters. The second instead considers the lossy nature of the resonators when they are implemented in dielectrics. In this work, the Filtenna was designed in dielectric (PCB technology) because of the available space for the design and for a better integration with the rest of the equipment. Thus, a lossy technique seems the most adequate.

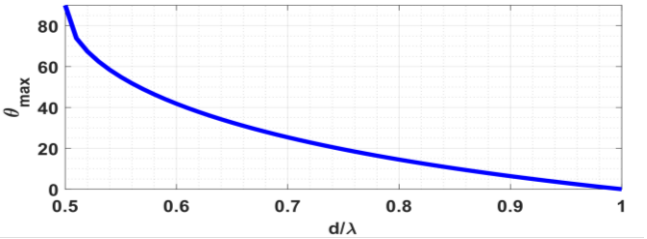


Fig. 4.15 Maximum steering angle (θ_{max}) without grating lobes versus normalized separation distance (d/λ) between radiation elements in a uniformly-spaced linear antenna array. $\theta_{max} = asin\left(\frac{\lambda}{d} - 1\right)$ [3]

In general, lossless techniques work very well for Filtennas, in fact most of the previous synthesis-based works were done with this technique, even in PCB. However, since the lossless assumption does not agree with the real resonators (lossy), the flatness of the transmission parameter (gain in the Filtenna case) in the passband is lost. In contrast, when lossy synthesis is used, flatness of the gain in passband is preserved. To show the differences, the two techniques are discussed in this work. To the authors' knowledge, the work presented here is the first lossy synthesis-based design of a Filtenna in the literature.

Finally, let us summarize the design requirements and constraints. Since the design is focused on Tx, the passband extends from 24.549 GHz to 24.997 GHz. In the stop band, extending from 25.557 GHz to 26.005 GHz, the gain must be 20 dB less than in the passband. The return loss (RL) should be better than 10 dB. Since the target is a PAA, the size of the Filtenna directly affects the spacing between the radiation elements; this in turn affects the maximum angle at which the main beam can be steered without the appearance of undesirable grating lobes [59], as shown in Fig. 4.15. Note that Filtenna size is constrained to be less than a wavelength ($\lambda\sim$ 12 mm at 25 GHz), otherwise, grating lobes would appear even without beam steering. Of course, the closer to $\lambda/2$ the better.

4.5.2.1 Lossless Filter Synthesis Technique

The procedure starts by synthesizing a lossless filter prototype that fulfills the specifications described above by using any of the methods available in the literature [66]. A third-order all-poles Chebyshev filter fulfills these specifications with RL = 20 dB in the passband. The de-normalized synthesized circuit is shown in Fig. 4. a. Because of the small space available, a vertical stacked architecture was exploited [67], [68] as shown in Fig. 4. b. Each resonator was physically implemented with a Substrate Integrated Waveguide (SIW) cavity. Note from Fig. 4. a that all the cavities must have the same resonant frequency (F = 24.772 GHz) and they were initially dimensioned by using the well know design formulas for SIW cavities [69]:

$$W_{eff} = W_{siw} - \frac{d^2}{0.95\,s}, \quad L_{eff} = L_{siw} - \frac{d^2}{0.95\,s}, \quad F_{TEmp0} = \frac{c}{2\sqrt{e_r}}\sqrt{\left(\frac{m}{W_{eff}}\right)^2 + \left(\frac{p}{L_{eff}}\right)^2}, \quad (4.3)$$

where d is the via diameter, s is the vias separation and $Wsiw$, $Lsiw$ are the cavity dimensions and $m=p=1$ is used to address the TE110 resonant mode.

The coupling between resonators (inverter J_i in the equivalent circuit) were physically implemented with slots. The closer the coupling slots are to the edge of the SIW cavity, the greater the coupling. To determine the position of the slots, the relationship between the dimension d_S (Fig. 4.16 d) and the coefficient of coupling J_i (Fig. 4. a) was computed. This

relationship is shown in Fig. 4.17 17 a. This curve was made by coupling two SIW cavities, varying d_S and calculating the coefficient J_i using the Eq. 4.2 for each variation, where f_1 and f_2 are the two peak frequencies in the S_{21} parameter. The coupling with the source and load must be as low as possible, for this procedure to work properly [70].

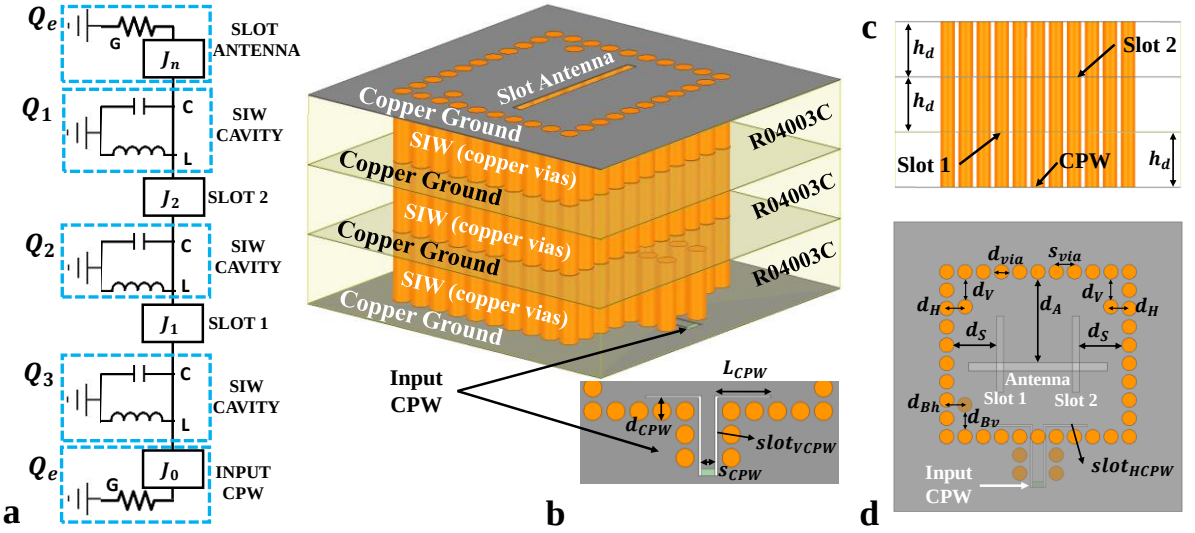


Fig. 4.16 **a** Synthesized lossless filter highlighting the relations with the designed Filtenna. **b** Designed Filtenna, 3D view. **c** Designed Filtenna, 2D front view. **d** Designed Filtenna, 2D top view. Circuital values: $C = 6.425\,pF$, $L = 6.425\,pH, G = 1\,\Omega^{-1}$, $J_{0,n} = 0.1456$, $J_{1,2} = 0.01863$, $Q_e = 47.19$, $Q_{1,2,3} = \infty$. Physical dimensions in mm: $d_{via} = 0.4$, $s_{via} = 0.506$, $d_V = 0.565$, $d_H = 0.512$, $d_S = 1.188$, $d_A = 2.303$, $d_{Bv} = 0.684$, $d_{Bh} = 0.5$, $slot_{VCPW} = 0.06$, $slot_{HCPW} = 0.042$, $s_{CPW} = 0.3$, $L_{CPW} = 1.16$, $d_{CPW} = 0.491$, $h_d = 1.524, h_{ground} = 0.017$, Antenna Slot: 3.85 x 0.235 . Coupling Slots: 2.1 x 0.23

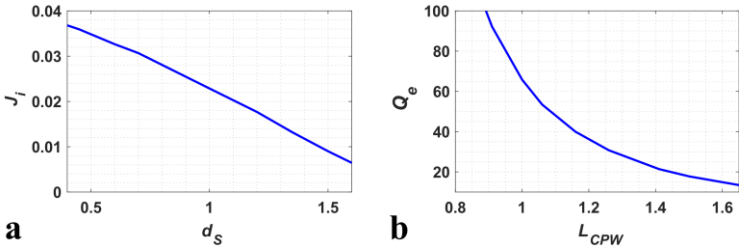


Fig. 4.17 **a** Relation between the dimension d_S and the coupling J_i. **b** Relation between the dimension L_{CPW} and the quality factor Q_e

$$J_i = \frac{{f_2}^2 - {f_1}^2}{{f_2}^2 + {f_1}^2} \tag{4.4}$$

To design the external quality factor (Q_e) at the input port, a 50 Ω coplanar waveguide (CPW) with two perpendicular slots was designed as shown in Fig. 4.16 b. By varying the dimensions L_{cpw} and d_{CPW} in a short circuited SIW, the Q_e can be computed by [70]:

$$Q_e = \frac{2.\pi.f_0.\tau_{s11}(f_0)}{4} \tag{4.5}$$

where f_0 is the peak of the group delay of the S11 parameter and $\tau_{s11}(f_0)$ is the group delay at f_0. The relation between the dimension L_{CPW} and Q_e is shown in Fig. 4.17 17 b. The dimension d_{CPW} does not affect greatly Q_e, but it can be used for fine tuning.

Note from Fig. 4.16 a that the circuit is symmetric, therefore the physical Filtenna must also be so. This implies that the scattering parameter response of the input part (CPW + SIW) should be the same as the output part (SIW + Antenna slot). Therefore, since the input part is already designed, the output part must be optimized to behave in frequency as the input part. Also note that in both input and output SIWs, there are vias inside the cavity. These vias help to tune the cavities in the central frequency. This is because the slots (Antenna, CPW) make these cavities electrically bigger in comparison with the central cavity.

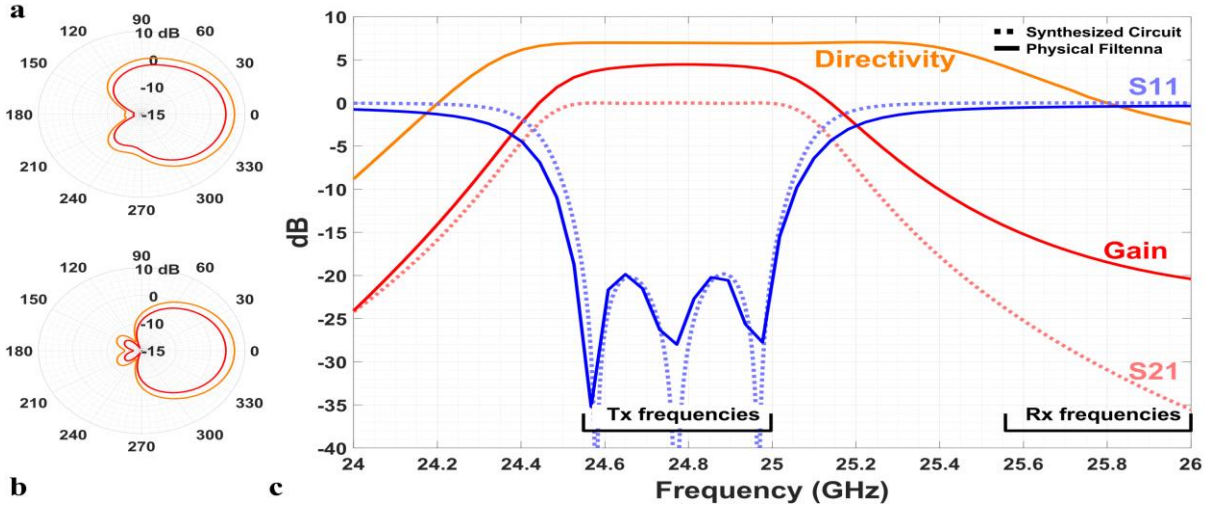


Fig. 4.18 Circuit and Full-wave simulations of the designed Filtenna. Radiation pattern at central frequency 24.772 GHz: **a** (cut $\emptyset = 0°$), **b** (cut $\emptyset = 90°$). **c** Scattering parameters of the synthesized lossless filter in dotted lines. S11, gain and directivity response of the designed Filtenna in solid lines

To the best of the authors' knowledge, the above procedures provide a very good initial design that would require only a few full-wave optimization steps. Final dimensions of the Filtenna are written in the caption of Fig. 4.16 a. The frequency response of both equivalent circuit and physical Filtenna is shown in Fig. 4.18 c. Note the good correlation between the S_{11} of the synthesized circuit and the full-wave simulations of the physical Filtenna.

Focusing instead on the transmission parameter, note the flatness of the S_{21} of the synthesized lossless circuit throughout the bandpass, in contrast with the Filtenna gain with 4.46 dBi in the center frequency and 3.73 dBi at passband edges. This is because of the losslessness assumption at the beginning of the design, which is not true in the physical Filtenna. The difference between the gain at the central frequency of Tx and at the beginning of the Rx band is 19 dB approximately, close enough to the desired (20 dB). To increase the isolation, the filter order could be increased, but this would also imply an increase in the complexity of the Filtenna (additional layer in the stack-up) and a decrease in the antenna gain due to the increase in insertion loss. A better option would be to add complementary split ring resonators between the Tx and Rx antenna arrays to get further isolation [71].

Figures Fig. **4.** a-b shows the $\emptyset = 0°, = 90°$ cuts of the antenna radiation pattern, the directivity and gain are about 6.96 and 4.46 dBi at boresight, respectively. Finally, according to the Filtenna size, it is possible to get 6 mm ($\lambda/2$) of separation between radiation elements in the PAA. Therefore, according to Fig. 4.14, it would be possible to perform beamsteering up to $\pm 90°$ in both azimuth and elevation planes without the appearance of grating lobes.

4.5.2.2 *Lossy Filter Synthesis Technique*

The main difference with respect to the previous design lies in the synthesis technique. Here we have used the lossy synthesis described in [72]. The procedure starts by computing the rational polynomials defining a desired transmission and reflection characteristic $S_{11}(s)$, $S_{21}(s)$ and $S_{22}(S)$, using for example the procedure of [73] to get Chebyshev filtering response. Then, the all the numerators N_{11}(s), $N_{21}(s)$, and $N_{22}(s)$ are scaled with a suitable constant, according to the desired or expected insertion loss (-2dB in the current design). Then, by using the even- and odd-mode decomposition, $N_{11}(s)$ and $N_{22}(s)$ are recomputed so that $S_{11}(\infty) = S_{22}(\infty) = 0$, which imposes a degradation to 12dB of return loss in the passband. All the polynomials of all these three steps are detailed in Table 4..

Table 4.5 Polynomials throughout the process of the lossy filter synthesis.

	$N_{11}(s) = N_{22}(s)$	$N_{21}(s)$	$Denominator\ (s)$
$Lossless\ Chebyshev\ Polynomials\ (RL = 22dB)$	$s^3 + 0.75s$	-3.1374	$s^3 + 2.5881s^2 + 4.0990\,s + 3.1374$
$Scaling\ -2$ dB	$0.7943s^3 + 0.5957s$	-2.4921	
$Force\ S_{11}(\infty) = S_{22}(\infty) = 0\ (RL = 12$ dB$)$	$s^3\ (1 + 0.002i) + s^2\ (0.532 + 0.006i) + s\ (1.439 + 0.009i) + (0.645 + 0.007i)$	-2.4921	

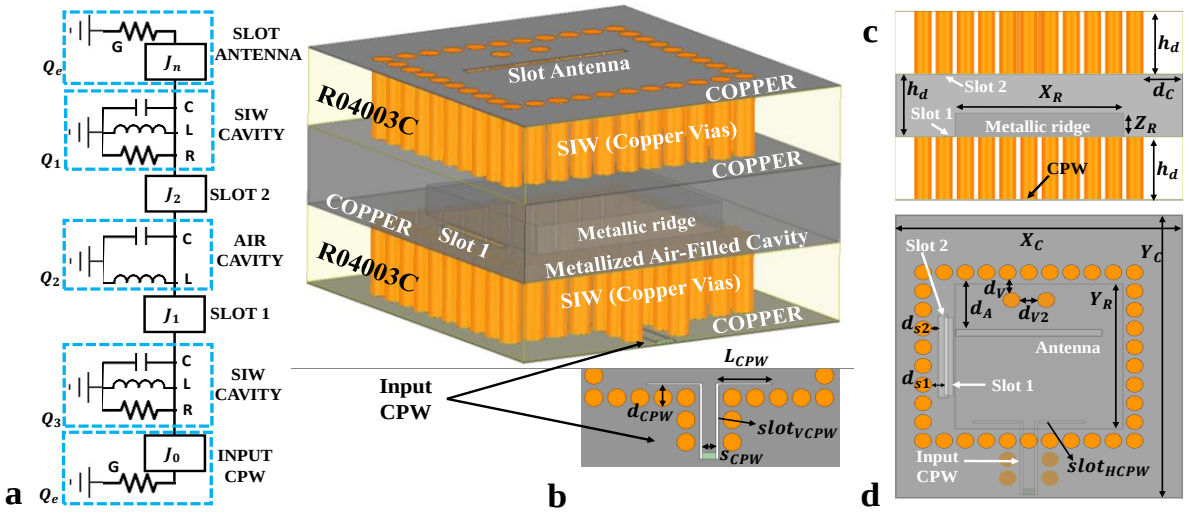


Fig. 4.19 a Synthesized lossy filter highlighting the relations with the designed Filtenna. **b** Designed Filtenna, 3D view. **c** Designed Filtenna, 2D front view. **d** Designed Filtenna, 2D top view. Circuital values: $C = 6.425\,pF$, $L = 6.425\,pH$, $R = 207.8\,\Omega$, $G = 1\,\Omega^{-1}$, $J_{0,n} = 0.1363$, $J_{1,2} = 0.01991$, $Q_2 = \infty$, $Q_e = 53.8$, $Q_{1,3} = 207.8$. Physical dimensions in mm: $d_{via} = 0.4$, $s_{via} = 0.5$, $d_V = 0.439$, $d_{V2} = 0.42$, $d_A = 1.317$, $d_{S1} = 0.3$, $d_{S2} = 0.166$, $slot_{VCPW} = 0.06$, $slot_{HCPW} = 0.056$, $s_{CPW} = 0.3$, $L_{CPW} = 1.099$, $d_{CPW} = 0.276$. $X_R = 3.968$, $Y_R = 3.872$, $Z_R = 0.57, h_d = 1.524, h_{cooper} = 0.017$. Antenna Slot: 3.451 x 0.187. Coupling Slot 1: 2.1 x 0.205. Coupling Slot 2: 2.194 x 0.225

With these new polynomials, the normal coupling matrix synthesis described in [66] can be applied. The final de-normalized synthesized circuit is shown in Fig. 4. a. Note that in

the resulting circuit, the first and last resonator are lossy, but the middle one is lossless. It is possible to make lossy the central resonator (to have all the cavities in the same dielectric) by matrix rotations, but this leads to obtaining lossy couplings, which are physically implemented by adding resistors which is not desired in our design for integration reasons.

To physically implement this circuit as faithfully as possible, the middle cavity needs to be lossless: it can be achieved by an air-filled cavity (approximately lossless). New techniques have emerged to manufacture these cavities in PCB technologies, such as the one described in [74]. According to [74], the air-filled cavity can be modelled by a traditional waveguide cavity since the manufacturing procedure consists of digging the dielectric and then metalizing the walls. The first issue that arises in the design procedure is that the size of the air cavity is in the order of λ which considerably limits the beam steering capabilities as detailed above. Therefore, to reduce the size, a metallic ridge is inserted inside the cavity. This ridge makes the cavity electrically bigger, which allows to reduce the size. Note that maintaining the cavity dimensions, as the ridge height increases, the cavity resonance frequency decreases. By using this rule and with the help of an eigenmode solver, the cavity can be tuned to our desired center frequency and with acceptable dimensions according to the constraints imposed by the antenna array theory. The first (CPW + SIW) and last part (SIW + Antenna slot) of the synthesized lossy circuit can be physically dimensioned with the same design rules of the previous section and again finding that the closer the coupling slots are to the edge of the SIW or air-filled cavity, the greater the coupling.

Different views of the designed Filtenna using a lossy synthesis technique are shown in Figs. Fig. 4. b-d, while the final dimensions are shown in the captions. Note in Fig. 4. c the very good agreement between S_{11} response of the synthesized lossy filter and the full-wave simulations of the designed Filtenna. Also note the flatness of the transmission parameters throughout the bandpass in both circuit (S_{21}) and Filtenna (gain). Also note the coherence between the directivity D_{Fil} and gain G_{Fil} of the Filtenna and the S_{21} of the synthesized lossy filter: $G_{Fil} \sim D_{Fil} + S_{21}$.

Fig. **4.**a-b show the $\emptyset = 0°, \emptyset = 90°$ cuts of the antenna radiation pattern. The directivity and gain are about 7 and 5 dBi at boresight, respectively. As in the previous case, the difference in dB between the gain at the central frequency of Tx and at the beginning of the Rx frequencies is 19 dB approximately and complementary split ring resonators can be placed between the Tx and Rx Filtenna arrays to get further isolation [71].

The size of the designed Filtenna is $6.8\ x\ 7.6\ mm^2$ approximately, but according to [74], vias holes must surround the air cavity to ensure connectivity of the upper and lower ground planes. Despite the negligible impact of these vias in the frequency response of the design, they increase the total footprint of the Filtenna up to $7.8\ x\ 8.6\ mm^2$ $(0.72\ \lambda\ x\ 0.65\ \lambda)$ approximately. This in turn limits beamsteering up to $\pm 32° \ x \ \pm 25°$ in azimuth and elevation, respectively. This is achieved without the appearance of grating lobes according to Fig. 4..

It is important to remark that this design based on a lossy filter synthesis technique overcomes in terms of gain flatness in the passband the previous one based on a lossless technique. To the best of the author's knowledge this is the first Filtenna design based on a lossy filter synthesis technique. Finally, the same procedure can be applied to the design of the Filtenna for the Rx frequencies.

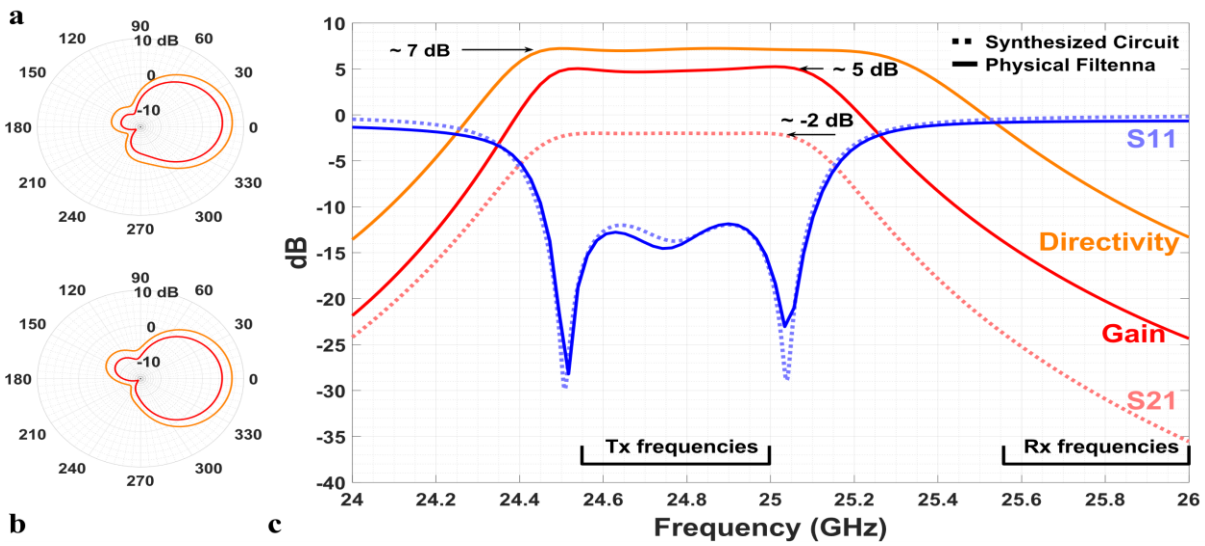


Fig. 4.20 Circuit and Full-wave simulations of the designed Filtenna. Radiation pattern at central frequency 24.772 GHz: **a** (cut $\emptyset = 0°$), **b** (cut $\emptyset = 90°$). **c** Scattering parameters of the synthesized lossy filter in dotted lines. S11, gain and directivity response of the designed Filtenna in solid lines

4.6 Insensitive Phased Array Antenna for 5G Smartphone Applications

To support the increasing demand of high transmission rate with throughput for various fixed and mobile services, phased arrays with multiple antenna elements have been attracting much more attention for next-generation (5G) networks [75]. Apart from the sub 6 GHz spectrum, 5G devices are also expected to cover the higher frequencies (beyond 10 GHz) where it can be carried out by employing phased array antennas [76],[77]. One of the challenges in designing phased arrays is the implementation and arranging of compact antennas with improved performances [78][79]. In this study, a high efficiency phased array antenna is proposed for 5G smartphone applications. Sufficient and quite good outputs have been achieved for the presented design. It also offers sufficient performance in data-mode with hand phantom.

4.6.1 Beam-steerable and Phased Array Antennas for 5G Smartphones

In cellular environments, the angle of arrival is likely to be distributed across the sphere. Therefore, high-gain phased array with wide scanning and improved radiation coverage is desirable for universal applications. The phased array contains multiple compact radiators arranged in planar or linear from and fed with different phase shifts [80]. The antenna radiation pattern can be steered electronically to different scanning angles. Fig. 4.21 shows a phased array architecture that can be used for the beam-steering purpose in linear array 5G smartphone antennas. The feeding network of the antenna arrays can be accomplished by employing cheap phase shifters. This might increase the complexity of the system but would improve the increase coverage and performance of the antenna array [81].

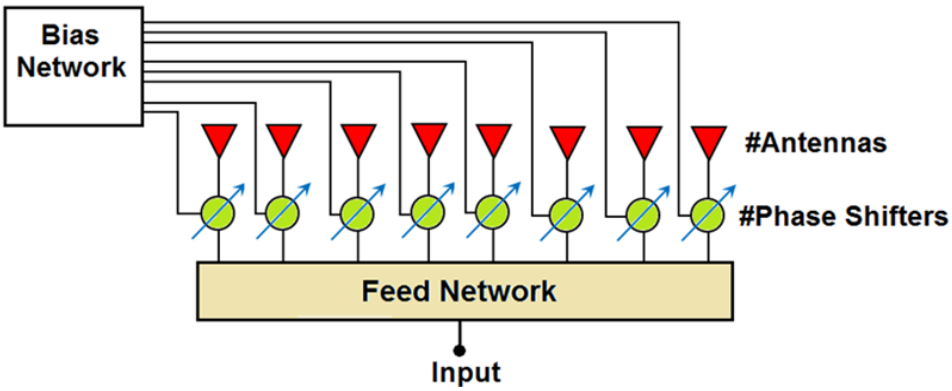


Fig 4.21 Phased array architecture

Compact antennas can be arranged in linear or planar array form to be used in phased array structures with high-gain characteristics for 5G wireless communications. Different from the conventional antennas (patch, monopole, and planar inverted-F antenna (PIFA) antennas) with omnidirectional radiation, the end-fire resonators, such as Vivaldi, Yagi, linear tapered slot *antenna* (LTSA) are more suitable for the communication between user and base station in 5G mobile communications [82]-[84].

4.6.2 Antenna Design Details

The introduced phased array smartphone antenna is arranged on a cheap FR-4 dielectric with characteristics of h_{sub}=0.8 mm, permittivity (ε_r)=4.3, and loss tangent (δ)=0.025. As illustrated in Fig. 4.22, eight substrate-insensitive antenna elements have been with linear array arrangement is placed in the top edge of the board with the size of $W_{sub}\times L_{sub}$=55×110 mm^2. The arranged array has a low-profile. For the beam steering purpose, the distance among the antenna resonators ($W+W_2$) is chosen to be $\lambda/2$ of the resonance frequency. The EM simulation CST software was used for the investigation. The dimensions of the design parameters are specified in Table 4.6.

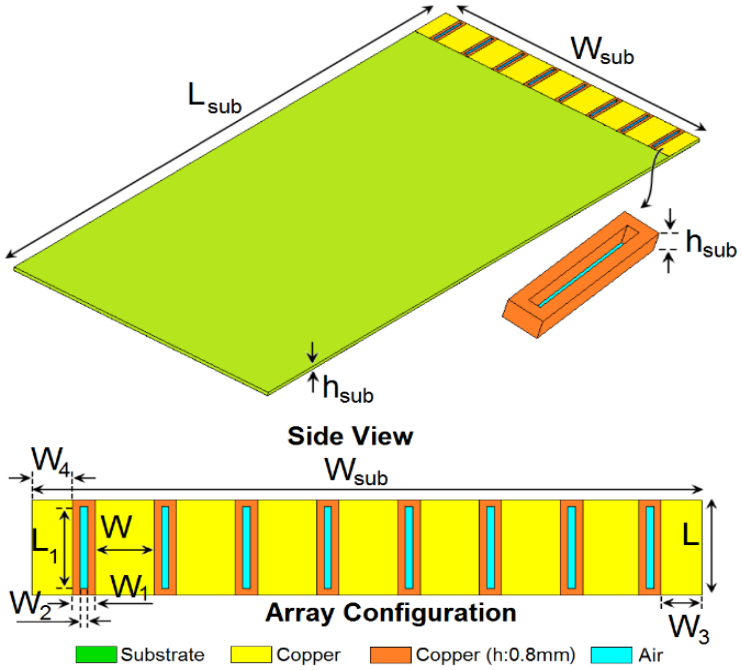


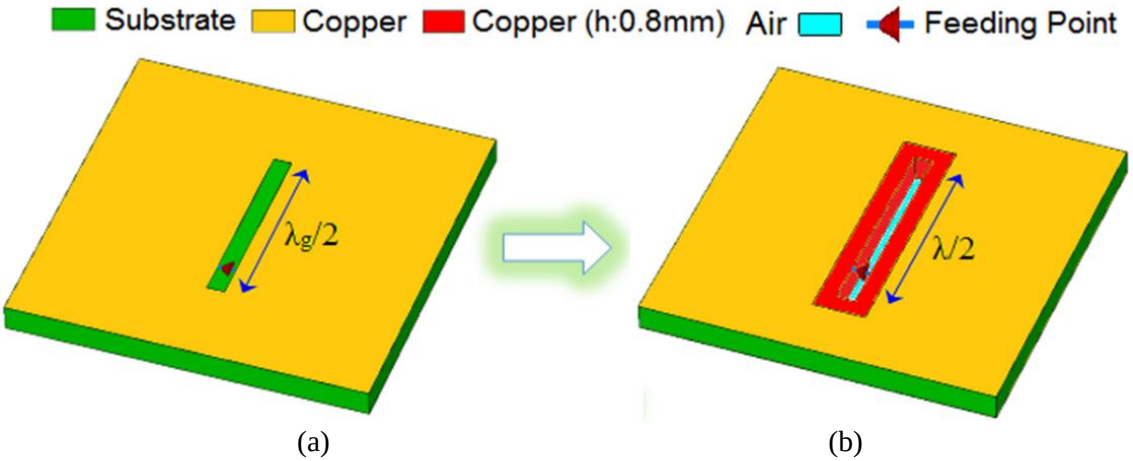
Fig 4.22 Proposed 5G smartphone antenna configuration

Table 4.6 The values of the design parameters

Parameter	W_{sub}	L_{sub}	h_{sub}	W	W_1
Value (mm)	55	110	0.787	5.25	1.5
Parameter	W_2	W_3	W_4	L	L_1
Value (mm)	0.5	3.125	3.125	8.3	7.8

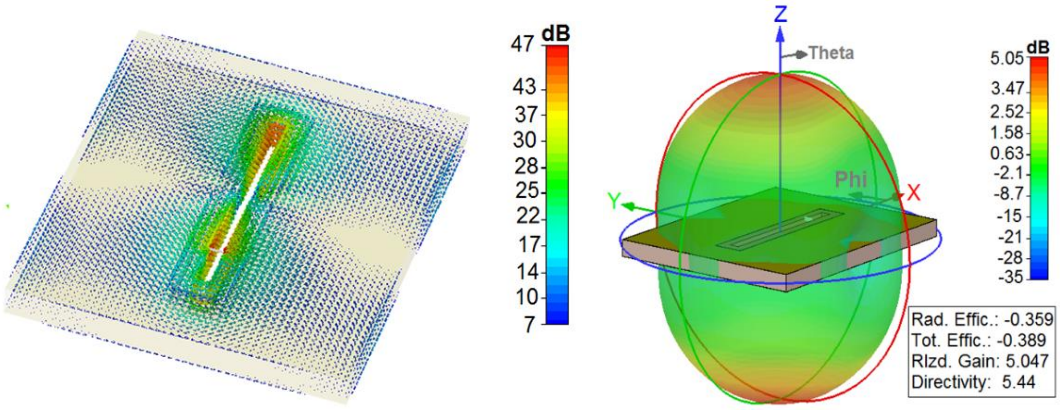
4.6.3 Characteristics of the Antenna Element

Conventionally, the printed slot antenna (PSA) contains a radiation element which is arranged by cutting a rectangular slot in a copper layer. Its length is about λ/2 and the width is a small fraction of a wavelength. The slot antenna is a complementary element of a dipole antenna with a different polarization mode. It has a low profile with a simple structure and flexible in nature, and low-cost for fabrication [85]. In the presented antenna design technique, as illustrated in Fig. 4.23, the resonator of a conventional slot structure with an operation band of 22-23.5 GHz is converted to a metal-ring loop resonator with the same thickness of the substrate. This could not only improve the performance of the antenna but also eliminate the effect of the FR-4 dielectric which is lossy for higher spectrums. The discrete-port feeding technique is employed for the antenna excitation. The current density for the metal-ring slot resonator at its resonant frequency (22.25 GHz) is plotted in Fig. 4.24 (a). As expected, the employed metal-ring radiator has maximum densities and behaves highly active [86]. The 3D radiation of the metal-ring design is represented in Fig. 4.24 (b). It is found that the design offers a well-defined radiation, covering both sides of the FR-4 dielectric. Besides, it provides a high realized gain of 5 dB.



(a) (b)

Fig 4.23 (a) conventional 22.25 GHz slot resonator and (b) the proposed insensitive antenna



(a) (b)

Fig 4.24 (a) The surface current and (b) transparent radiation pattern at 22.25 GHz

4.6.4 Fundamental Properties of the Insensitive Phased Array Design

Fundamental properties of the proposed beam-steerable 5G smartphone antenna are described in this section. Fig. 4.25 illustrates the scattering parameters (S_{11}~S_{81}). As illustrated, the design exhibits quite good S_{11}~S_{81}characteristics around 22.25 GHz. Moreover, low coupling (S_{mn}<-15 dB) is observed for the introduced array design. Fig. 4.26 illustrates the cartesian realized gains of the array different scanning angles. As seen, the antenna has good gain levels could cover a wide scanning range of ±70^o.

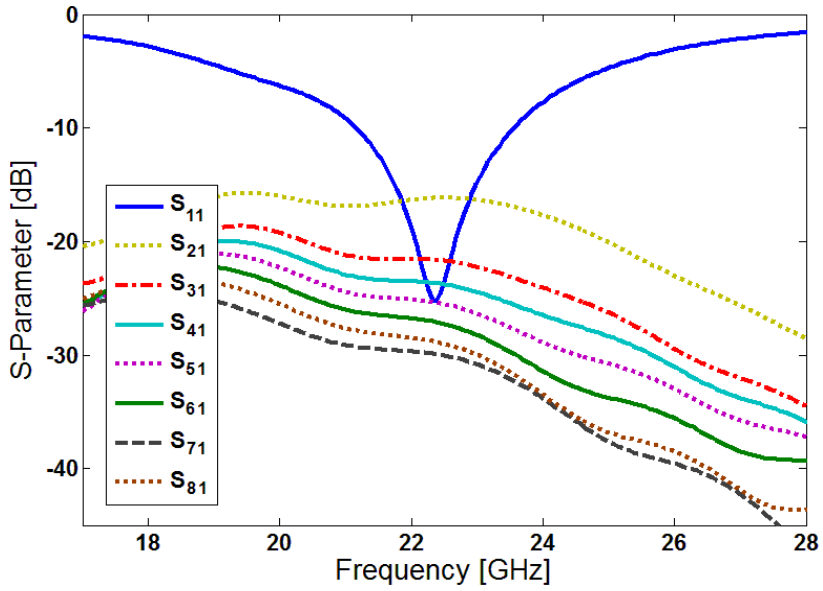


Fig 4.25. S-parameters of the designed 5G phased array

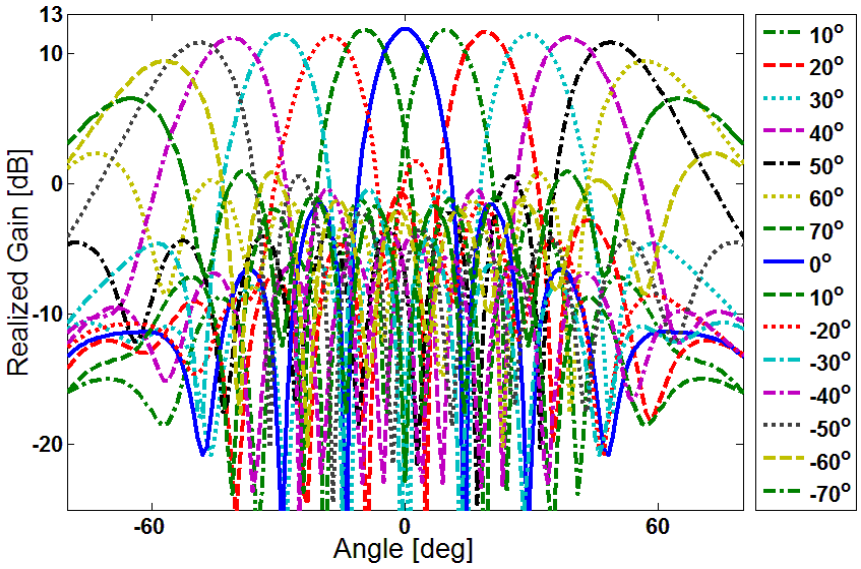


Fig 4.26 Beam steering of the 5G phased array with 2D cartesian gain values

Fig 4.27 illustrates the 3D beams of the designed array 5G antenna for various angles. It is seen that excellent radiation beams over 0-70 scanning angles are provided. As shown, the design provides well-defined radiation beams at 0°,15°, 30°,45°, 60°, and 70° which could cover half-space of the radiation coverage for the smartphone mainboard [87]. Fundamental properties of the design including directivity and efficiencies for the steered beams of the mobile-phone array at 22.25 GHz design are presented in Fig. 4.28 Across the range of 0^{o} to 60^{o}, the efficiencies are greater than 90% (-0.5 dB). Also, it provides sufficient maximum gain levels.

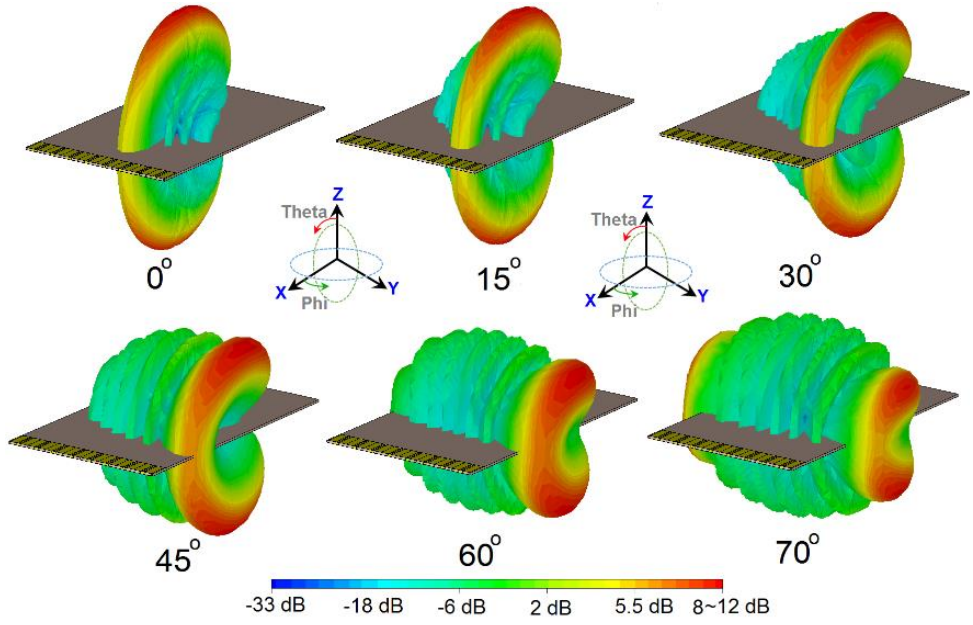


Fig 4.27 3D radiation beams for 0 to 70 degrees

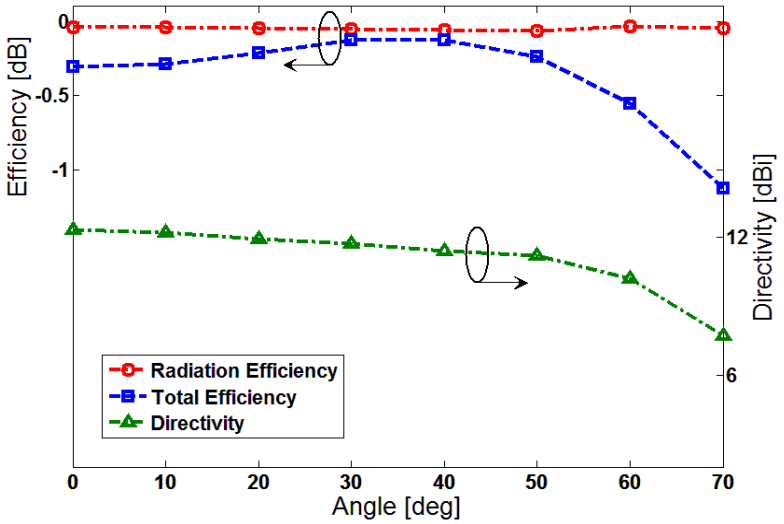


Fig 4.28 Fundamental radiation characteristics

4.6.5 Insensitivity Characteristic of the Proposed Antenna

The design characteristics of the proposed phased array are insensitive to various substrate's properties. To understand this function, the coefficient reflection (S_{11}) results for different dielectric constant (epsilon: ε) are investigated in Fig. 4.29. In addition, the antenna gain and efficiencies (radiation and total) for different loss tangent (δ) values are studied in Fig. 4.30. It should be noted the studied substrates have different loss tangent values which could affect the efficiency and gain of an antenna [88]. According to the obtained results in Figs. 4.29 and 4.30, it can be discovered that the designed phased array is insensitive for different substrate types and exhibits similar behavior for different dielectric constant and loss tangent values.

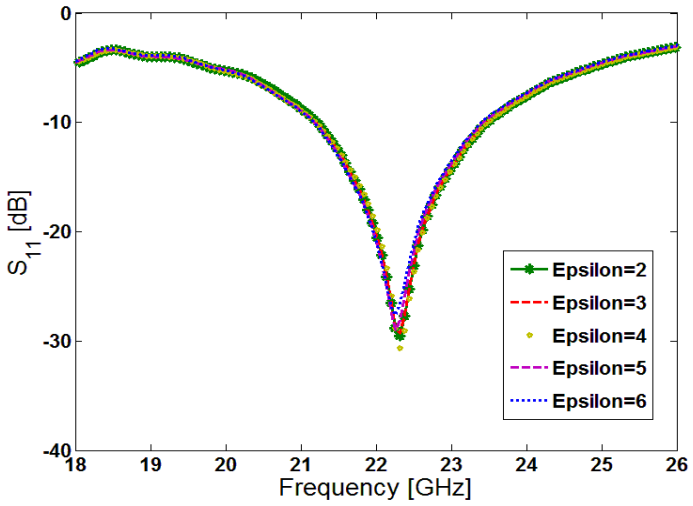


Fig 4.29 The coefficient reflection (S_{11}) for various substrate-types

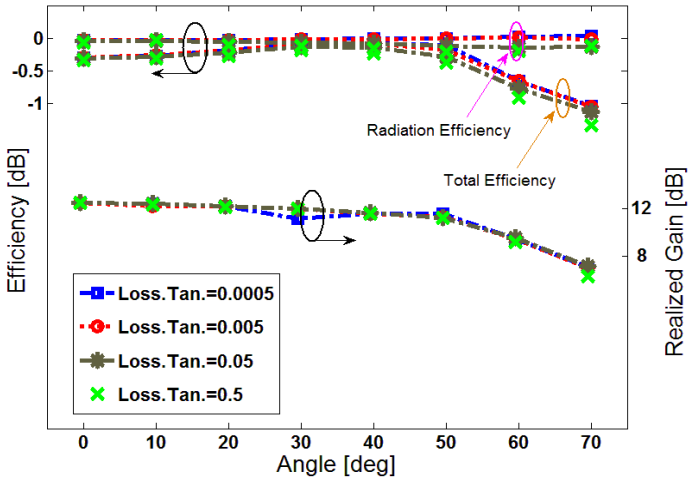


Fig. 4.30 The efficiency and gain results for different loss tangent (δ) values

4.6.6 User-Hand Impact on Antenna Performance

The user-hand is a body-part that most frequently touch handheld devices and usually has negative impacts on antenna performance [89]. Fig. 4.31 represents the 3D beams at various angels (0°~60°) in the presence of hand phantom (data-mode). As plotted, the beam-steerable phased array antenna provides well-defined radiation beams at various angels. This might be due to compact sizes and insensitivity function of the employed elements which are not highly affected by user-hand.

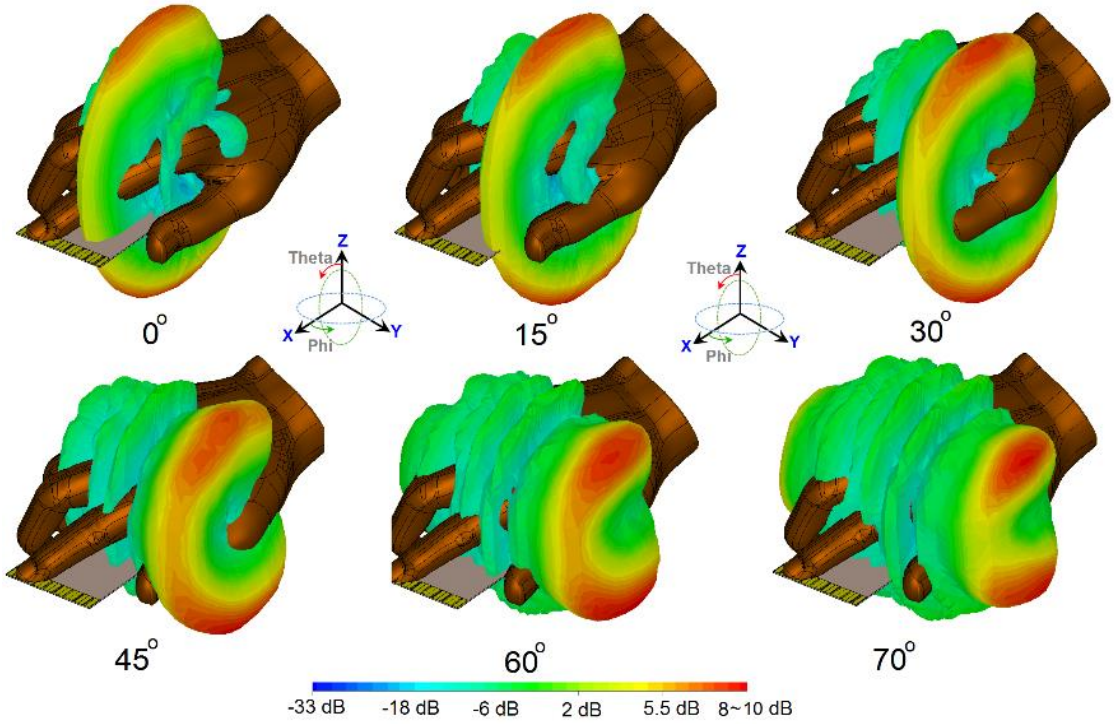


Fig. 4.31 Radiation beams of the design in the presence of the user-hand

4.6 Conclusion

5G single handset MMIC PA design is necessitated to exhibit linear operation and broadband coverage for entire bandwidth, while it is restricted by size and power consumption. The main

cause of the limited battery lifetime of typical PAs for multicarrier systems is the rapid reduction of PAE with the output power level when they require to back off the power handling. The dynamic load modulation Doherty PAs have been widely used to amplify the modulated signals with high crest factors due to its enhanced efficiency in deep power back-offs. The linearity and efficiency of a MMIC PA are deeply relied on the transistor characteristics of transconductance profile, the ratio between drain bias and knee voltage and the harmonic traps. GaAs pHEMT process is a mature technology with a high cost advantage that has led to widespread adoption in the cellular communication market. The multiband transmitters tend to employ harmonic tuned MMIC DPAs in medium power levels applications, due to their higher efficiency and lower thermal dissipation in comparison with linear counterparts. In addition, there are other techniques for improving the power amplifier efficiency at the back-off, however, the Doherty is the simplest one. Designing compact Doherty amplifier increases the design complexity, however, it can achieve the required linearity. Also, design of a differentially driven reconfigurable planar filter-antenna integration with high-gain and high-common mode suppression is proposed for 4G and 5G RF front end systems. Along with the frequency reconfigurable characteristics, the design has some more advantages including high-gain, high radiation efficiency and low cross polarization level due to the differential-fed terminals as well as the accurate symmetry of the structure. Four open-loop rings are used to realize the required nulls at both edges of the passband for the filtering performance. The introduced reconfigurable filtenna has a height of 0.82 mm and operates at the centre frequencies of 4G and sub-6 GHz 5G. The presented filtenna is simulated, analyzed and optimized using the CST tool. In addition, a filter-antenna integration has been studied here. A synthesis-based approach has been followed for the filter-antenna co-design. Two Filtenna synthesis techniques have been discussed: lossless-based and lossy-based, being the last one a better approach to preserve the flatness in the gain of the Filtenna. To the best of the author's knowledge this is the first Filtenna design based on a lossy filter synthesis technique. Filtennas allows the practical application of Phased Arrays in commercial FDD backhauling radios. This also enables several positive features at application level, among which: increased network flexibility thanks to beam steering; compatibility with software-defined network (SDN) paradigms involving dynamic reconfiguration. These also reflect several aspects related to the ever-increasing topic of green telecommunications: less intrusive visual impact in urban areas than conventional dish-like antennas; reduced number of radios equipment to cover a meshed network; more efficient exploitation of radio and power resources even extending coverage and mobile traffic data rates up to the forthcoming 5G standards. Moreover, an insensitive phased array antenna with air-filled slot-loop resonators is introduced for 5G mobile communications. It is designed on the FR-4 substrate and working a 21-23.5 GHz. Eight elements of metal-ring elements are linearly arranged on the top of the phone PCB. Sufficient and quite good outputs have been achieved for the presented design. It also offers sufficient performance in data-mode with hand phantom.

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