# GAMMA: a 16-Channel Spectroscopic ASIC for SiPMs Readout with 84dB Dynamic Range

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***Abstract*—GAMMA (Gain Amplitude Modulation Multichannel ASIC) is a 16-channel ASIC, designed in 0.35 $\mu$m technology to read the charge provided by silicon photomultipliers on a wide amplitude range. This chip was designed to satisfy the demanding requirements of the INFN the GAMMA project, where a 3" $\times$ 3" large lanthanum bromide crystal is to be read by silicon photomultipliers, aiming at state-of-the-art energy resolution. Because the energy range of the application is 100 keV - 20 MeV, signals in a wide dynamic range have to be processed by the ASIC. This wide dynamic range requirement raised the necessity of an adaptive gain change solution in order to guarantee high signal to noise ratio together with large full-scale range. While the ASIC input stage features a programmable static gain, the analog filtering channel exploits a self-triggered gated integrator stage with an automatically adjusted gain for each detected input current pulse; one of the following values is selected: 10 [mV/pC], 2 [mV/pC], or 0.83 [mV/pC]. The gated integrator gain is predictively adjusted before the circuit reaches saturation, thanks to a time-gated threshold mechanism, and provides negligible charge loss when the gain is switched (<20 fC). A pre-integration feature is also implemented in order to get rid of non-linearity due to delays in the integration phase that could take place in a multi-ASIC system. The ASIC uses a 5 V and a 3.3 V bias voltages, the overall power consumption being 280 mW. The ASIC was tested with a 12 $\times$ 12 SiPMs matrix coupled with a 3 inch $LaBr_3$, providing good spectroscopic performances (2.6% at the $^{137}$Cs photopeak emission energy of 662 keV), and was also tested irradiating the SiPMs with fast, bright NUV light pulses, in order to explore the ASIC wide range coverage while simulating the scintillation light emission of a lanthanum bromide crystal.**

***Index Terms*—SiPMs integrated readout circuits, Gated-Integrator, Lanthanum Bromide, Silicon Photomultipliers, Scintillators**

## I. Introduction

THE GAMMA experiment is supported by Istituto Nazionale di Fisica Nucleare (INFN) and it aims at exploring the frontiers of nuclear spectroscopy. In particular, one research line in instrumentation design focuses on the development of clusters of indirect detectors for gamma-ray spectroscopy based on $LaBr_3$ crystals, chosen for their high light yield (63-73 ph/keV, depending on the doping) and fast response time (16-25 ns).

Although excellent spectroscopic results can be achieved using photomultiplier tube (PMT) photodetectors to read the scintillation light, Silicon Photomultipliers (SiPMs) nowadays represent the state-of-the-art solution, in particular when a pixellated configuration is needed. Thanks to recent advances in manufacturing technologies, SiPMs have been increasingly employed in several domains, spanning from dark matter research to medical imaging [1]–[7]. They are particularly suitable as photodetectors for spectroscopic detectors for colliders or fixed-target accelerators experiments, thanks to their small pixel size, robustness, high quantum efficiency and low sensitivity to large magnetic fields or ionizing effects [8]–[11].

In this paper we present a multichannel ASIC for SiPMs readout named GAMMA (Gain Amplitude Modulation Multichannel ASIC), specifically designed to fulfill the requirements of the experiment for a new position-sensitive the GAMMA spectrometer [12]–[14]. The requirements, presented in the following section, are particularly demanding in terms of spectroscopic energy range and resolution and, consequently, dynamic range (DR) of the input charge. The new position-sensitive spectrometer aims at sub-centimeter spatial resolution of the gamma photon interaction point in the scintillation crystal (for post-processing correction of the relativistic Doppler broadening effect [15]). An ASIC-based solution for the module accordingly favors a large number of channels integration and, in turn, a more dense sampling of the light distribution.

For the ASIC design, we targeted the readout of scintillation light produced by a co-doped $LaBr_3$ crystal, given its excellent performance for spectroscopy [16].

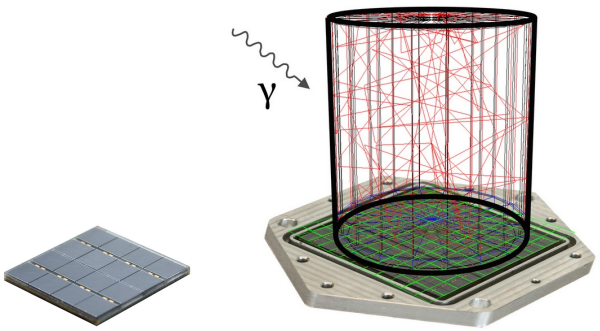
The interaction probability of photons over their path in matter is described by the Lambert-Beer absorption law; given the crystal mass attenuation coefficient [17], since the energy range of interest reaches 20 MeV, a thick cylindrical crystal is employed with a volume of 3" $\times$ 3" (respectively diameter and height), reaching a total interaction efficiency for gamma photons between 75% and 80% in the 10 MeV-20 MeV energy range.

The crystal is optically coupled to a 12 $\times$ 12 array of SiPMs whose charge signals have to be individually digitized. NUV-HD SiPMs produced by FBK were selected [18]. They are organized in tiles of 4 $\times$ 4 pixels (Fig. 1a), with a pixel size of 6.28 mm $\times$ 6.28 mm and cell size of 30 $\mu$m. Typical values of PDE, gain and DCR of the detectors are reported in [11]. In order to cover the exit window of the $LaBr_3$ crystal, a total of 9 tiles are employed. Each one will be individually read by a 16-channel GAMMA ASIC.

In previous works, smaller arrays of SiPMs (with individual readout of each detector) were tested with 2" $\times$ 2" crystals, providing 3.2% FWHM at $^{137}$Cs photopeak emission energy of 662 keV [19], but the use of an ASIC designed for targeting

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(a) (b)

Fig. 1. (a) Single tile of SiPM consisting of 4 × 4 pixels of 6 mm size. (b) 3D model of the detection module and simulated paths of the scintillation light emissions in a cylindrical 3" × 3" $LaBr_3$ crystal. 9 tiles of SiPM are arranged in a planar array (with 12 × 12 pixels), to reach an energy range spanning between 100 keV and 20 MeV.

medical applications [20], [21] limited the acquisition to a maximum energy of 1.3 MeV. The goal of this development is to extend the full scale range (FSR) to 20 MeV, while keeping a good energy resolution in the lower part of the range, thanks to the Automated Gain Control (AGC) circuit. The AGC is designed to swiftly optimize the feedback capacitance of the integrator filter each time a new scintillation event is detected.

The paper is organized as follows: Sec. II discusses the requirements of the GAMMA ASIC, whose design is illustrated in Sec. III. The results of the experimental characterization are reported in Sec. IV, while conclusions are drawn in Sec. V.

## II. ASIC Specifications

### A. Dynamic Range Requirements

The GAMMA experiment targets spectroscopy in an energy interval from 20 keV to 20 MeV, and count rates up to 50 kcps. In order to determine the amount of optical photons collected by each SiPM (and correspondingly the range of charge at the input of each ASIC channel), the light emission of the 3" × 3" crystal, collected by an array of 144 SiPMs of 6 × 6 $mm^2$ area each, has been simulated by means of ANTS2 software [22] up to 20 MeV (Fig. 1b).

The light distributions extracted by these simulations showed that, considering the minimum SiPM signal at the minimum gamma energy and the maximum signal at the maximum energy, the number of photons collected by each SiPM in the array ranges from few photons to about $10^4$ photons, providing a maximum charge 1 at the ASIC input of 3 nC. Maximization of scintillation light collection is a key factor to enhance resolution, but in order to have a circuit that allows both single-photon resolution and the collection of $10^4$ photons, the dynamic range of each channel has to be larger than 80 dB.

Many ASICs have already been developed for the readout of SiPMs, and a review can be found, for instance, in [23]. As reported with few examples selected and listed in TABLE I, commercially available ASICs are mainly developed for medical applications like PET, with limited DR. CITIROC [24], [25] features a DR of $2.5 \times 10^3$ photons and a maximum input charge of 400 pC. The ASIC SIPHRA [26], [27] shows an excellent 78 dB DR and a 4.8 nC maximum input charge. Considering our requirements (see bottom line in TABLE I) we have decided to develop a new ASIC that is able to provide at the same time a low noise in the lower energy region and high DR capability.

TABLE I
ASICs FOR GAMMA SPECTROSCOPY COMPARISON TABLE

| ASIC | Input Noise | FSR | max n. phe / DR | # Ch |
|---|---|---|---|---|
| PETIROC 2A | - | 400 pC | 3000 phe | 32 |
| SIPHRA | 630 fC | 4.8 nC | 78 dB | 16 |
| TIMPIC-II | 250 fC | 800 pC | 70.1 dB | 16 |
| CITIROC 1A | - | 400 pC | 2500 phe | 32 |
| **Requirements** | 200 fC | 3 nC | 85 dB | 16 |

| ASIC | Technology | Power diss. | Ref. |
|---|---|---|---|
| PETIROC 2A | 0.35$\mu$m SiGe | 6 mW/ch | [24] |
| SIPHRA | 0.35$\mu$m CMOS | 15-30 mW | [26] |
| TIMPIC-II | 0.35$\mu$m CMOS | 7 mW/ch | [28] |
| CITIROC 1A | 0.35$\mu$m SiGe | 7 mW/ch | [24] |
| **Requirements** | - | < 30 mW/ch | - |

Our design aims at minimizing the electronic noise with respect to the statistical one [29]. Neglecting the lanthanum bromide crystal intrinsic contribution to energy resolution, the energy resolution is optimized if the electronic noise contribution is smaller than the one given by statistical fluctuations of the number of photoelectrons (for a a given energy).

We will now shortly focus on the DR > 80 dB requirement, which can be derived from simple calculations. The total number of photoelectrons $N_{phe}$ generated after the 20 MeV gamma photon interaction in a $LaBr_3$ crystal is:

$$N_{phe}\Big|_{20MeV} = 20\ [MeV] \cdot 73\ \left[\frac{ph}{keV}\right] \cdot PDE \approx 58 \times 10^4\, phe \tag{1}$$

where 73 [ph/keV] is the light yield of commercial co-doped $LaBr_3$ and PDE≈40% is the photodetection efficiency of the SiPMs. For a 20 keV gamma photon interaction in a $LaBr_3$ crystal the total number of generated photoelectrons $N_{phe}$ is 730, therefore:

$$\sigma_{stat}\Big|_{20keV} = \sqrt{580} = 24\, phe \tag{2}$$

where $\sigma_{stat}$ is the statistical fluctuation of the number of photoelectrons that is associated to the collection of optical photons. Let us now assume that, in order to have an electronic noise $\sigma_{elect}$ that is negligible with respect to the statistical noise $\sigma_{stat}$, their ratio has to be $\sigma_{stat}/\sigma_{elect} > 4$. The maximum electronic noise generated by a single channel $\sigma_{elect,1ch}$ that allows to have a negligible worsening of the energy resolution is:

$$\sigma_{elect,1ch} = \frac{\sigma_{elect}}{\sqrt{N_{ch}}} < \frac{\sigma_{stat}}{4\sqrt{N_{ch}}} = 0.54\, phe \tag{3}$$

where $N_{ch}$=120 is the number of channels of the module that are covered by the scintillation crystal, out of the 144 SiPMs in the array (see Fig. 1b).

As anticipated, the detection system shown in Fig.1b has been simulated with ANTS2 with gamma photons from

100 keV to 20 MeV, considering a gain of SiPM of $2\times10^6$, an electronics noise of 1 mV superposed to the useful signal sampled value (computed assuming a 3 V voltage swing at the integrator output, and a value of 70 dB for the DR of the stage), and a gain of the amplifier sufficiently low not to provide saturation with the largest signal in the energy range.

In order to avoid saturation in each channel for a 20 MeV interacting of gamma photons, ANTS2 simulations indicate that the saturation signal should be equal or larger than $10^4$ photoelectrons. Under this condition, less than 20% of the events present at least one saturated channel on the 144-SiPM array; the tall, cylindrical shape of the crystal leads to a large amount of scattering and reflections, therefore making the light distribution over the SiPMs uniform. The overall dynamic range required by a single channel is therefore:

$$DR > 20\, log_{10}\left(\frac{10^4\,[phe]}{\sigma_{elect,1ch}}\right) \approx 85\, dB \qquad (4)$$

In Fig.2 the overall statistical noise and the total electronics noise (both extracted from simulations and numerical analysis, assuming that the gain is constant or it is set by the AGC circuit) are reported for the complete energy range. Both contributions are extracted from ANTS2 simulations; if the AGC is active we assume that each ASIC channel has adopted the best gain (that is, the highest gain that does not induce saturation) in the measurement, out of three available settings.

If a constant gain is considered for the amplifier, the simulation showed that the electronics noise is dominant with respect to the statistical noise in the low energy range, affecting the overall resolution up to many hundreds keV; the relation $\sigma_{stat}/\sigma_{elect} < 4$ holds up to 600 keV. The constant gain of the readout electronics implies in fact a trade-off for the readout electronics between low-noise and dynamic range capabilities.

Considering our detector reference technology for the application (NUV-HD SiPMs produced by FBK), the typical dark count-rate corresponds to 100 kHz/mm$^2$. If the current signal from SiPMs is integrated for a period equal to 5 times the 30 $\mu$m cell SiPM reset time constant and the dark counts are modeled using a Poisson distribution in time, the dark counts fluctuation are smaller than the statistical fluctuation of the photoelectron signal even for a 20 keV gamma photon interacting in the $LaBr_3$ scintillator, and therefore negligible for all energies in our target application.

When an adaptive gain for the amplifier is implemented, calculating the equivalent noise at the input, supposing that each amplifier channel has adopted the best gain in the measurement, the resulting noise is negligible with respect to the statistical noise in the whole energy range.

We have introduced in the ASIC the AGC circuit, which automatically increases the integration capacitance of the gated integrator stage to reduce the gain for large signals. This technique, already implemented in other ASICs for x-ray detection [30] or astrophysics experiments [31], allows to implement a piece-wise linear characteristic and an overall gain compression. The sizing of the capacitors and of the switching thresholds, as well as the switching logic, are described in Sec. III-C.

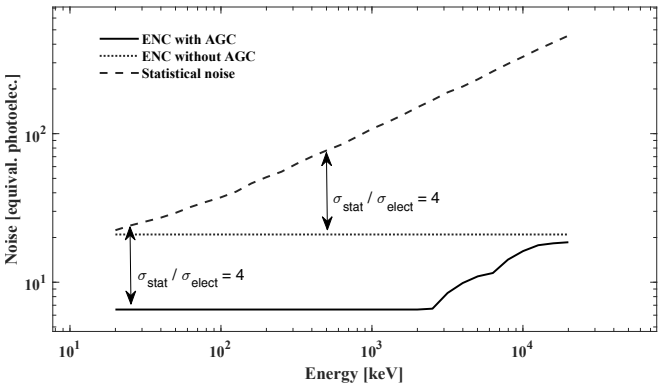



Fig. 2. Comparison of equivalent input noise contributions to energy resolution as a function of the incoming photon energy in the 100 keV - 20 MeV range, obtained from numerical simulations in ANTS2 software. The adaptive gain control circuit allows for lower noise at low energies and, in turn, to extend the energy interval of the measurement. Fixed gain acquisitions are degraded at low energies by the electronics noise, in the energy interval where the electronics noise results comparable or even higher than the one associated to the collection of photons in the detector (statistical noise).

### *B. Input Stage Requirements*

The input stage requirements strongly depend on the characteristics of the SiPM detectors. A typical circuit model for SiPM NUV-HD detector (Fig.3), that was adopted in our simulation phase, is described in [5], [23], [32]. Key parameters of such model are the SiPM detectors reset time, the micro-cell capacitance $C_D$, and the ASIC input impedance $R_L$, the values of which also define the minimum time constant of the input current signal $\tau_i$ [23].

A review of input stage architectures for SiPM readout is presented in [23]. The input stage of the GAMMA ASIC, described in detail in Sec. III-A, is a current-buffer based on a positive-feedback configuration with a loop gain lower than one [33]. It has to be compatible with 100 kcps count rate capability, while also providing stability when merging SiPMs output nodes.

Let us analyze the fast response of the detector, in order to address stability and the suitable input stage impedance. In small-signal analysis, the overall parallel capacitance connected to the input node of the current buffer is mainly defined by the parallel composition of $N_S$ silent (non-firing) SiPM cells junction capacitance. Typical values for SiPM parameters of the reference technology are listed in [11], [32]. As shown in [23], the $C_{DET}$ capacitance that determines the response of the detector in small-signal condition might in principle be estimated as:

$$C_{DET} = C_G + N_S\,\frac{C_D\,C_Q}{C_D + C_Q} \qquad (5)$$

For the SiPM reference techology ($6 \times 6$ mm$^2$ NUV-HD pixels, 30$\mu$ cells), the $C_{DET}$=3 nF value was experimentally obtained; also, the SiPM recovery time constant $\tau_R$ equals 80 ns. Considering a single readout channel for each SiPM, and a target input resistance of the ASIC of 20 $\Omega$, a 3 nF detector capacitive load provides a time constant of the signal current equal to:

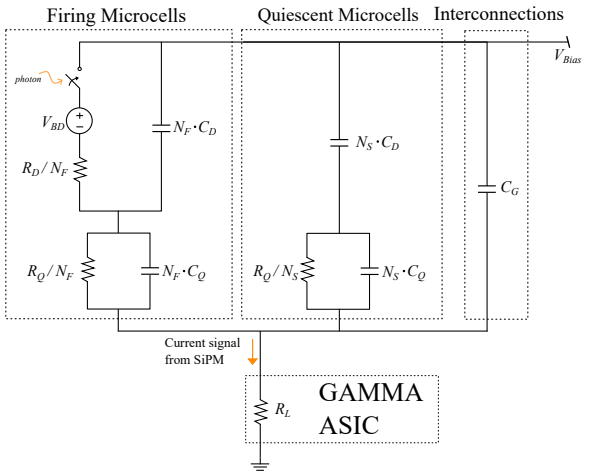



Fig. 3. SiPM circuit model. The large number of silent cells per channel results in the dominant time constant of the input signal current pulse.

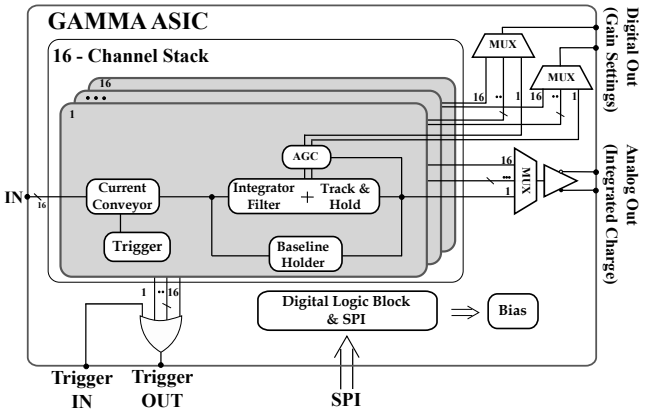



Fig. 4. GAMMA block diagram. The chip features 16 SiPM inputs and a multiplexed analog output. The Current Conveyor stages collect the signal charge, that is integrated in all filter stages when the input signal overcomes a programmable threshold in the Trigger circuit. The parallel outputs are multiplexed and sent to an external ADC by the fully differential output buffer. The AGC circuit adapts the gain of the filter to the signal amplitude.

$$\tau_i = \tau_R + R_L\, C_{DET} \approx$$
$$\approx 80\,[ns] + 3\;[nF] \cdot 20\;[\Omega] = 140\;[ns] \quad (6)$$

However, we have to consider that in some potential applications of our ASIC (e.g., in compact spectrometers for radiation monitoring, or in measurements with a much larger number of channels), it could be useful to merge several SiPMs ($N_{SiPM}$) to a single readout channel. In this case, the input time constant becomes:

$$\tau_i \approx N_{SiPM}\, R_L\, C_{det} \quad (7)$$

In particular, a large capacitive load at the input stage may impose severe challenges to the frequency response and even stability issues when a classical negative-feedback regulated cascode configuration, adopted in several ASICs, is considered [34].

The current-buffer Temes architecture allowed for the merging, in the experimental measurements described in Sec. IV, of few tens of SiPMs for a total input capacitance up to 70 nF, while providing an input impedance sufficiently low for the integration to last few microseconds.

## III. Analog Channel Design

The block diagram of the ASIC is shown in Fig. 4. The circuit can be connected to 16 SiPMs providing a simultaneous readout of the charge delivered by the detectors with independent AGC in each channel. The outputs of the channels (analog amplitude and digital code corresponding to the used gain for each integration) are multiplexed, converted to fully-differential signal, and routed towards the chip output pads.

Input currents are buffered by the Current Conveyor (CC) stage to both the Trigger stage and the Integrator Filter stage. The readout starts when one of the Trigger outputs overcomes an SPI-programmable voltage threshold. The DC current flowing from the Current Conveyor to the filter does not add any information to the readout and is subtracted by the Baseline Holder (BLH) circuit. The AGC circuit modulates the gain of the filter as a function of the input signal current integral amplitude. The channels share other auxiliary circuitry, including the SPI interface, a digital logic controller, and timing and voltage references.

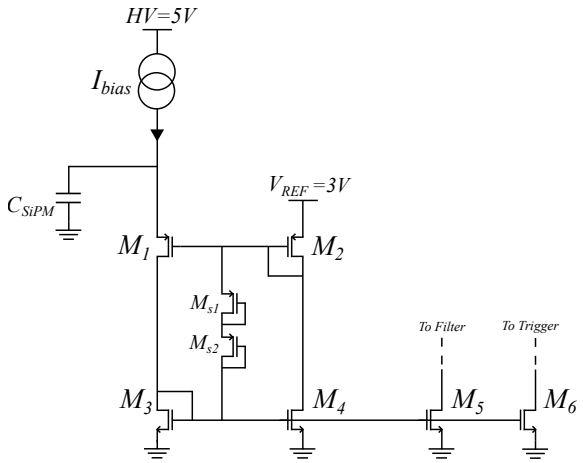



Fig. 5. Implemented positive feedback current conveyor circuit. The loop gain is lowered by the output resistance of current generator $I_{bias}$ at low frequency ($M_1$ is in voltage buffer configuration), but the $G_{loop}$ gets closely unitary when $C_{SiPM}$ can be considered a short circuit ($M_1$ is in common source configuration). Transitors $M_{s,1}$, $M_{s,2}$ are necessary for the circuit start-up phase, while $M_5$ and $M_6$ mirror the input current signal toward, respectively, the gated integrator stage and the trigger stage.

### A. Input Stage

The input stage is a CC circuit, necessary to convey the fast and large signal currents generated by SiPM detectors to both trigger and filter stages. The circuit is a Temes current buffer [33], shown in Fig. 5. In order to be stable independently of the input capacitance and provide low input impedance, the circuit exploits a weakly-positive loop gain $G_{loop}$, propagating across $M_1$, $M_2$, $M_3$, $M_4$ transistors. The low input impedance of the current buffer, ranging from 15 Ω to 35 Ω in small-signal conditions, allows to maintaining the tens of MHz wide

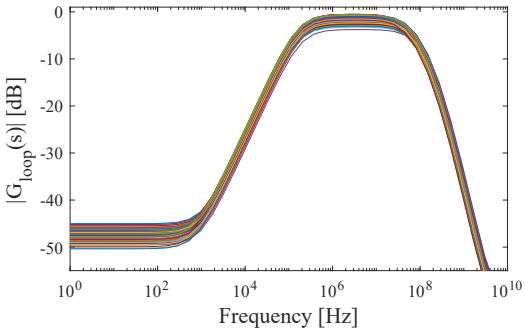



Fig. 6. Montecarlo simulation of the current conveyor loop gain with 300 points; the input stage of GAMMA is connected to a single $6 \times 6$ mm$^2$ NUV-HD SiPM. Because the loop gain is never larger than or equal to 0 dB, the circuit stability is ensured. The gain is closely unitary between 500 kHz and 50 MHz.

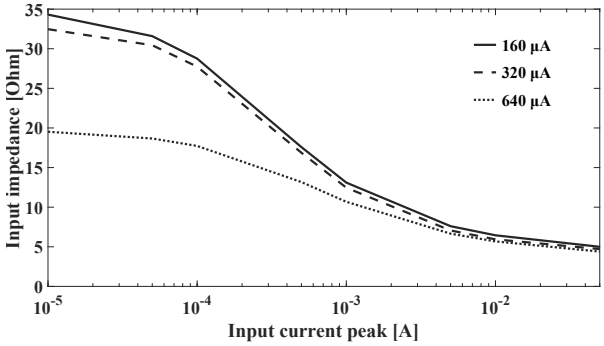



Fig. 7. Input impedance as a function of the input current peak amplitude for three different biasing current of the input stage. For larger biasing current of the input stage, the input impedance becomes less sensitive to input amplitude.

bandwidth of the input signal, even when loading a single channel with multiple SiPMs, for a total capacitance of few tens of nF. The CC bandwidth is superiorly limited at 65 MHz by the $M_1$ gate capacitance load.

The ASIC is designed with 3.3 V biasing, but the input stage biasing circuit is designed with 5V tolerant transistors. The main buffer is composed of $M_1$, $M_2$, $M_3$, $M_4$ transistors, which bias the Input Pad (Fig. 5) at a reference voltage $V_{REF}$ by circuit symmetry. Thanks to the small variance in NUV-HD SiPM breakdown voltage, the user-tunable input voltage reference $V_{REF}$ can be shared by all the channels. The input current biasing $I_{bias}$ is set by an internal DAC and can be tuned to optimize the circuit performance; it is sized to work at a nominal value of 160 $\mu$A total current consumption. The circuit has two stable operating points, thus $M_{S,1}$ and $M_{S,2}$ are used to start up the circuit and set the correct DC operating point.

In the frequency range of the signal ($f > 1\ MHz$), the detector capacitance $C_{SiPM}$ can be considered a short circuit, lowering the degeneration resistance at the source of $M_1$ down to a negligible value. Approximating all other capacitances to open circuits, the maximum loop gain in this frequency range is computed as:

$$G_{loop,max} \approx \frac{g_{m,M_4}}{g_{m,M_2}} \frac{g_{m,M_1}}{g_{m,M_3}} \tag{8}$$

Designing the stage with $G_{loop,max}$ smaller than unity, it ideally provides a sufficient condition to ensure the stability of the input stage. Such condition has been widely verified also with Monte Carlo simulations, taking into account process and mismatch variations (Fig. 6). Designing the circuit to have the loop gain low-frequency pole around a few hundred kHz with 1 nF detector capacitance allows for a correct behavior with larger detectors [35], from few mm$^2$ to many cm$^2$ in current technology processes. The upper limit for the detector area is set by the input current bandwidth requirements, considering the maximum integration time and counting rate required by the specific application: as specified before, a larger $C_{SiPM}$ implies a longer $\tau_i$. However, from just the point of view of circuit stability, while for negative feedback-based input stages a large detector capacitance may be critical, it does not introduce instability in the configuration adopted here.

From circuit analysis, the small signal input resistance is at the first order independent from the detector capacitance; for the signal frequencies, the following expression can be derived:

$$R_{in} \approx \frac{1}{g_{m,M1}} \left(1 - G_{loop,max}\right) \tag{9}$$

The input resistance $R_{in}$ is a function of the current flowing in the input stage: considering that in our application the signal current may be much larger than the fixed bias current, the input resistance may be dependent on the input signal current amplitude, scaling down to 5 $\Omega$ with very large input current, as reported in Fig. 7.

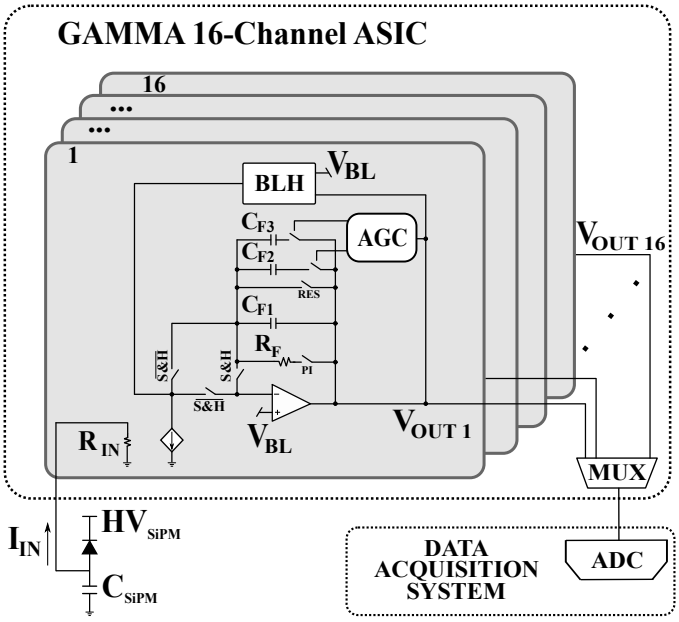
In order to integrate in a on-chip filter capacitance a 3 nC maximum input charge from the SiPMs, a scaling of the signal current is mandatory: a selectable demultiplication gain $G_{ccF,1}$=1/50 or $G_{ccF,2}$=1/100 for the filter input is implemented by programming the transistor $M_5$ aspect ratio W/L. The gain for the trigger input signal is also programmable but the current is scaled by $G_{ccT,1}$=1/2 or $G_{ccT,2}$=1/8, in order to achieve better sensitivity for small signal amplitudes.

Despite the introduction of demultiplication in the signal path, the filter stage has been designed to obtain an equivalent noise at the input of the circuit smaller than the signal induced by a single photon in the SiPM. Discrimination of discrete number of photons at the output of the filter is reported in Sec.IV.

### *B. Gated Integrator Filter*

To properly integrate the charge provided by the current conveyor, a Gated Integrator circuit is implemented. It can be demonstrated that this shaper offers better performance with respect to RC filter [20], in particular in terms of ballistic deficit for a given processing time. The schematic of the filter is shown in Fig. 8, including two other stages: a BLH circuit to cancel the bias current from the CC stage and the AGC block to extend the dynamic range.

Since we are dealing with monolithic crystals shining several SiPMs simultaneously, the gated integration starts at the same time for all channels. The integration state of the ASIC




(a)

Fig. 8. Implemented gated integrator filter with bleeding resistor and adaptive gain control block. The feedback resistance $R_f$ is connected until the start of the integration phase. The S&H switch is open until the end of the integration phase, then it is closed (the two complementary switches are opened) and the integrator holds the charge to be read. At the end of the read phase, the feedback capacitance is discharged by switch RES.

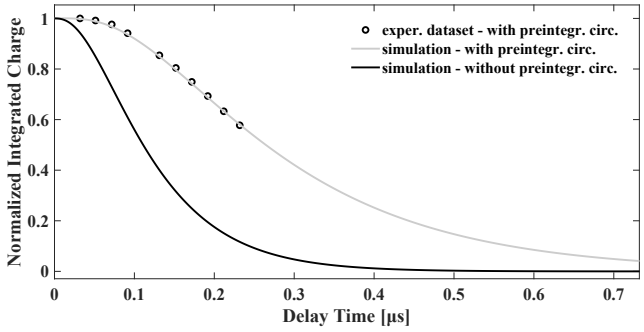



Fig. 9. Effect of the presence of pre-integration versus injection delay time. The integration is externally triggered, with a gradually increasing delay with respect to the optical pulse (generated using a laser diode based scintillator crystal emulator [36]) on the SiPM detectors. It can be noticed the improved robustness with respect to a standard gating approach in both measurements and theoretical data.

is set by a logic block that is sensitive to the trigger of all channels, or from an out-of-chip trigger (coming from other ASICs).

In order to avoid any charge loss, e.g. due to a delay in the trigger occurrence, the capacitor $C_{F1}$, which is permanently connected in the integrator in order to start the integration as soon as a current signal from the SiPMs is detected, is also connected in parallel to a bleeding resistor $R_F$ (PI switch is normally closed) which has the role to discharge the capacitor $C_{F1}$ when only noise is integrated in the filter and no signal is present. When a signal arrives and the integration state is set, the switch PI opens and the current integration proceeds on $C_{F1}$, without any discharge through $R_F$, which is disconnected.

In case a delay occurs from the trigger channel, no significant charge is lost from the delivery of the signal and the disconnection of $R_F$, as the time constant formed by $C_{F1}$ and $R_F$ is made sufficiently large with respect to possible delays from the trigger channel used as start-of-integration signal. The RC time constant is designed to be shorter than the following gated integration phase. This solution counteracts the possible ballistic deficit due to trigger channel output delays.

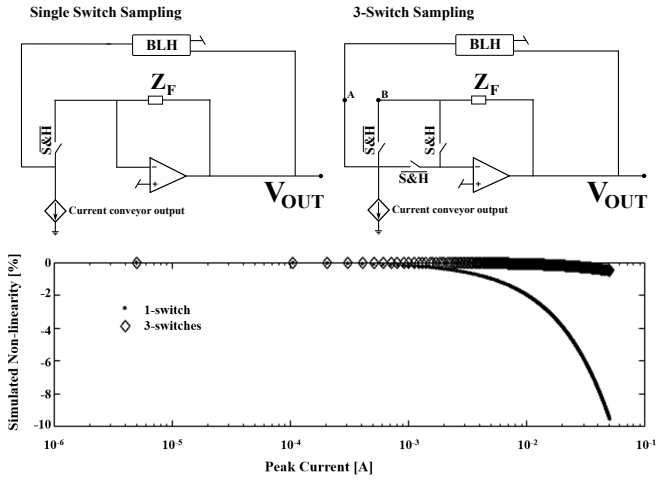



Fig. 10. (top) Circuit comparison of the single switch configuration and the 3-switch configuration for sampling the gated integrator output voltage. (bottom) Non-linearity comparison between the single switch solution and the 3-switch solution here proposed.

In Fig. 9 the experimental characterization of the asynchronous RC filtering (pre-integration) feature is shown. The solid line shows the integrated charge in a conventional integrator (i.e., without pre-integration circuit), where the start of the integration (i.e., the opening of the reset for $C_{F1}$) is delayed with respect to the arrival time of the signal. The time in the horizontal axis reports such delay. In the proposed solution, with $C_{F1}$ always able to integrate and with the presence of the bleeding resistance $R_F$ as discharging element (i.e. with pre-integration circuit), the simulation data show a much smaller loss of integrated charge vs. delay of the trigger with respect to the case without pre-integration, confirmed by the points from experimental measurements in this condition.

Counteraction of the ballistic deficit is also needed for a correct gain prediction, which is discussed in larger detail in Sec.III-C. Moreover, another contribution of the feedback resistance is to provide a path for the DC bias input current, therefore enhancing stability of the BLH-based analog filter.

The integration time in the filter can be set in a wide range from 100 ns to 20 $\mu$s, in order to properly integrate signals provided by scintillation crystals with different time constants.

Two switches configurations for sampling are depicted in Fig. 10. The 3-switch configuration is implemented in the the GAMMA ASIC; the three sample and hold (S&H) switches are alternatively connected to provide a track and hold feature to the circuit without adding another stage. A single switch, opening the input branch, could in principle allow for the correct sampling of the output voltage of the integrator and perform the same task of the 3-switch configuration.

For the single switch configuration, the gated integrator

TABLE II
ASIC NOISE FLOOR AND FSR WITH DIFFERENT SETTINGS

| CC Gain | Integ. Cap. | Input Noise | FSR |
|---|---|---|---|
| 1/50 | 1 pF | 0.44 pe$^-$ | 429 pe$^-$ |
| 1/50 | 5 pF | 1.26 pe$^-$ | 3429 pe$^-$ |
| 1/50 | 12 pF | 1.28 pe$^-$ | 5144 pe$^-$ |
| 1/100 | 1 pF | 0.66 pe$^-$ | 856 pe$^-$ |
| 1/100 | 5 pF | 1.96 pe$^-$ | 6858 pe$^-$ |
| 1/100 | 12 pF | 2.1 pe$^-$ | 10286 pe$^-$ |

input branch is connected to the CC output mirror before and during the integration. When the integration period is over, the S&H switch opens, and the capacitance in the feedback branch of the integrator holds the value. An issue of this configuration is that the voltage drop across the MOS implementing the switch pushes the CC output mirror MOS in ohmic region for large currents, inducing non-linearity.

Let us now analyze the circuit in Fig. 10 top right to understand the advantage of the 3-switch configuration. It can be noticed that the filter input voltage A, to first order, is not a function of the signal current. In fact, the loop gain sets the voltage on node A during the integration phase. When the integration period is over the switches commute, the virtual ground node is set on node B; the voltage at the output of the filter is fixed and multiplexed towards the output pad.

The 3-switch configuration guarantees a lower input impedance of the filter stage with respect to the single switch solution, the linearity interval of the latter being limited by the voltage drop on the switch, which pushes the current conveyor output mirror MOSFET in ohmic region for large signals.

It is important that in both configurations the BLH circuit is always connected to the input stage, allowing for a continuous subtraction of the DC current.

Once the gated integrator output is sampled, the output buffer converts the sampled gated integrator output in the fully-differential signal that is sent to the output pads of the ASIC for the ADC conversion. The 16 channels are scanned in round-robin fashion by an externally controlled multiplexer.

As soon as the hold phase (having a programmable duration of 8 or 16 $\mu$s) is over, a low impedance branch is connected in parallel to the integration capacitance (controlled by the switch RES in Fig. 8), allowing a fast reset of all channels.

TABLE II shows the dynamic range performance of different gain settings (simulated using Cadence EDA), considering a single photoelectron charge provided by the SiPM of 0.3 pC integrated for 800 ns (i.e. about 8 times the time constant of the input current pulse, considering the typical case of a single SiPM connected to each the ASIC input, and a 30 $\Omega$ small-signal input impedance of the ASIC, Fig.7).

### C. Adaptive Gain Control

For the implemented topology of the GAMMA ASIC, the energy resolution is a function of the absorbed the gamma photon energy. A detailed analysis of the many contributions to energy resolution in scintillator-based spectrometers is proposed [29] and [37].

The GAMMA ASIC has a piece-wise linear transfer function for each channel, shown in Fig. 11, designed in such a way

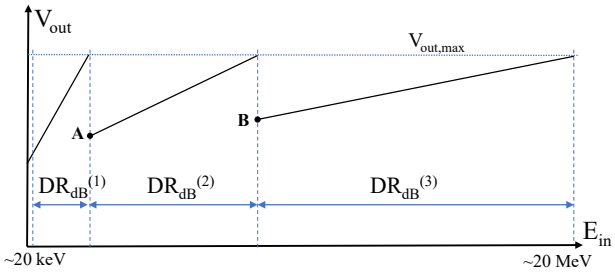



Fig. 11. Piece-wise linear transfer function of the GAMMA ASIC, designed to keep the electronic noise contribution to energy resolution well below the statistical contribution. In points A and B, the $\sigma_{stat}/\sigma_{elect}$ ratio is larger than a given constant.

that for input signal charges from SiPMs corresponding points A and B (they are drawn where the value of statistical noise is minimum on the trait of the piece-wise linear transfer function, and therefore the electronics noise might be relevant), the $\sigma_{stat}/\sigma_{elect}$ ratio is larger than a given constant, and therefore the electronic noise contribution to energy resolution stays well below the statistical contribution. This results are supported by numerical simulations of the scintillation events in ANTS2 environment shown in Fig. 2.

In this design the authors set the condition $\sigma_{stat}/\sigma_{elect} > 4$ and iteratively computed the maximum value of capacitance that can be set in points A and B, defining the gains ratio and therefore the overall dynamic range of the ASIC:

$$DR_{dB}^{GAMMA} = DR_{dB}^{(1)} + DR_{dB}^{(2)} + DR_{dB}^{(3)} \qquad (10)$$

Because the dynamic range $DR_{dB}^{(i)}$ has to decrease in each interval in order to cope with design requirements (the statistical noise doesn't increase linearly with the input signal) the authors found non beneficial to implement more than 3 possible integrator feedback capacitance settings.

Reducing the filter gain to increase the FSR signal charge would worsen the signal-to-noise ratio, therefore a simple gated integrator design with a static, large integration capacitance was avoided.

The adaptive gain approach (an example of adaptive gain control circuit-based front-end is presented in [30], [38]) is implemented to fully take advantage of the large linearity interval of the detectors, spanning from single photoelectrons up to $10^4$ avalanches. The AGC block is able to automatically switch from one gain set to another while integrating the pulse.

Two AGC switching logic circuits are integrated in the GAMMA ASIC. In the Voltage Threshold (VT) mode, the integration starts with the highest available gain (only $C_{F1}$ is connected). Then, when the output voltage overcomes a threshold, the AGC block connects the $C_{F2}$ feedback capacitance, lowering the filter gain. In order to further extend the FSR, the capacitor $C_{F3}$ is also connected if the threshold is overcome again.

The voltage threshold is internally generated or can be externally set using an ASIC pad. In order not to risk saturating the output of the filter while the new capacitor is added to reduce the gain, the voltage threshold has to be kept as low as 1 V. Because the integrator baseline value is 500 mV,

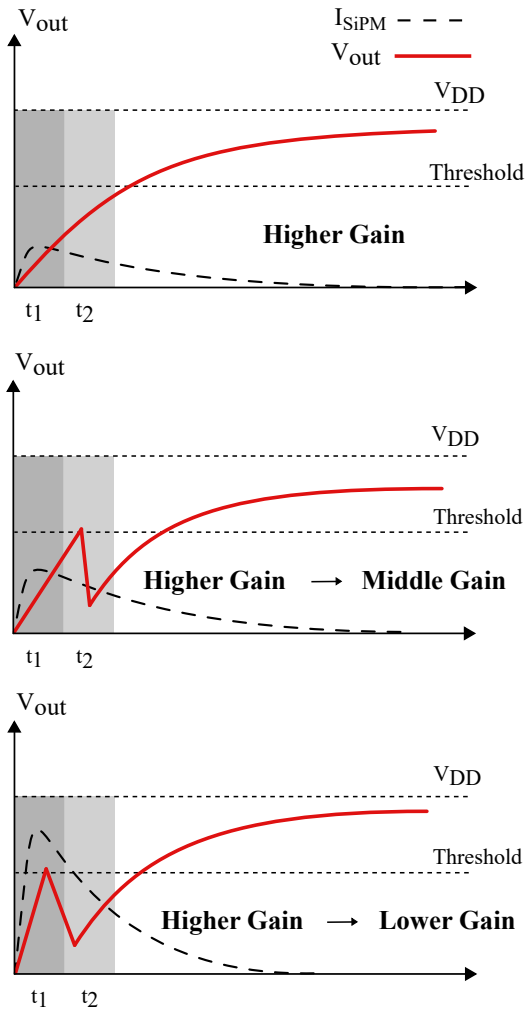



Fig. 12. TT operation of AGC circuit. Whenever the fixed voltage threshold is overcome within a programmable time window, the AGC circuit sets a lower gain for the gated integrator filter.

this significantly limits the voltage swing of the stage to only 500 mV more when the two higher gains are active; according to simulations, for typical time width of current pulses of few tens of nanoseconds, a higher threshold value leads occasionally to a late modification of the feedback capacitance, and therefore to a loss of the integrated charge when the integrator output reaches the upper voltage limit.

The second AGC operation mode, the Time Threshold (TT) mode, has been implemented in order to get rid of the aforementioned VT voltage dynamics limitations. The filter stage output voltage time-derivative is used at the start of the gated integration to estimate the optimum gain. This method uses two time windows, $t_1$ and $t_2$ (Fig. 12), generated from the main logic block and distributed to all the analog channels. The AGC logic checks, in each channel, if a fixed voltage threshold has been overcome within one of the two time intervals, setting the proper gain. When the threshold is overcome, a shorter time corresponds to a larger delivered charge: if the crossing happens in window $t_1$ the lowest gain is set. Else, if it happens in window $t_2$, the middle gain is set. If the threshold is not crossed within $t_2$ the higher gain is kept, and no capacitor is

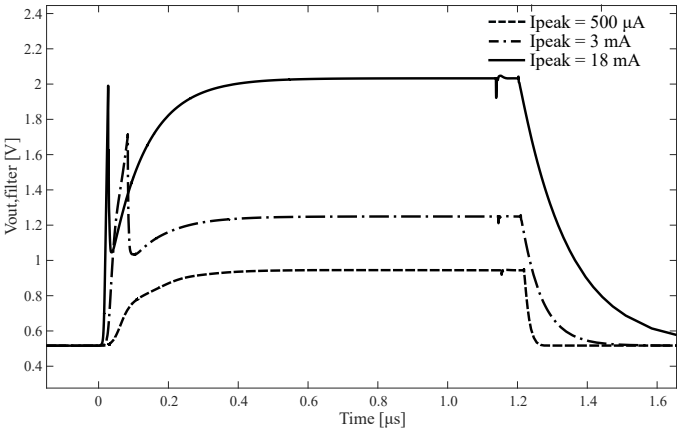



Fig. 13. Simulation of gated integrator output during the integration phase. Once the pulse is sampled, the following multiplexer provides to the output buffer an analog single-ended value. The gain switching is activated for the two higher amplitude pulses; a larger capacitance is connected in parallel to the feedback branch while integrating. When the hold phase is over, a low impedance path is connected in parallel to the feedback branch, allowing a fast reset of the capacitors.

added.

The simulated filter stage output is shown in Fig. 13 for three different amplitudes of the input pulse. For the two largest simulated inputs, the gain switching activates, and an additional capacitance is added to the feedback branch. The largest value of capacitance is added after the shortest time, because the output overcomes the fixed threshold within the shortest time window $t_1$.

The main advantage of this 'predictive' TT AGC strategy with respect to the VT one is that the threshold voltage can be safely placed at a middle value without sacrificing the output swing of the gated integrator, extending therefore the input charge range for which electronics noise contribution is minimized. A second, minor advantage is that there is always single switching between two gain settings, and the sequence of switching among all three gains is avoided.

In order to accommodate a charge distribution over time coming from different SiPMs and scintillation crystals combinations, each one of the two static time windows width is programmable via SPI interface, spanning from 4 ns to 2 $\mu$s on 512 non-linear steps; 2 bits are used for coarse setting and 7 bits for fine tuning of the TT time windows width.

### *D. Baseline Holder*

The BLH circuit has the purpose of guaranteeing a stable baseline at the filter output. Dynamically subtracting the DC current is a key aspect for correct integration of the signal: current pulses rate and dark current variations could generate a shift of the DC baseline and the integrated value. Not rejecting the DC and low-frequency components at the filter input would worsen the overall resolution of long measurements.

The circuit is similar to the one proposed in [39], providing a current output signal that is a function of the input differential voltage; transistor-level implementation is shown in Fig. 14. The non-linear voltage buffer stage allows the circuit output, to first order, to be insensitive to fast pulses (and

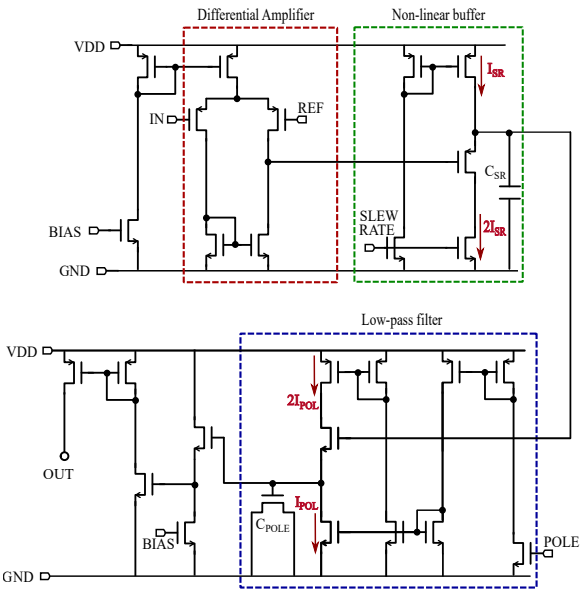



Fig. 14. Baseline Holder circuit implementation. The differential stage amplifies the differential signal with respect to a reference voltage, that is amplified and processed from a current limited buffer. The non-linear processing of the differential input allows to reduce sensitivity with respect to input count rate fluctuations.

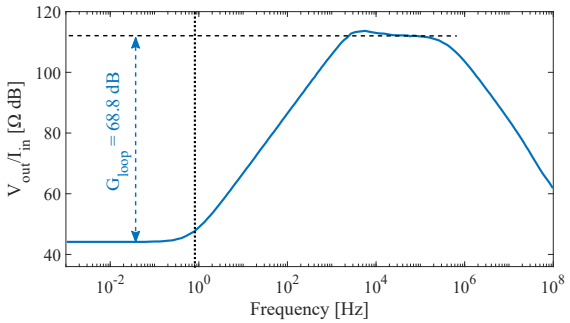



Fig. 15. Simulated effect of the baseline holder $G_{loop}$ on the output transfer $V_{out}/I_{in}$ of the filter while the resistor $R_f$ is connected. A $G_{loop}$ of 68.8 dB provides a dynamic DC cancellation.

therefore to their arrival rate variation in time). Because the integration and hold phases of the circuit only last few $\mu$s, the slew-rate limited buffer is not able to promptly adjust its output node, and the positive pulse does not propagate towards the output of the BLH stage.

The specifications the BLH has to fulfill can be expressed as a minimum 60 dB DC loop gain and a 1 Hz low-frequency pole to kill the loop gain at very low frequency, thus leaving the integrator response unaffected by this additional loop.

The low-frequency pole of the BLH is fixed by the transconductance of a current starving transistor and from a 70 pF capacitance. In order to save area, the capacitance is made with the gate of a standard n-MOS transistor with the drain and source connected to ground (the nominal voltage dynamic of this node is limited to few tens of mV, therefore the dependence of the capacitive load from voltage bias is not an issue).

In Fig. 15 it is shown the transfer function of the filter, when the BLH circuit is active. The low frequency small-signals are

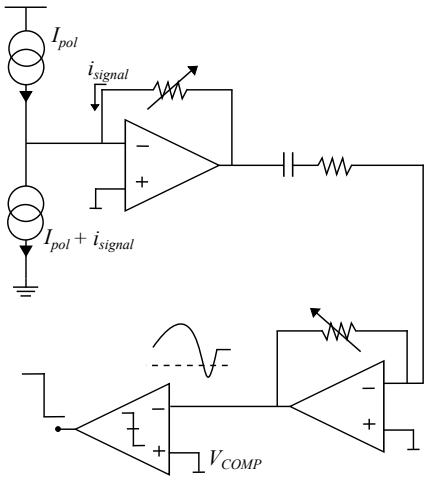



Fig. 16. Schematic representation of Trigger stage. It is made up of a static DC current subtraction, a programmable gain transimpedance amplifier ($G_{TIA}$ = 2 kΩ ÷ 20 kΩ), an AC coupled gain stage, and a voltage comparator with user-programmable threshold. Every time the analog output overcomes a fixed threshold, the Filter stage starts the gated integration. The self-triggering of the circuit allows for the integration of signals randomly distributed in time.

subtracted from the filter input by the BLH output stage. It can be noted that the BLH pole behaves as a zero in the overall transfer function; the gain is 106 dB at signal frequencies and 58 dB for frequencies down to 1 Hz.

### *E. Trigger Stage*

Even though pre-integration mitigates the effect of the delay on the start-of-integration signal, early detection of the pulse is a key aspect for time-variant filters.

A high gain, fast pulse detection stage is implemented in each channel to allow all of them to trigger a simultaneous acquisition (on all channels) of the integrated charge signal. Every time one of the analog outputs of a trigger stage overcomes a fixed threshold, all channels in the GAMMA ASIC start the gated integration. A digital signal is also sent towards an external pad for the transmission of the integration state among multiple ASICs.

The trigger circuit, represented in Fig. 16, is made up of a static DC current subtraction circuit, a programmable gain transimpedance amplifier ($G_{TIA}$ = 2 kΩ ÷ 20 kΩ), an AC coupled gain stage, and a voltage comparator with user-programmable threshold.

A high sensitivity of the stage is desirable in case of single photon measurements or to detect low-level signals.

The comparator threshold is common between the channels, provided by an internal DAC with multiple outputs. Because of the AC coupling between first and second stage, an imperfect DC current cancellation from the CC stage does not affect the DC value of the comparator input voltage, making it reasonably uniform across the 16 channels and enabling the sharing of the threshold DAC output among channels.

In small signal conditions, the trigger circuit output voltage is proportional to the number of generated photoelectrons. Considering a standard SiPM gain of $G_{SiPM} \approx 2 \cdot 10^6$ and an input signal characteristic time constant of 80 ns, the linear

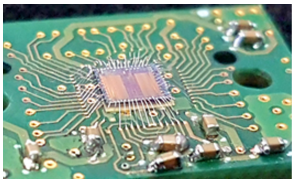


Fig. 17. GAMMA ASIC bonded to the carrier PCB. It is designed in the AMS 0.35$\mu$m technology and its die area is 3.1 mm $\times$ 3.1 mm.

transfer from photoelectrons to output voltage peak value is $G_{Trig} = 35\,[mV/pe]$.

### F. Biasing and Timing Logic

A 128-bit volatile memory block programs the internal settings of the ASIC, largely devoted to the seven internal DAC; settings data are transmitted to the ASIC using an SPI interface. Each DAC has multiple current outputs, used for biasing of the analog chain (current conveyor and BLH stages polarization) and of the logic blocks (trigger channels threshold setting, definition of time windows for the TT AGC operation mode).

The main task of the timing logic is to activate the integration state of the system when one trigger channel threshold is overcome. Once one of the trigger outputs is fired, all feedback resistors $R_F$ are opened, and the integration on all ASIC channels starts simultaneously. The logic also generates the two monostable pulses $t_1$ and $t_2$, corresponding to the programmable AGC windows in TT operation mode.

Once the integration time is over, the integrated charge on the capacitance is held in the readout phase for a time adequate to transfer the channel outputs to the external DAQ by means of the internal multiplexer. Once all channel outputs are multiplexed, the readout phase ends, and the reset signal rises, connecting a small resistance in parallel to the feedback resistance $R_F$, inducing a fast discharge of the integration capacitance in the filter. Once all channels are reset, the trigger channel outputs are enabled, the low impedance paths are disconnected from the filter feedback branches, and the ASIC is ready for the next pulse to be integrated. Considering the minimum hold time of 7.5 $\mu$s and a standard 500 ns integration time, the maximum count rate of the chip is 100 kHz.

A new release of the ASIC under production will provide a higher throughput thanks to the possibility to externally control the hold time, reducing the hold phase duration from 7.5 $\mu$s down to about 1 $\mu$s (time needed to scan the 16 channels with a 200 MHz clock ADC), and therefore the ASIC dead time during operations.

## IV. Experimental Characterization

The latest version of the GAMMA ASIC is designed in 0.35 $\mu$m technology, and features layout optimizations and an improved DR, thanks to previous experimental characterization of the $LaBr_3$ crystal. The integration capacitance absolute value was in fact trimmed in later releases of the ASIC, taking into account that the intrinsic contribution of the scintillator crystal is also an unavoidable contribution to energy resolution,

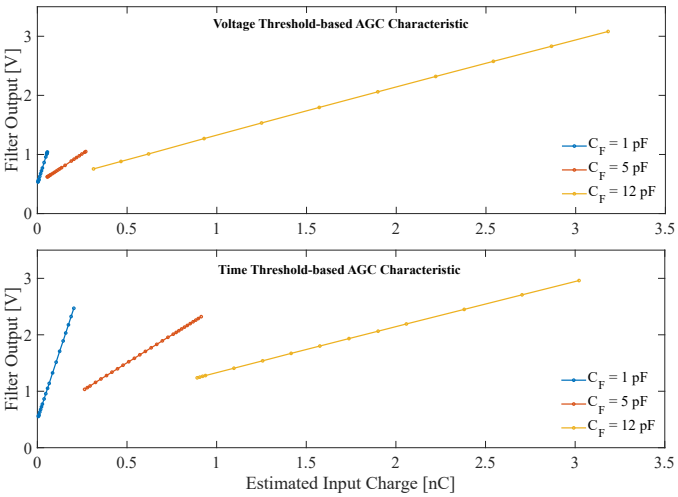
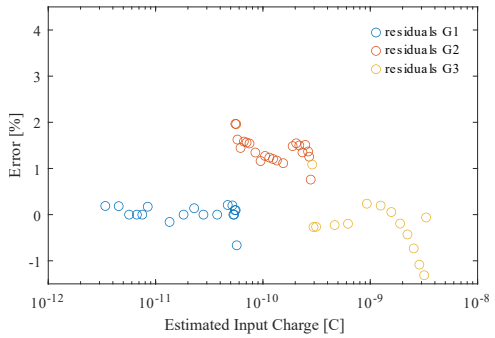
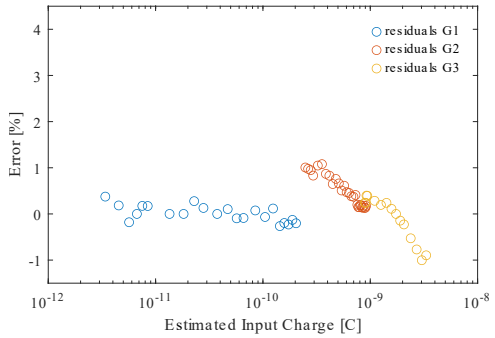



Fig. 18. Static transfer function of the GAMMA ASIC for time- and voltage-threshold (TT and VT) operation mode.




(a)




(b)

Fig. 19. (a) Non-linearity measured over the three interval of the static transfer function from a GAMMA ASIC individual channel, operating in VT mode. (b) Non-linearity measured over the three interval of the static transfer function from a GAMMA ASIC individual channel, operating in TT mode.

and therefore the ratio among different gains could be set to be larger without worsening the ASIC performance.

The chip area is 3.1 mm $\times$ 3.1 mm (Fig. 17). The typical total power consumption 280 mW was experimentally measured. The input stage absorbs 15 mW from the 5 V bias and 1 mW from the 3 V bias. The main contribution to power consumption is given by the DC current absorbed by the filter stages, by the trigger stages and by the DACs (respectively about 25%, 35% and 20% of the overall power consumption, from schematics simulation).

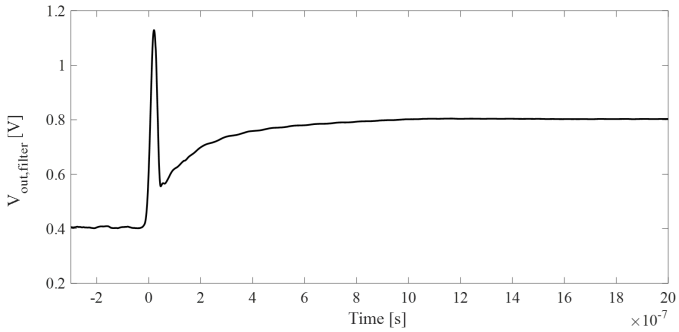



Fig. 20. Measurement of gated integrator output, using the VT operation mode of the AGC. Once the signal overcomes the voltage threshold, the AGC circuit modifies the feedback capacitance, in order to avoid saturation of the gated integrator stage output voltage.

TABLE III
OUTPUT VOLTAGE 10%-90% RISE TIME VS INPUT CAPACITANCE

| Capacitance [nF] | Rise Time [ns] |
|---|---|
| 0 | 60 |
| 1.20 | 80 |
| 4.70 | 180 |
| 72.0 | 2250 |

### A. ASIC characterization

The transfer functions of nine 16-channel GAMMA ASICs were measured for the VT and TT operation modes, in order to collect the data necessary for the individual calibration of the ASIC channels, and to estimate the impact of the ASIC non-linearity on the measured spectrum.

The transfer function of a single channel is shown in Fig. 18. The higher gain at low energies corresponds, for the input in the same range, to a lower equivalent input noise charge that is generated by the electronic readout chain. The TT operation mode of the AGC circuit extends the DR of lower gains, allowing for an output swing of the gated integrator up to 2.7V and avoiding saturation in the same channel.

The data from the aforementioned measurement are interpolated and used to compute the non-linearity error of the transfer function, an example of which is shown in Fig. 19a for the voltage threshold operation mode and in Fig. 19b for the time threshold operation mode. In TT mode, the non-linearity is smaller than $\pm 1\%$ over the entire input charge range of interest.

The characteristics extracted from each channel could in principle be used in post-processing phase for the correction of linearity error. This might be necessary when 15$\mu$m cell SiPMs, the linearity error of which is expected to be reduced of about a factor 4 with respect to 30$\mu$m cell SiPMs in this case study, will be used in future experimental measurements.

An example of experimentally measured response of the gated integrator is shown in Fig. 20. The settling time following the addition of a capacitance to the feedback branch is fast with respect to typical input signal bandwidth and it is, in agreement with simulations, free of notable ringing.

The 10%-90% rise time of the gated integrator output voltage was measured for different values of the input node capacitive load, and it is shown in TABLE III. These measurements allow indirectly to assess bandwidth limitations of the CC while buffering the input current pulses, which is not possible with a direct measurement. The ASIC input is externally connected to a C-R branch on which voltage ramps with steep positive slope are applied using a commercial waveform generator, inducing fast current pulses in the CC (each pulse being the step response of the C-R branch). The C-R discrete components are set in such a way that the current pulse is shorter than the minimum rise time value shown in TABLE III. It is noteworthy that the CC stage is correctly working even for a 72 nF capacitive load at the input.

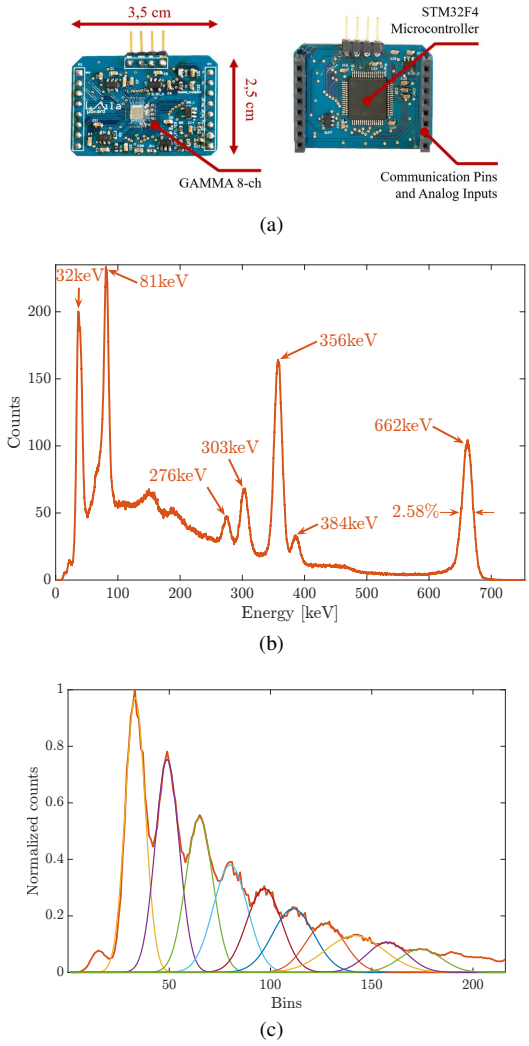



Fig. 21. (a) An 8-channel miniaturized DAQ was used to obtain first experimental results, in order to test the ASIC and validate its spectroscopic capability [40]. (b) $^{137}$Cs and $^{133}$Ba gamma energy spectrum, measured coupling a 3 inch cylindrical $LaBr_3$:(Ce+Sr) crystal to a 144 NUV-HD SiPM array, using a single 8-channel DAQ. (c) Single photon spectrum measured with the GAMMA ASIC, obtained optically pulsing a single NUV-HD SiPM. The laser diode voltage driver synchronization signal was used to trigger the ASIC.

### B. 8-channel DAQ: 16 SiPMs per ASIC channel

The ASIC was experimentally characterized using an 8-channel DAQ [40], [41]. In order to read the entire SiPM detector matrix with only 8 channels (Fig. 21), the large GAMMA FSR was exploited, together with its stability for

large detector strain capacitance. The anode of 16 SiPMs was connected to each channel input, obtaining a sum of the current signals from the detectors in the low impedance input node.

The 16 channels merging implies a high input capacitance of around 50 nF, thus limiting the input bandwidth and implying a long optimum integration time. It is worth noting that it would be challenging for a large-bandwidth regulated cascode input stage to avoid instability, with such a large capacitive load connected at the input. Regardless of this limitation, the developed prototype allowed state-of-the-art resolution measurement of 2.6% at the photopeak emission energy of $^{137}$Cs, 662 keV (Fig. 21b, [42]). Using the same 8-channel microcontroller-based DAQ, up to 24 SiPM anodes were merged together in [40].

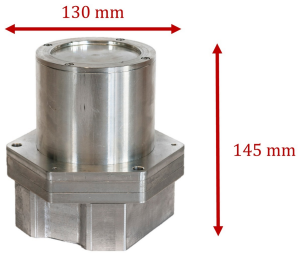
The 8 channel ASIC low-noise capabilities were also tested optically pulsing the NUV-HD SiPMs using a scintillation crystal emulator [36] based on a low-intensity pulsed laser ($\lambda_{em}$= 405 nm). The single photoelectron spectrum shown in Fig. 21c was obtained in these conditions (with 800 ns integration time). A signal synchronized to the low-intensity light pulses was used to trigger GAMMA, which integrated the signal using the highest gain. This measurement is an important demonstration of the GAMMA 84 dB dynamic range, proving single photon sensitivity together with $10^4$ photoelectrons FSR.

### C. 144-channel DAQ: single SiPM per ASIC channel

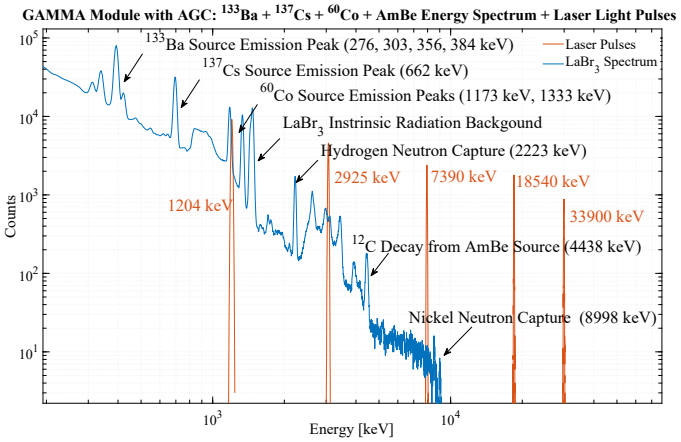
The 16-channel release was exploited in a modular array of 9 ASICs in order to individually read all the 144 SiPMs of the matrix. This solution is meant to extend the energy measurement interval up to 20 MeV, reducing the fraction of saturating events, thanks to the extended FSR of the 16-channel chip, and to densely sample the scintillation light distribution in order to correct the relativistic Doppler effect in nuclear physics experiment [15] using machine learning techniques (in real-time [41] or post-processing).

The 144-channel module is shown in Fig. 22a. The aluminum enclosure hosts all electronics boards. A single 5.5 V biasing voltage is fed to power the system; the SiPM biasing and FPGA-based DAQ biasing are internally generated.

It is shown in Fig. 22b the $^{137}$Cs, $^{60}$Co and AmBe gamma energy spectrum, superposed to spectral lines obtained from a calibrated 410 nm pulsed light source that emulates a $LaBr_3$ scintillation crystal up to 33 MeV; the latter was used to easily test the system at energies otherwise not available in standard laboratories. The spectrum is measured with the AGC circuit enabled while acquiring the data, using the TT operation mode. The obtained energy resolution and non-linearity at different energies are listed in TABLE IV. An energy resolution loss is here observed for the 662 keV spectral line, with respect to the spectrum in Fig. 21b; the main reason behind it is the temperature drift of the module during the 20 hours long spectrum measurement (the 9 MeV peak count rate corresponds to few tens of events per hour), which affects detectors and electronics. A temperature drift compensation might be implemented acting in closed-loop on the SiPM detectors voltage bias [13]. The 4.438 MeV line from the AmBe source resolution is degraded by relativistic Doppler effect. The non-linearity at high energy is due to the detector cell size, in agreement with the model reported in [36].




(a)




(b)

Fig. 22. (a) Module for the experimental validation of the GAMMA ASIC. The aluminium mechanical structure holds the cylindrical crystal coupled to the SiPM matrix and hosts the PCBs for the biasing and the DAQ, and the nine the GAMMA ASICs for the readout of 144 analog channels. (b) $^{137}$Cs, $^{60}$Co and AmBe gamma energy spectrum, measured with the 16-ch GAMMA ASICs, coupling a 3 inch cylindrical $LaBr_3$:(Ce+Sr) crystal to a 144 NUV-HD SiPM array. The spectrum is superposed to spectral lines obtained from a calibrated 410 nm pulsed light source that emulates a $LaBr_3$ scintillation light up to 33 MeV. Each SiPM is individually coupled to a GAMMA input channel, in order to obtain the pixellated image of light distribution, aiming at relativistic Doppler effect correction with machine learning techniques.

TABLE IV
ENERGY RESOLUTIONS OBTAINED FROM FIG. 22B SPECTRUM

| Source or Reaction | Energy [keV] | Resolution [%] | Linearity Fitting Residuals [%] |
|---|---|---|---|
| $^{133}$Ba | 356 | 4.20 | 0.00 |
| $^{137}$Cs | 662 | 3.03 | 0.37 |
| $^{60}$Co | 1173 | 2.38 | 0.22 |
| $^{60}$Co | 1333 | 2.24 | 0.00 |
| $^{1}$H(n,$\gamma$)$^{2}$H | 2223 | 1.40 | -0.72 |
| AmBe | 4438 | 3.1 | 0.4 |
| $^{58}$Ni(n,$\gamma$)$^{59}$Ni | 8998 | 1.66 | -1.66 |

## V. CONCLUSIONS

A 16-channel ASIC based on adaptive gain switching for high DR gamma spectroscopy and imaging was designed and

characterized. It leverages the combination of many ASIC features, such as: the current-conveyor architecture, the AGC circuit and TT operation mode, the 3-switch sampling circuit and the trigger stage architecture. The chip has been exploited for the readout of a 12 $\times$ 12 SiPM matrix, both by merging of 16 detectors per channel (in a 8-channel microcontoller-based DAQ) as well as by means of individual readout of each detector.

Initially, a single-photoelectron spectrum was acquired with channels merging, and a state-of-the-art the GAMMA spectrum providing 2.6% FWHM at the $^{137}$Cs photopeak emission energy of 662 keV was measured with the LAILA-based prototype [42].

In later stages of the experiment, the detectors were individually read by the ASIC channels, enlarging the dynamic range up to 20 MeV and keeping the resolution only limited by statistical processes of photon collection in the SiPMs and from the intrinsic resolution of the scintillation crystal.

The module that features nine GAMMA ASICs will soon be used in beamline facilities in order to validate its energy resolution performances using higher energy gamma-ray sources, and to validate the relativistic Doppler effect correction with machine learning algorithms, thanks to the 144-channel monolithic readout.

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